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# PROCEEDINGS OF SECOND NASA MICROELECTRONICS SYMPOSIUM

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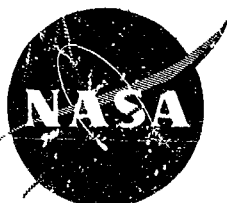
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————— GODDARD SPACE FLIGHT CENTER —————  
GREENBELT, MARYLAND



X-722-67-252

**PROCEEDINGS OF SECOND NASA MICROELECTRONICS SYMPOSIUM**

**September 19-22, 1966**

**GODDARD SPACE FLIGHT CENTER  
Greenbelt, Maryland**

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## 1. GODDARD SPACE FLIGHT CENTER MICROELECTRONICS PROGRAM

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The following paper is a review of the in-house research and development program in microelectronics at Goddard Space Flight Center (GSFC). It covers integrated circuit block development as well as semiconductor process development tasks which have been performed at GSFC.

Three years ago at the first NASA Microelectronics Conference, there was a brief discussion of the way in which the GSFC in-house microelectronics program was to be started. The first aim of the program was to set up a thin-film laboratory where passive circuit components could be deposited and active devices could be added. It was believed that components such as the thin-film transistor and so-called "hot" electronic devices would become available soon and could be integrated with passive elements to make integrated thin-film circuitry. Also some elementary work in solid state silicon devices was anticipated. This work, however, was to be completely secondary to the thin-film effort.

The first thin-film circuit attempted was a low power, low frequency binary, with thin-film resistors and evaporated silicon monoxide capacitors for the passive elements. Miniature diodes and transistors were to be soldered onto the thin-film interconnections. The passive portion of the circuit, fabricated by a contractor, functioned satisfactorily when tested. However, it was discovered that soldering the components was much more difficult than had been anticipated. Consultation with a number of experts in the field revealed that the bonding of any wire, large or small, to a thin-film pad was probably one of the most difficult areas in thin-film technology. At that time the best solution seemed to be the use of a fine, thermal compression, gold wire bonded to the film. This wire in turn had to be bonded to some form of header and the entire assembly hermetically sealed to prevent damage to the gold wire.

As a result of these problems, more serious thought was given to solid state integrated circuit technology. A few initial successes in this area, coupled with a large demand by people at GSFC for this type of circuitry, soon resulted in abandonment of the thin-film approach and directing of the entire effort toward developing solid state devices.

## GSFC THIN-FILM LABORATORY

Before a detailed discussion of the microelectronics program at GSFC, the three main purposes of the thin-film laboratory should be noted.

First, the laboratory provides GSFC with a source of accurate information on the application of new semiconductor devices. Numerous technical representatives come to the laboratory from semiconductor manufacturers with disclosures of new discoveries and techniques which will result in exotic new circuits. Some of these predictions are well founded and some are not. Only a person well versed in semiconductor processes and fabrication techniques can advise an applications engineer on the feasibility of these new ideas.

Second, the laboratory provides a source of solid state circuits which are not available on the open market. To this end, three different integrated circuits have been developed and are currently being used or evaluated for spacecraft applications. Usually these circuits do not have a wide application and, for this reason, are not practical for commercial manufacturers to develop.

Third, the laboratory attempts to reduce the time between experimentation and application of new techniques. There is usually a period of 1 to 3 years between the development of a new fabrication technique in the laboratory and its incorporation into integrated circuits which can be purchased on the open market. Because of its small size and flexibility, the laboratory is able to reduce this lead time considerably and incorporate processes, such as gaseous diffusion and pyrolytic oxide depositions, in a shorter time.

## PROCESS STUDIES

During the last 3 years laboratory efforts have been concentrated in two major areas: process development and circuit development. The majority of the process studies have been conducted under contract. Below is a list of the process studies which have been undertaken:

1. Diffusion from Gaseous Sources — The objective of diffusion of impurities into silicon using gaseous sources was to determine the effects of various dopants on the surface conditions and impurity profiles of silicon crystals.
2. Dielectric Isolation — Dielectric isolation studies were initiated to eliminate the parasitic components introduced into a circuit when PN junction isolation is used. Silicon dioxide isolating barriers were successfully deposited between various electronic components on a circuit in an epitaxial reactor. However, this process needs to be improved to provide a uniform isolating barrier across the wafer and to produce a wafer flat enough, after final polishing, for accurate photoengraving.



3. Photoengraving Techniques -- It was obvious that advanced photoengraving techniques were essential to produce high performance, high complexity integrated circuits. As a result of this study, lines 0.0001 inch wide can be photoengraved. The application was first used on a contract to Marshall Space Flight Center for a mosaic detector calling for 2500 phototransistors to be fabricated on a single piece of silicon, with a 90 percent yield of good transistors. A 100 percent yield was achieved in the resulting detector. This process continues to produce excellent units in the commercial semiconductor field.

4. MOSFETS -- A process for the fabrication of stable and P-channel metal-oxide semiconductor field effect transistors (MOSFET) has been developed. This work, performed by the Westinghouse Corporation, is centered around the doped-gate oxide approach. Several Westinghouse examples of each type of device have proved to be stable. Information about the repeatability or yield of this process is not yet available but the excellent results seen to date are encouraging.

5. Silicon Nitride Insulated-Gate Field Effect Transistors -- An investigation has been initiated into the use of silicon nitride, rather than silicon dioxide, as a material for surface passivation and gate insulation on field effect transistors. A process for deposition of silicon nitride epitaxially has been developed. To date, no field effect devices using this technique have been fabricated, but they are expected in the near future.

6. Evaporated Silicon Resistors -- A requirement exists for a resistor with the following characteristics:

- Sheet resistivity of 5000 ohms per square
- Capable of being photograyed using processes compatible with silicon technology
- Capable of withstanding diffusion furnace temperature up to 1200 °C

The Philco Corporation found that by evaporating silicon onto the passivated silicon dioxide surface on a wafer, a resistor could be formed which meets all of these requirements. The parallel Philco and GSFC efforts have indicated that the process is feasible and that the resistor does meet the ground rules stated above. However, resistor tolerances less than  $\pm 50$  percent are difficult to achieve. In addition, a contact problem has developed between the thin silicon film and aluminum interconnects on an integrated circuit. This problem can be eliminated by utilizing the proper circuit geometry in the contact area. Unfortunately, the poor reproducibility of resistor values precludes use of resistors in anything but experimental circuits at this time.

7. Surface Passivation -- A process has been developed for annealing lead oxide onto a silicon dioxide passivated surface. The process greatly enhances gain and low leakage in bipolar

transistors; it is discussed in detail in another paper, "Surface Effects in Semiconductors Due to Evaporation Techniques."

8. **Pyrolytic Oxides** — A process has been developed for the deposition of silicon dioxide by means of the thermal decomposition of tetraethyl orthosilicate (TEOS). Oxide films using this technique were deposited in thicknesses ranging from several hundred angstroms to greater than 0.001 inch. These films were grown at temperatures between 500°C and 700°C and can be neutral or doped. This technique should have wide applications to processes in which higher temperature steps are to be avoided. Doped oxides might also be used as an impurity source for  $p-n$  junction formation. Circuit fabrication is performed using the processes and techniques mentioned previously.

## CIRCUITS AND DEVICES

The GSFC laboratory has produced numerous circuits and devices, some of which are briefly described below:

1. **Low Signal Transistor** — This transistor was fabricated as a test vehicle for the evaluation of our diffusion processes. The transistor has a VCE saturation of 0.020 volt at a collector current of 0.1 milliamperes and gain greater than 200 at a base current of 1 microampere. Since the processes used in fabricating this device are identical to those used in triple diffused integrated circuit fabrication, the laboratory continues to calibrate its processes by making these transistors.

2. **Thirteen-Input Diode OR Gate** — This circuit consists of 13 diodes with common cathodes, and is packaged in a 14-lead flat pack. A number of these circuits will be used on the statistics computer in the IMP-F spacecraft.

3. **Four-by-Four Diode Matrix** — This triple diffused circuit consists of 16 transistors and 4 resistors. The transistors have their bases and collectors shorted to act as high-speed diodes. The circuit is being used in an advanced OGO experiment to commute pulses with rise times of 20 nanoseconds.

4. **Ten-stage Ring Counter** — A single chip containing two of the 10-ring counter stages was designed and produced in limited quantities. Five of the two-stage chips made up each complete counter. Each chip contained 2 transistors, 2 capacitors, 6 resistors, and 24 diodes. This circuit is particularly interesting because it utilizes all of the techniques available for triple diffusion circuitry, including MOS capacitors.

5. **Two-bit MOS Accumulator** — This circuit is made of MOS transistors and thin-film resistors only. It contains two binaries with signal conditioning, freeze network, reset, and readout

gates. About 30 circuits have been successfully made, but the difficulty encountered with the thin-film resistors has put this circuit in the experimental category. Several problems must be overcome before these units are suitable for production.

## FUTURE PLANS

Future plans include more work on bipolar circuits as well as additional MOS circuit development. The laboratory intends to attempt to use MOS resistors in conjunction with conventional bipolar circuit blocks. The advantage of these resistors is that they have an extremely high sheet resistivity and can be fabricated coincidentally with bipolar components. Some changes will be necessary in the impurity concentrations and profiles of the bipolar components. It will be necessary to determine how these changes affect bipolar operations.

In the area of complementary bipolar circuitry it is generally agreed that high quality PNP and NPN transistors cannot be fabricated in the same circuit block. However, the lateral PNP with unity gain can be fabricated at the same time as an NPN. When it is coupled with an NPN, it exhibits characteristics similar to the conventional PNP transistor. The biggest drawback to the lateral transistor is poor speed characteristics. However, there are a great many requirements in the medium-speed and low-speed fields for which it appears that the device will have excellent application.

Additional experimental work will be carried on in the use of silicon nitride as the gate material in field effect transistors. Insulated gate field effect transistors using silicon nitride will be fabricated and evaluated with the aim of eventually replacing silicon dioxide as a gate insulating material.

There is a great demand by digital system designers for circuits employing complementary insulated gate field effect transistors. The most attractive feature is the extremely low power dissipation in even large arrays of these circuits. The laboratory will work on developing complementary circuits using both silicon dioxide and silicon nitride as gate materials.

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## **2. LANGLEY RESEARCH CENTER MICROELECTRONICS PROGRAM**

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Langley Station, Hampton, Virginia**

Microelectronic technologies are used at Langley Research Center to study many of the problems of aircraft and spacecraft instrumentation. Development of systems using off-the-shelf hardware and in-house hybrids will be continued in order to satisfy in-house requirements. In each area, peripheral research and development will be continued to support projected missions. Emphasis is placed on using thick-film and other bulk material electronic properties to solve advanced payload instrumentation and telemetry problems.

### **INTRODUCTION**

Because of Langley Research Center's (LRC) diverse interests in aircraft and spacecraft and their performance in varied environments, microelectronic studies run the gamut from basic materials research to hardware development. This includes research and development in physical and chemical electronics, studies of advanced electronic techniques leading to miniaturization, and the application of these techniques of advanced spacecraft payloads. Although most future electronic systems will be off-the-shelf hardware, some electronic systems are not amenable to the mass production requirements of integrated microelectronics. Such systems must be made from discrete circuits or from one of the various hybrid forms. Therefore, the present LRC microelectronics program includes development of hybrid techniques, applied materials research, and continued development of new integrated circuit devices.

This paper describes the research and development in microelectronics being performed at LRC. Also discussed are the state-of-the-art of microelectronics at LRC and studies of materials for peripheral devices.

Microelectronic investigations and developments at LRC are in three basic categories: systems, circuits and devices, and materials and components. Ultimately, all programs lead to fabrication of hardware or solutions to hardware problems. However, the scientific procedures

required to approach these solutions cover a wide range of material and device studies; and out of this peripheral work, much basic information is generated and reported. Therefore, research efforts at LRC are primarily concerned with bulk monocrystalline, polycrystalline, and amorphous materials. Investigation of thin-film microelectronics, for the present, has been discarded in favor of studies of thick films. Development and design work are also confined to bulk materials.

## APPLICATION OF MICROELECTRONICS

Virtually all digital circuits in LRC payloads are using off-the-shelf resistor diode transistor logic (RDTL) or diode transistor logic (DTL) integrated circuit microelectronics. The Lunar Orbiter, for example, uses over 600 DTL microcircuits in the inertial reference unit, command decoder, and the programmer. Because of the complexity of the programmer, microelectronic components were essential to maintain limits of volume and weight. The programmer memory handles 128 word commands at 21 bits per word. Listed below are other LRC payloads using microelectronics or hybrid circuits.

Recovery A	— Integrated circuits with hybrid timer
Pacemaker	— Integrated circuits with hybrid timer Anticipate using screened circuit solid-state commutator
Voyager	— Integrated circuits with hybrid timer
RAM	— Integrated circuits with hybrid timer
C5A airplane	— Free flight model, integrated circuits with hybrid

In most of these payloads, microelectronics are used for tape speed compensation, timers, and commutators.

In addition, study programs of future payloads are evaluated with microelectronics in mind. As shown in the photograph of typical systems in Figure 2-1, solder techniques are used on two-layer printed circuit boards. Since printed circuit board and interconnection technology appear to satisfy existing requirements at LRC, multilayer boards and resistance welding have not been adopted. However, advanced interconnection developments supported by LRC are expected to satisfy the future requirements of advanced payloads. These advancements will be discussed in detail later in this paper.

Within the payloads described previously are several interesting circuit developments. Figure 2-2, for example, illustrates the screened circuit, thick-film hybrids developed at LRC. These hybrids are the result of extensive developments in thick-film technology and include a 100-KHz clock oscillator for payloads requiring timers; a low-level switch, which is basically a Bright circuit using dual emitter transistors; and a biaxial ferrite memory sense amplifier, using a Goddard Space Flight Center circuit.

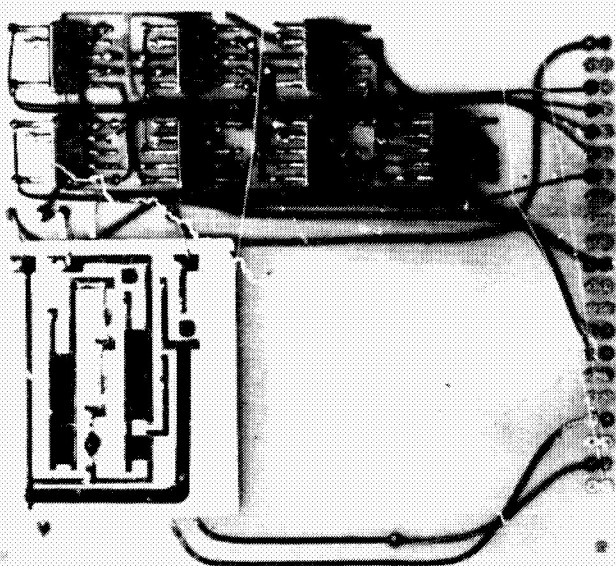
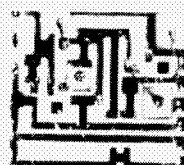


Figure 2-1—Typical microelectronic subsystem used at LRC.

#### ADVANCED DEVELOPMENT

Langley Research Center has extensively investigated analog and digital low power, integrated circuits. Early studies at LRC indicated that integrated complementary bipolar logic would be practical at low speeds; however, practical implementation was very difficult. Figure 2-3 (a) illustrates the basic RDTL complementary gate circuit, a straightforward, complementary form requiring high beta, matched NPN-PNP transistors. In a low power configuration, high impedances are required. While this requirement is easily met with discrete components, mass production of complementary pairs and high resistances by multiple diffusion is considered impractical today. Converting the basic complementary form to an emitter follower

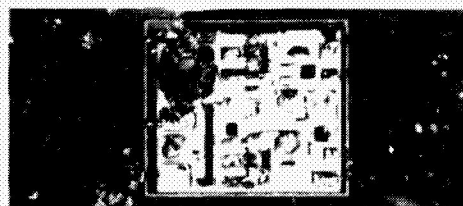
100 KHZ CLOCK OSCILLATOR  
XTAL CONTROLLED



HIGH STABILITY DIFFERENTIAL AMPLIFIER



LOW LEVEL SWITCH



BIAXIAL FERRITE MEMORY SENSE AMP.

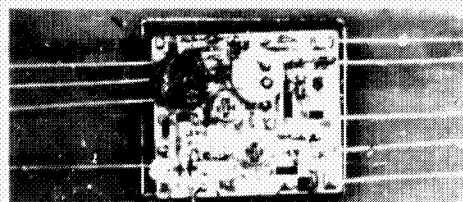


Figure 2-2—Screened circuit, thick film hybrids developed at LRC.

input, as shown in Figure 2-1 (b), reduces the high impedance requirements. The addition of multiple emitters for logic reduces the circuit to a modified transistor-transistor logic (TTL). Texas Instruments, under an LRC contract, developed gates and flip-flops in the TTL configuration. The 1-microsecond propagation time of the TTL, is long; half a microsecond is more desirable. Nevertheless, the flip-flops were square wave clocked up to 700 kHz; at 50 kHz, the power drain was less than 300 microwatts.

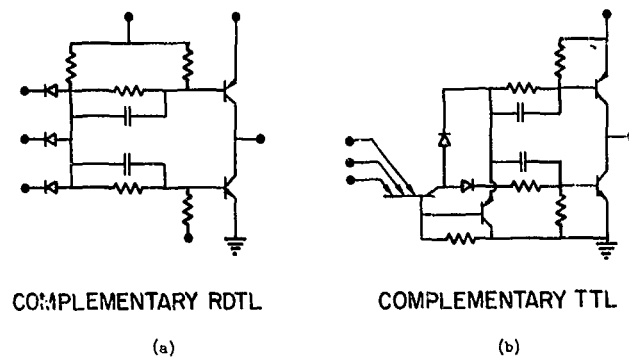


Figure 2-3—Schematics of the basic complementary RDTL gates and the modified TTL gates.

However, the modified TTL did not negate the need for matched, high beta complementary transistors. These transistors were fabricated by doubling the number of diffusion steps, the result being detrimental to process control. Uneven oxide surfaces prohibited using thin-film resistors and evaporated capacitors. Even the gold interconnections had to be bolstered by electrolytic gold plating. However, gold interconnections cannot be mass-produced to take full advantage of the reliability inherent in an existing high-volume process. The need for economical and reliable low-power logic is still great. Future efforts will be concerned with both the development of circuits which are amenable to existing high-volume processes. Simpler complementary fabrication procedures will also be studied.

Logically, the concepts and ramifications of mass-produced hardware must apply to almost all circuit forms and the implementation of systems. Interconnections are not excluded. Although large integrated arrays will solve many of the existing problems, these arrays are not applicable to dissimilar integrated circuits. Under a contract to International Telephone and Telegraph Inc., LRC is investigating the use of a beam lead matrix to interconnect arrayed and nonarrayed integrated circuit chips. In Figure 2-4 the beam lead matrix is compared to the conventional ball-bonded flat pack. Metal, plated on very thin mylar, is etched to the desired circuit configuration; leaving a tiny metallic beam in line with the integrated circuit pads. After a chip pocket has been etched out of the mylar, the chip is inserted and ultrasonically bonded to the metal. Multilayers are used for complex circuits. This chip assembly process can be inspected while the bond is being made. Furthermore, encapsulation does not weaken the integrity of the bond. Because the bonds are made individually or collectively and existing integrated circuit pads are used, a variety of circuit functions and chip sizes are available for use. This program includes an investigation of metallurgical problems, glassing processes, bonding, and substrate materials. In the area of large integrated arrays, Langley Research Center has a contract with RCA, Princeton, to develop 100-milliampere metal-oxide semiconductor (MOS) word drivers and associated logic for laminated ferrite memories. RCA will deliver a test vehicle, consisting of 64 line-integrated word drivers. The MOS drivers were selected because of the high yield possible. A two-step metalization procedure seems to reduce surface leakage. However, as in most MOS processes, cleanliness and crossovers are the greatest problems.



## COMPONENTS, MATERIALS, AND PROCESSES

Recently Robert Stermer of LRC demonstrated modulation of the resistance of a thick, screened-on film of cadmium sulphide by means of electrostatic fields. This development led to the thick-film, field effect transistor. A contract has been awarded to RCA, Somerville, to define processing problems and the potentials of these devices.

While thick films are not the solution to all the problems of microelectronics, these films do satisfy many requirements of size, weight, versatility, and fabrication time. Stable and predictable resistor fabrication is essential, and screened capacitors are highly desirable. LRC has published in a working paper, LWP-190, data which demonstrate test procedures and processing schedules required for screened cermet resistor fabrication. Several capacitors have also been developed using two approaches: dielectric matrix suspension and recrystallization.

The dielectric matrix suspension consists of polycrystalline dielectric powders suspended in a glassy matrix. There is no chemical bond between the glass and the polycrystalline dielectric. These constituents are easily mixed and may be screened and fired on conductors commonly used for screened circuits. Although the dissipation factors are low, practical capacitance

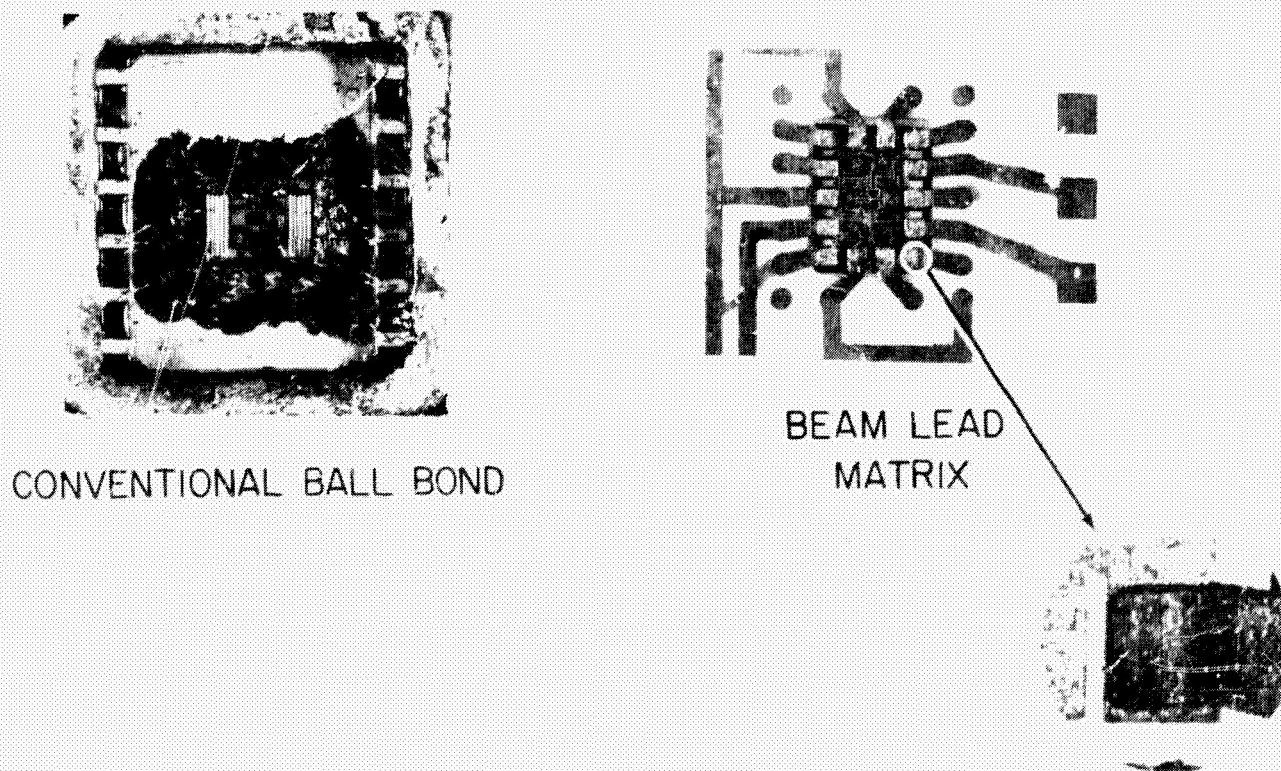
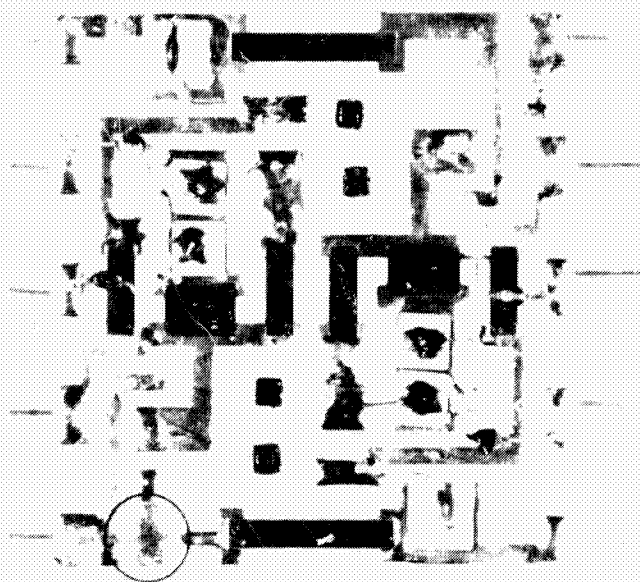
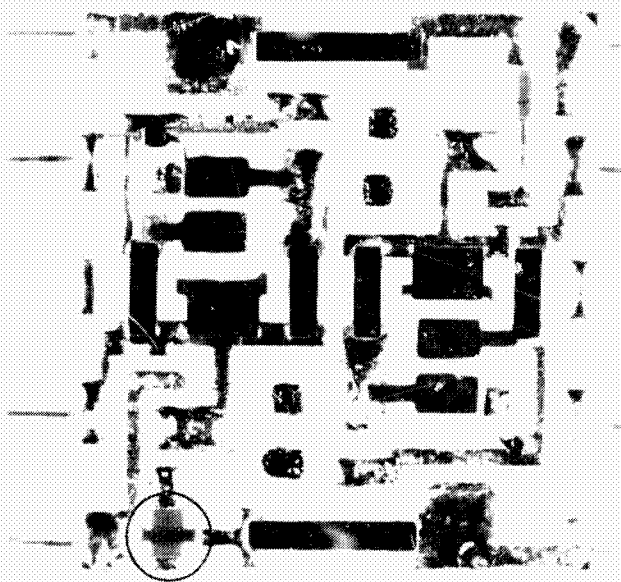


Figure 2-4—Beam lead matrix instrumentation with a close-up of one of the bonds.



1a-BONDED ON CAPACITOR CHIP  
AND CROSSOVER JUMPER



1b-SCREENED ON FIRED ON  
CAPACITORS AND CROSSOVER

Figure 2-5—Screened circuit flip-flops showing discrete and integrated capacitors.

values are limited to 1000 picofarads. The complementary flip-flop in Figure 2-5 shows the capacitors in two forms, discrete and integrated.

To overcome the problem of a low dielectric constants, the polycrystalline densities must be increased. This increase can be achieved by transforming the polycrystalline powders to an amorphous state, crushing to a frit, screening, and firing to recrystallize the dielectrics in place in the circuit. One of the results of this effort is illustrated by the data in Figure 2-6. These dielectric constant versus temperature curves show a comparison of recrystallized and conventionally sintered barium titanate dielectrics. The peak for the conventional barium titanate appears at the Curie point. Note the severe reduction and broadening of Curie point effects for the recrystallized barium titanate.

Uniformly small grains, less than 500 angstroms, are believed to be the cause. In conventionally sintered dielectrics, the relatively large (greater than 10 microns), unevenly distributed grain sizes cause the Curie point to peak significantly at 125 °C. For very small grains, many Curie points can be observed, thereby lessening the gross effect. This

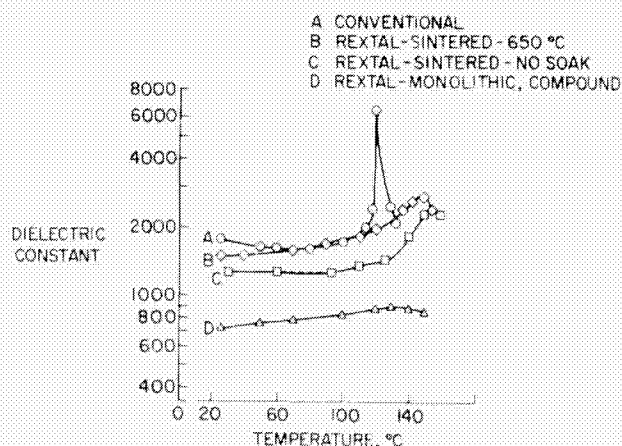


Figure 2-6—Narrowing of the Curie point of conventionally sintered barium titanate and broadening of the Curie point of recrystallized barium titanate.

# ELECTRIC AND MAGNETIC FIELD MICROSCOPE

FERROELECTRIC DOMAIN WALL STUDIES

SURFACE FAULTS ON CRYSTALLINE SILICON

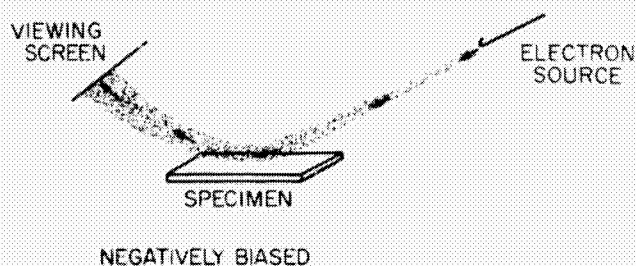
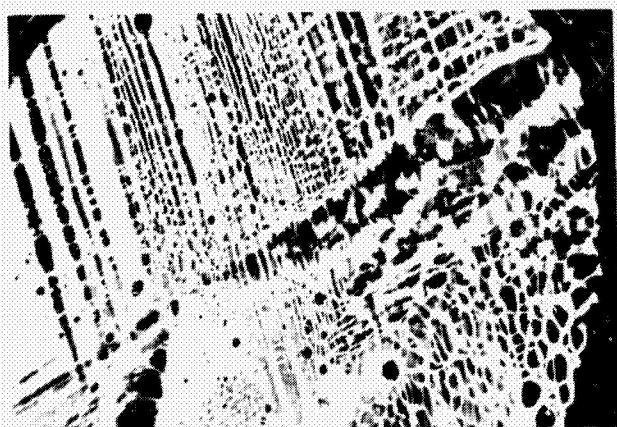
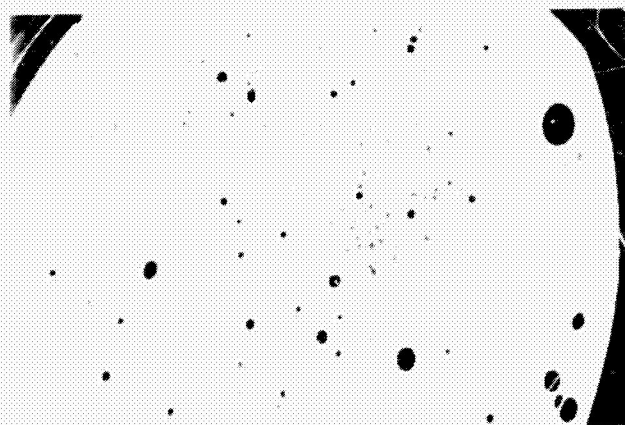


Figure 2-7—Operation of an electron mirror microscope.

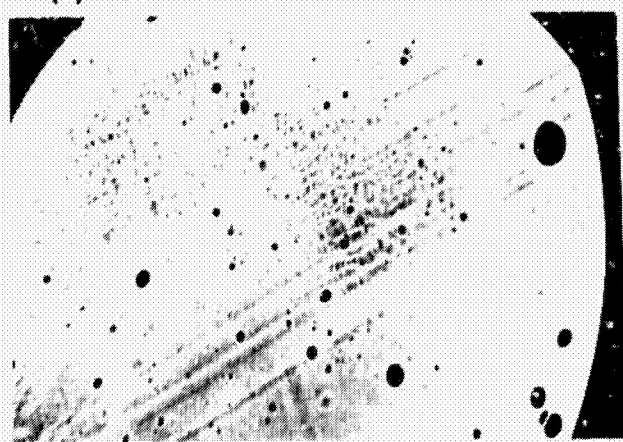
phenomenon means that nonlinear dielectrics such as barium titanate may possibly be stabilized to operate over several hundred degrees. As no existing theory could predict this effect, much more theoretical information regarding polycrystalline dielectric behavior is required before the true performance of nonlinear polycrystalline dielectrics is realized. The Illinois Institute of Technology Research Institute, under contract to LRC, is investigating the basic characterization of barium titanate. This investigation is a new approach to develop a working theoretical model of grain and grain boundary contributions to dielectric properties.



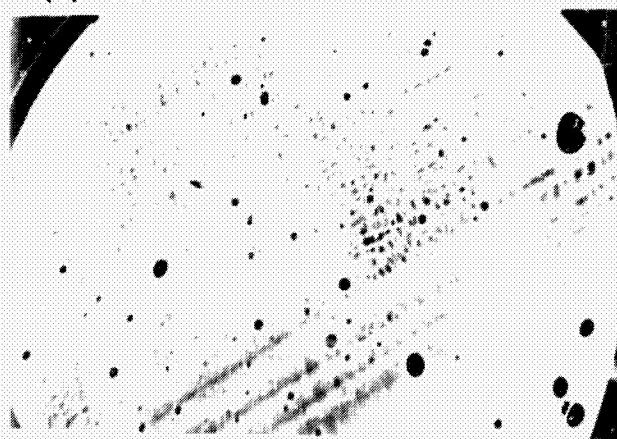
(a) 120°C ASCENDING TEMP



(b) 120°C DESCENDING TEMP



(c) 118°C DESCENDING



(d) 116°C DESCENDING

Figure 2-8—Electron mirror micrograph of the movement of domain walls on the surface of crystalline BaTiO<sub>3</sub>.



During the characterization program, LRC has conducted studies of crystalline barium titanate surfaces with an electron mirror microscope. As illustrated in Figure 2-7, the electron beam is directed to a charged specimen but is deflected away by a negative bias. The resultant image is a projection of electron paths perturbed by the electric charge field on the surface of the specimen. Figure 2-8 illustrates electron mirror micrographs of the movement of domain walls on the surface of the barium titanate at specified temperatures. In (a) the temperature is at 120° C and is increasing to the Curie point of 125° C. Though these data have not been reduced, it is significant that dynamic domain action of bulk materials can be seen easily with the mirror microscope.

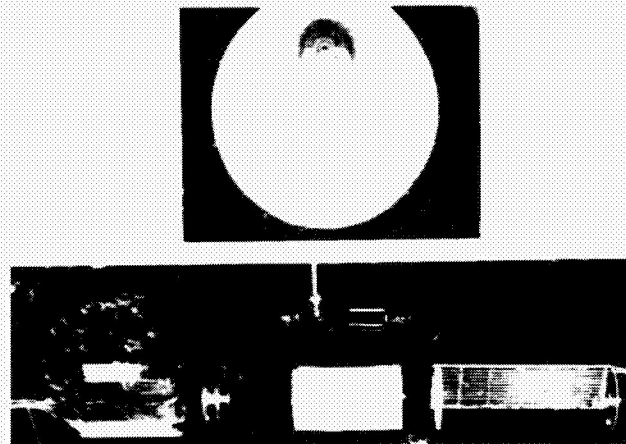


Figure 2-9—Restricted gas flow in a diffusion furnace and experimental baffles.

Finally, in conjunction with multiple diffusion processes, Figure 2-9 presents photographs of restricted gas flow into the diffusion furnace and experimental baffles. Working with internal aerodynamics at LRC, the baffle arrangements were developed to break up this gas-flow pattern and obtain a well-mixed flow pattern.

#### CONCLUDING REMARKS

In fiscal year 1967 LRC will continue system and circuit prototype development for experimental payloads. Voltage controlled oscillators with very small constant bandwidths are now under development. Completion of the beam lead matrix interconnectors is expected to satisfy many of the future payload instrumentation requirements. Although LRC has not yet converted to S-band telemetry, microelectronics applications are being considered and will be pursued after completion of a 3-watt UHF FM transmitter. The solutions to many system problems lie within material technology. Microminiature thermistor bolometers, for example, are being investigated to correlate material behavior, processing, device performance, and system requirements. Solid solubilities in semiconductor crystals, polycrystalline semiconductors and dielectrics; characterization of polycrystallines; and diffusion studies are essential to the ultimate reliable performance of very small components, sensors, and systems.

N67-31565

### 3. MARSHALL SPACE FLIGHT CENTER MICROELECTRONICS PROGRAM

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A generalized discussion concerning the background, managerial philosophy, and implementation of the microelectronics program at MSFC is presented. The objective of the program is to increase reliability and flexibility and reduce the cost of electronic systems of Saturn vehicles and Apollo application programs within the Center's responsibility. The effort is MSFC and NASA mission-oriented to identify areas that require fundamental research, technological advancement, and hardware implementation in support of mainstream responsibilities. The importance of supporting research as an integral part of the overall plan, along with areas of competency, is also described.

#### INTRODUCTION

The specific objectives of the microelectronics program at the Marshall Space Flight Center (MSFC) are to increase reliability and flexibility, while reducing the cost of flight and ground electronic systems of Saturn vehicles and Apollo application programs within the Center's responsibility.

Present Saturn systems were in the design stage before anyone had a "handle" on reliability numbers and confidence levels of microcircuits. As a result, most Saturn electronic systems are built with discrete components. In general, these discrete components are of the "micromin" variety generated during development of the Redstone, Jupiter, and Pershing missiles, which preceded the Saturn. Although schedule and funding constraints and ground rules for Apollo applications have limited the microcircuitization of existing electronic systems, solid-state devices have a long history at Marshall. For example, the Redstone flew in the early 1950's with no tubes in the critical elements of the guidance and control systems. This early interest and involvement in solid-state devices by MSFC design engineers has grown with the multidisciplinary technologies that have spawned the present microcircuit industry. Saturn electronic systems designers continue to study and evaluate developments in microcircuit techniques for possible applications for existing systems and the Apollo applications program.

## TRENDS IN SPACE VEHICLE COMPLEXITY

Because of space, weight, reliability, and cost considerations, it appears imminent that microelectronics will be the way of the future in both the aerospace and commercial markets. However, the trends in complexity and requirements of space vehicles should be touched upon to emphasize MSFC's preoccupation with techniques to implement increasing demands.

A number of parameters could be used to indicate trends in complexity and requirements. However, time and part-count are rather fundamental ones that will suffice, especially when one considers their related theoretical and practical aspects. For example, the controlled flight time of the Redstone vehicle that launched America's first astronaut on May 5, 1961, was about 6.5 minutes, and the electronic part-count was about 40,000. Five years later, the controlled flight time of the multistage Saturn V vehicle was more than an order of magnitude greater, while the part-count, not including the command, service, and LEM modules, was increased by nearly two orders of magnitude. When one considers Apollo applications missions in terms of months and post-Apollo applications missions in terms of years, it becomes apparent that every plausible means of achieving excellence must be explored. Microelectronics presents the best means of extending electronic system life and coping with the mushrooming part-count problem.

## MICROELECTRONICS PROGRAM IMPLEMENTATION

The program oriented microelectronic effort at MSFC provides direction regarding the type of systems meriting study, the type electronics that can best implement these systems, and the research and technology necessary to support system development. This is not to say that all research projects are linked to specific hardware projects. Generally, however, basic research is directed toward advancing the state of the art to support MSFC and NASA overall program requirements through the cooperative efforts of system design and analysis, subsystem definition and implementation, and supporting research — both in-house and contractor.

The Astrionics Laboratory of MSFC, with responsibility for all vehicle electronic equipment and electronic launch-site ground-support equipment, serves as the "center of gravity" for microelectronic efforts. A systems engineering office, reporting to the Astrionics Laboratory Director, functions as a focal point for overall systems design and analysis and coordinates the efforts of the several laboratory elements in subsystem definition and requirements. Subsystem implementation is the responsibility of individual laboratory elements. An R&D advisor on the laboratory director's scientific and technical staff works closely with the systems engineering office and laboratory elements to determine current and future research and technology requirements. The director critically reviews laboratory requests and submits his plan to the Center program office. Therefore, software, hardware, and R&D are in tune with the MSFC and NASA overall program plans.

## HARDWARE DEVELOPMENT

The approach to microcircuitizing current hardware at MSFC has been a systematic process, in consonance with general electronic program implementation and in accordance with funding, schedules, and Apollo application guidelines. As a first step, the Engineering Systems Office and the major elements of the Astrionics Laboratory analyzed the guidance and control system of the Saturn vehicle. The first objective of the analysis was to determine which critical subsystems (or black boxes) could be updated with microcircuits and possibly phased later on into the Apollo system. This would serve as a backup procedure in critical areas. The second objective was to identify those subsystems fundamental to the design of the special guidance and control systems necessary to meet the stringent requirements of future Apollo applications programs. If the subsystems were not phased into the Apollo program, they would be available for Apollo applications programs. An important addition to this overall approach would be experience gained in the reliability, analysis, and application of microcircuits in space vehicles.

## RESEARCH AND DEVELOPMENT

Historically, MSFC management has maintained a strong in-house capability since it is felt that those actively engaged in a research and development program are most aware of state-of-the-art developments and how they may be utilized to enhance mainstream programs and resolve problems. Furthermore, the experience and knowledge gained in such developments permits more effective management direction of contractor efforts. This is especially true as interdisciplinary boundaries begin to disappear as science and technology become more sophisticated. MSFC has established excellent facilities for microcircuit research, development, and prototype fabrication of both the thin-film and monolithic types. A much lesser degree of effort has been devoted to thick films and some hybrid types. Much of the in-house and out-of-house research and development is directed toward the solution of problems associated with selected "black boxes" or critical subassemblies. Other efforts include the establishment of a reservoir of scientific and technological knowledge that will be immediately available to meet the challenges of the burgeoning field of microelectronics.

## CONCLUSION

Fulfillment of the increasingly stringent requirements of future missions will depend to a large degree upon the ability of the NASA community to utilize microcircuitry effectively. This problem is not peculiar to NASA. It is typical of changing times and requires a new look. A quote from Captain B. H. Andrew's keynote address at the Third Conference on the Navy Microelectronics Program in 1965 indicates the Navy's concern. "Despite our best efforts to keep things simple, modern military operations are complex and getting more complex with every passing day. Most complex problems have complex solutions. Ample evidence of this is seen in the

trends in electronic equipments aboard our destroyers over the past 20 -year period. We have had a tenfold increase in weight and power consumption, a 7-to-1 increase in volume, and a 2-to-1 increase in the cost of purchasing this electronics equipment. . . . Widespread use of microelectronics has substantiated our belief that the complex physical, chemical, and electronic technologies which comprise microelectronics are passing through a critical transitional phase. This period of rapid acceleration from laboratory techniques to reliable hardware in the fleet is one in which the closest communications must be maintained between the research community and the development community."

Certainly the requirements of an astronaut in space will be as severe as those of the captain of a ship at sea.



**N67-31566**

#### 4. STUDY OF METALLURGICAL PROBLEMS RELATED TO MICROELECTRONICS RELIABILITY

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As part of a long-range effort to improve aerospace electronic component reliability, a study was undertaken to develop new metallurgical techniques for analysis of microelectronic device structures. The metallurgical problems investigated included interconnections, metal-semiconductor contacts, intermetallic compound formation, and thin-film process control. The instrumentation utilized for this study is briefly described. An electron probe microanalyzer was used to scan the sample with a finely focused beam of electrons and to obtain information from the generated characteristic X-ray spectra, back-scattered electrons, secondary electrons, or specimen current. The gold-molybdenum metallization on integrated circuits was examined to determine changes in the microstructure occurring during various heat treatments. An X-ray spectrometric method was developed for measurement of the thickness of aluminum films on silicon slices, affording improved control of the metallization process. A measurement accuracy of  $\pm 6$  angstroms for very thin aluminum layers has been achieved.

#### INTRODUCTION

For many years, there has been an increasing recognition of the importance of the application of physical, chemical, and metallurgical techniques for understanding failure mechanisms in microelectronic devices as an interdisciplinary field separate from that of the development of new electronic devices. One of the major functions of the Failure Mechanisms Branch of the Qualifications and Standards Laboratory of the Electronics Research Center is to carry out a research program for improved detection of the microscopic changes in device materials which may lead to failure under operating conditions in aerospace environments.

Better understanding of the basic failure mechanisms in microcircuits as a means of improving reliability has the following goals: (1) prediction of operating life based on physical, chemical, and metallurgical theory; (2) correction of unsatisfactory processing; (3) improved

screening techniques and accelerated testing; and (4) better process controls. A recent survey (Reference 1) has indicated that 58 percent of failure modes in integrated circuits are primarily metallurgical problems, while open thermocompression bonds constitute 24 percent, metallization defects are 12 percent, internal lead discrepancies are 10 percent, and die-to-header bond defects are 12 percent. Several of the contracts sponsored by the Failure Mechanisms Branch, including those with Autonetics (Reference 2), Librascope (Reference 3), Motorola (Reference 4) and Mallory (Reference 5), involve problems of interconnections, failure analysis, and pertinent instrumentation. This paper will not review the contract work, but will present the results and future plans of the in-house research program on metallurgical problems.

#### ALUMINUM METALLIZATION

Aluminum has been a logical choice for metallization on silicon planar transistors and integrated circuits for several reasons:

1. It forms ohmic contacts with silicon.
2. It has excellent adherence to silicon oxide.
3. It is easy to apply by evaporation.
4. It is available at low cost and high purity.
5. It has high electrical conductivity.

Two popular methods of lead attachment to the aluminum metallization are thermocompression ball-bonding of gold wire and ultrasonic bonding of aluminum wire. The gold-aluminum interconnection system has been under investigation for several years. The crux of the problem is the interaction of the two metals at temperatures greater than 200°C or under high stress conditions. In one case, a brittle intermetallic forms around the periphery of the gold ball-bond, resulting in intermittent or open contacts. This type of failure is shown in Figure 4-1(a). Failure analysis has

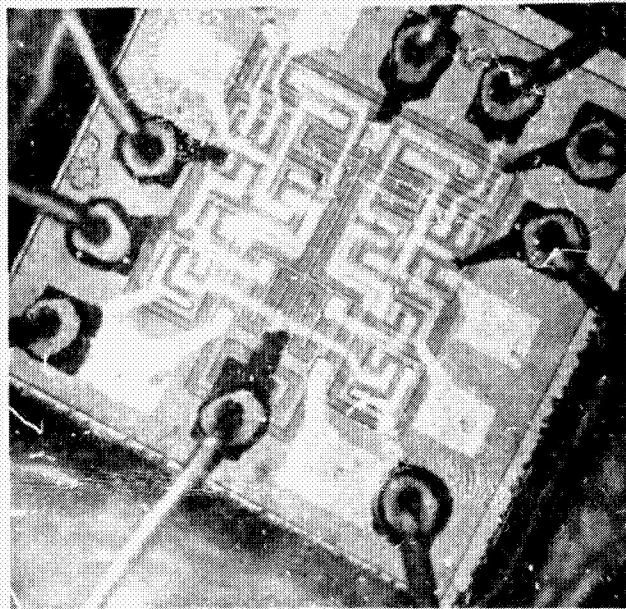


Figure 4-1—Formation of  $AuAl$ . (a) Around gold ball bond. (b) Along aluminum conducting strips.

shown that the growth can continue along the length of the aluminum conducting stripes, causing voids as in Figure 4-1(b). Although replacing the gold leads with aluminum ones eliminates difficulties due to gold-aluminum interactions, there still remain problems relating to the reliability of the aluminum-aluminum bond and the current-carrying capacity of the aluminum metallization as a function of time, temperature, and ambients.

A recent report (Reference 3) has indicated that there is a complex relationship between the current density in the aluminum metallization and the operating lifetime at various temperatures. An unexplained difference has been found between the operating lifetime when the conductors are subjected to comparable values of alternating and direct currents. In the case of oxide-passivated silicon devices, aluminum can cause electrical degradation in the form of soft reverse breakdown characteristics, high saturation currents, decreased current gain, and even short circuits.

A number of phenomena have been observed in-house on commercially available integrated circuits subjected to operating and storage stress testing in contractual work done by Librascope (Reference 3). These phenomena relate to reliability limitations of aluminum metallization on  $\text{SiO}_2$  surfaces of silicon devices and integrated circuits. Failure analysis has revealed open metallization, ragged edges on aluminum metallization, total disappearance of aluminum from certain regions, short circuits, changes in aluminum sheet resistivity, and reactions of aluminum in contact with other metals which result in formation of intermetallic compounds and/or loss of adhesion between aluminum and  $\text{SiO}_2$ . Conditions which could produce these phenomena are a reaction of aluminum with  $\text{SiO}_2$  to give silicon plus aluminum oxide; formation of an aluminum-silicon eutectic phase; chemical reactions to form oxides, nitrides, or other aluminum compounds; agglomeration (lateral migration) of aluminum on the  $\text{SiO}_2$  surface; diffusion of aluminum through  $\text{SiO}_2$  layers; influence of aluminum bonded to aluminum on the properties of the film in the vicinity of the bond; and electrolysis occurring as a result of an electric field crossing the dielectric and anodizing the aluminum metallization at positively biased electrodes.

Integrated circuits which had been on storage life at  $250^\circ\text{C}$  for 2500 hours were opened for observation. When one circuit was examined, it was observed that some of the aluminum had disappeared. After removal of the remaining aluminum by chemical means, the regions where the aluminum metallization had existed were observed in monochromatic light. It is believed that the pattern visible after removal of the aluminum (Figure 4-2) is a result of the interface reaction of the Al- $\text{SiO}_2$  system. It was noted that gross pitting occurred in certain areas of the  $\text{SiO}_2$ . In several instances, the pitting was so severe that the device had become electrically shorted. In other cases, "hot spots" had resulted, causing the resistance of the contact to increase to the point where the current density per unit area exceeded the current-carrying capacity of the aluminum film. Because increased temperature accelerated the failure mode, and because the physical appearance of the metallization was changed, it was concluded that these failure mechanisms are chemical in nature. It is significant that certain areas of devices subjected to power stress testing are more susceptible to failure than others. Because increased temperature apparently accelerates the failure mechanism, it is likely that the areas prone to failure during stress operation are

regions of localized high operating temperature. The areas especially susceptible to failure during stress testing include: (1) metallizations crossing elements of the device which dissipate considerable power, (2) metallization near contact cuts, and (3) metallization near oxide steps. Because of the procedures used for deposit-metallization, failures in the latter two areas may result because of constriction in the cross-sectional area; this causes increased resistance to current flow, and hence localized heating.

Another metallization failure mode is a growth which begins in contact windows and progresses outward along the metallization. This mode is also attributed to localized heating. Under microscopic examination utilizing vertical illumination, the growth appears as a black granular substance and is accompanied by a substantial increase in volume over the original aluminum metallization. The growth appears silver-white when viewed with a dark field or side illumination. Failures of this type normally occur during stress operating life at dissipations far in excess of the device rating, and failure is due to short circuiting of the device. The failure mode is believed to be the reaction of aluminum with silicon to form an aluminum-silicon eutectic.

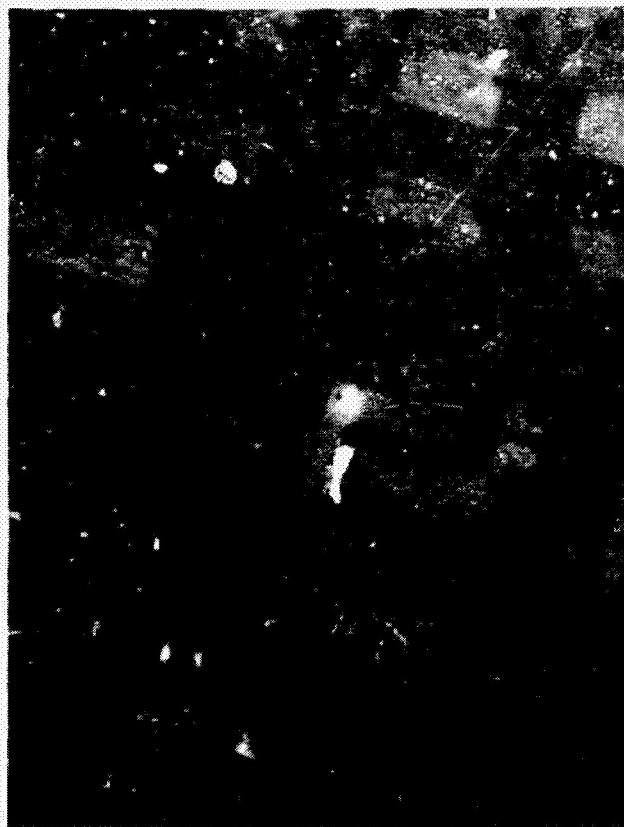


Figure 4-2—Intermetallic reaction between aluminum and  $\text{SiO}_2$ .

## X-RAY SPECTROMETRY

During the fabrication of integrated circuits with aluminum metallization, there is one stage at which the entire silicon slice is covered with deposited aluminum, before the excess areas of metallization are removed by photoetching techniques. In order to provide a method (Reference 7) for nondestructive examination of the thickness of deposited aluminum that could be used for process control on every slice used, a technique was developed using a commercially available X-ray fluorescence spectrometer (Philips Electronics, 50-kv, 50-ma power supply, FA-60 tungsten target tube, inverted four-position sample holder, vacuum spectrometer with EDT crystal and flow proportional counter). Two basic principles were involved in the investigation: emission of the characteristic aluminum K-alpha fluorescence by the aluminum film, and absorption by the aluminum film of the silicon K-alpha fluorescence radiation emitted by the substrate. The X-ray spectrometric technique for determining aluminum thickness on silicon has the following advantages over optical interferometric measurements:

1. It has greater sensitivity.
2. It does not require a step view showing both film surface and substrate surface.
3. The results appear in digital form compatible with an automated process control.

The samples, consisting of silicon wafers coated with vacuum-deposited aluminum, were exposed to the actuating X-ray radiation from the tungsten tube over an area of 0.625-inch diameter limited by stainless steel masks. Corrections were made for slight geometrical variations in the mask positions in each cell by comparing the counts from identical silicon samples. Calibrations were carried out by interferometric measurements with a Zeiss Interference Microscope in thallium light at 0.54 micron. For aluminum thicknesses below 1 micron, it was considered more advantageous to use the theoretical curve for the X-ray curve, because of the relatively poor sensitivity of optical interference measurement.

The dependence of the intensity of the characteristic aluminum K-alpha radiation  $I_t$  on the thickness of aluminum can be expressed by

$$\frac{I_t}{I_0} = 1 - e^{-At}, \quad (1)$$

where  $I_0$  is the radiation from thick (over 40 microns) aluminum,  $t$  is the thickness in microns, and  $A$  is a constant. The constant  $A$  can be calculated by

$$A = \frac{\mu_p}{\sin \phi} + \frac{\mu_s}{\sin \psi} \quad (2)$$

where  $\mu_p$  and  $\mu_s$  are the linear absorption coefficients of aluminum for the primary and fluorescence radiation, respectively;  $\phi$  is the angle of incidence of the primary radiation with the specimen surface; and  $\psi$  is the angle of emission of the fluorescence radiation. The second term was calculated from the data of Cooke and Stewardson (Reference 10), but the first term was determined experimentally. The variation of the ratio  $I_t/I_0$  with the thickness  $t$  is shown in Figure 4-3. Based on background fluctuations, the limit of sensitivity for a counting time of 100 seconds was estimated to be  $\pm 6$  angstroms of aluminum.

#### GOLD-MOLYBDENUM METALLIZATION

Alternate bimetal systems are now being used in various microelectronic facilities. Gold-molybdenum is of particular interest. Gold being a noble metal is noncorrosive and lends itself to integrated circuit processing. It is not desirable to have gold in contact with silicon, because of migration and lifetime degradation problems. The molybdenum is used as a barrier layer, and can be deposited by electron beam evaporation or the thermal reduction of molybdenum compounds. The molybdenum is selectively removed by photolithographic techniques, and the gold is deposited.

It has been claimed that the gold-molybdenum system is stable, that there is no intermetallic formation, and that the mutual solid solubility of gold and molybdenum is exceedingly small. Devices that were heated to 300° C for 2400 hours and sectioned indicated no movement or intermetallic formation at the gold-molybdenum interface. It is also important that there be no lateral movement of the gold across the surface of the molybdenum or SiO<sub>2</sub>. A study is presently being made to examine integrated circuits with gold over molybdenum interconnections for evidence of surface diffusion or migration. Integrated circuits are masked and the gold selectively removed from certain areas to reveal the molybdenum barrier layer below. The specific areas running across the gold to the gold-molybdenum interface and on across the molybdenum are scanned with the electron beam probe. The circuits are then subjected to heat treatment in an inert atmosphere at temperatures ranging from 200 to 600° C. The identical areas are examined after heat treatment to reveal any changes that have occurred.

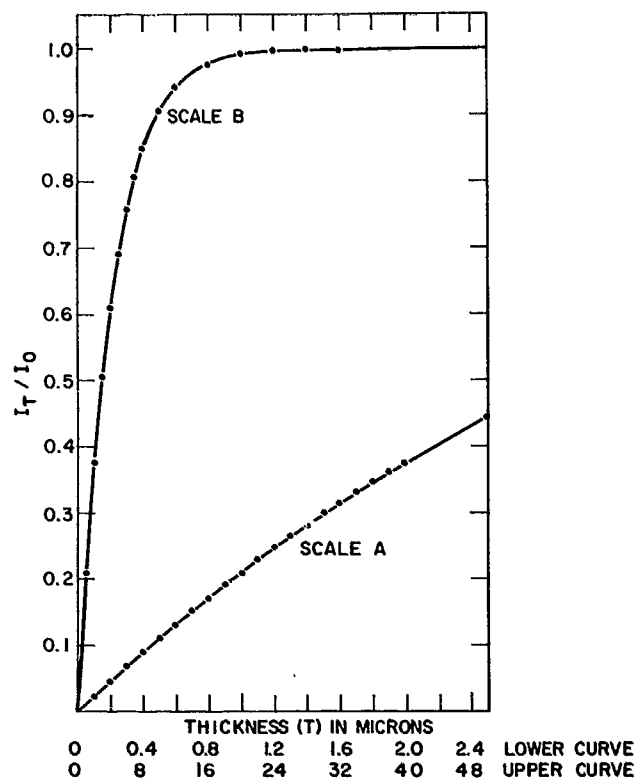


Figure 4-3—Intensity of aluminum K-alpha X-ray fluorescence as a function of thickness of aluminum on silicon.

## ELECTRON PROBE MICROANALYSIS

The electron probe microanalyzer used in this investigation was manufactured by Acton Laboratories, under license from the French firm Cameca. It is of recent design and has many features not found in older instruments. The electron optics system focusses a beam of electrons to a spot diameter of 0.3 to 1.0 micron, depending on the current density. At the point where the electrons strike the specimen, characteristic X-ray spectra of the chemical elements are generated to a depth of 1 to 3 microns below the surface. If appropriate crystals and detectors are used, all the elements from boron through uranium can be detected in approximately 1 cubic micron of material. The sample area can be simultaneously observed and photographed with a 400X optical viewing system. In addition to X-ray generation, the variation in specimen current is an indicator of changes in surface topology and material content, since these factors vary the fraction of the electron beam that is backscattered.

The information obtained by the electron probe microanalyzer can be recorded by:



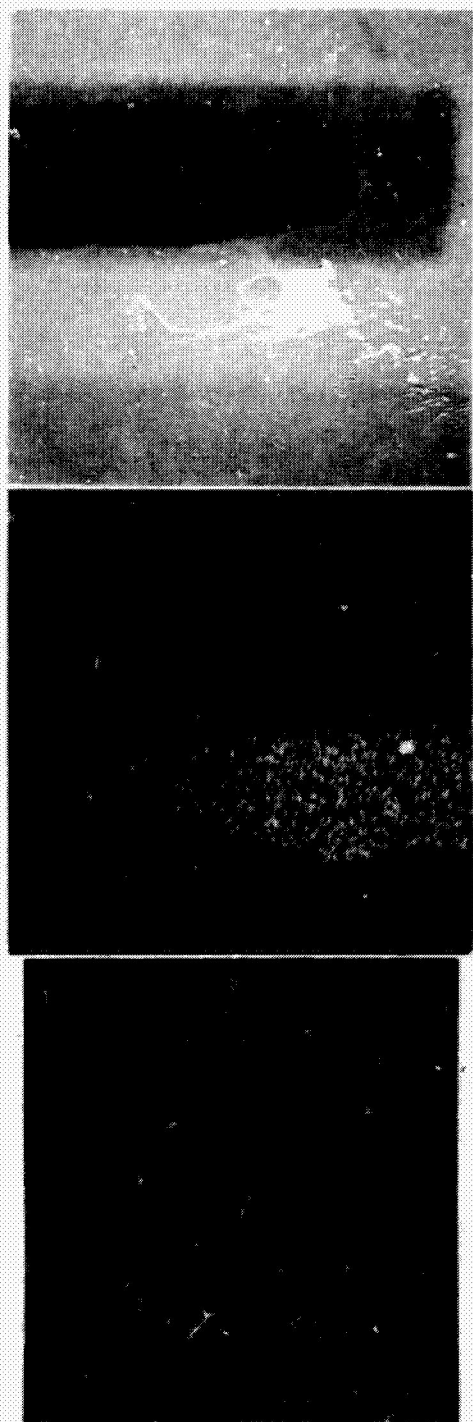


Figure 4-4—Area B of gold-molybdenum metallization, 150 x 150 micros, before heat treatment. (a) Electron micrograph. (b) Gold L-alpha X-ray image. (c) Molybdenum K-alpha X-ray image.

1. Direct counting of X-ray quanta, and reading sample position (to 1 micron) and x- and y- directions.
2. Chart-recording X-ray intensity, synchronized with mechanical linear scans.
3. Chart-recording X-ray intensity synchronized with mechanical variation of spectrometer wavelength setting.
4. Photographing oscilloscope display of either specimen current or X-ray counts during electrical or combined mechanical electrical raster scanning of the sample.

For every X-ray quantum reaching the spectrometer detector, approximately 1000 electrons must bombard the sample. Since the accuracy of the X-ray data is often limited by the statistical variation due to the total number of quanta counted, it can be seen that the number of electrons bombarding the sample can be reduced when specimen current readout is used instead of X-ray readout. Thus, after the general areas in the sample have been identified by X-rays, the fine structure can be shown in greater detail by an electron micrograph based on specimen current variations. Good contrast in specimen current is shown by elements with widely varying atomic weight, since the fraction of backscattered electrons increases significantly with atomic weight.

In Figure 4-4, an area of gold-molybdenum metallization, 150 by 150 microns, is shown before heat treatment as photographed with three different types of oscilloscope displays. Figure 4-4(a) is an electron micrograph scanned in 6 seconds, showing the gold area as very dark, the molybdenum area as medium

gray and the surrounding oxidized silicon surface as very light. Figure 4-4(b) shows the gold L-alpha X-ray quanta accumulated over 10 minutes of scanning with a total count of 11,780 X-ray quanta. Each X-ray quantum counted appears as a white mark. Figure 4-4(c) shows the molybdenum K-alpha X-ray quanta accumulated over 120 minutes of scanning with a total count of 9900. The lower signal-to-noise ratio in this scan decreases the contrast. This area was identified as area B, and further studies were made on it after heat treatment. These studies will be described.

In Figure 4-5, area D is shown by electron micrographs (a) before heat treatment, (b) after 4 hours at 350° C and (c) after an additional 4 hours at 600° C. There were some very noticeable effects after 600° C. For example, in Figure 4-5(c), one can see a distinct equilateral triangle. This was identified as the area containing gold (Figure 4-6). This area is shown as an (a) electron micrograph and (b) a gold L-alpha X-ray image. The same area D is shown before heat treatment (Figure 4-7) by (a) electron micrograph, (b) gold L-alpha, and (c) molybdenum K-alpha image.

In addition to oscilloscope information, data was taken by mechanical linear scans over the lines shown in Figure 4-6(a). In Figure 4-8, the scans are plotted in a form showing a 3-dimensional contourograph of the area with (a) molybdenum K-alpha, and (b) gold L-alpha. A similar contourograph of a gold-molybdenum area is shown in Figure 4-9, with (a) molybdenum K-alpha, and (b) gold L-alpha. Often the contourograph gives a sharper definition of gold-molybdenum boundaries than the oscilloscope image since the number of quanta counted per unit area is greater. More highly enlarged images of area E shown in Figures 4-10 and 4-11 reveal changes both in specimen current and gold X-ray images after heat treatment at 600° C.



Figure 4-5—Area D of gold-molybdenum metallization, 300 x 300 microns, electron micrographs. (a) Before heat treatment. (b) After 4 hours at 350°C. (c) After additional 4 hours at 600°C.



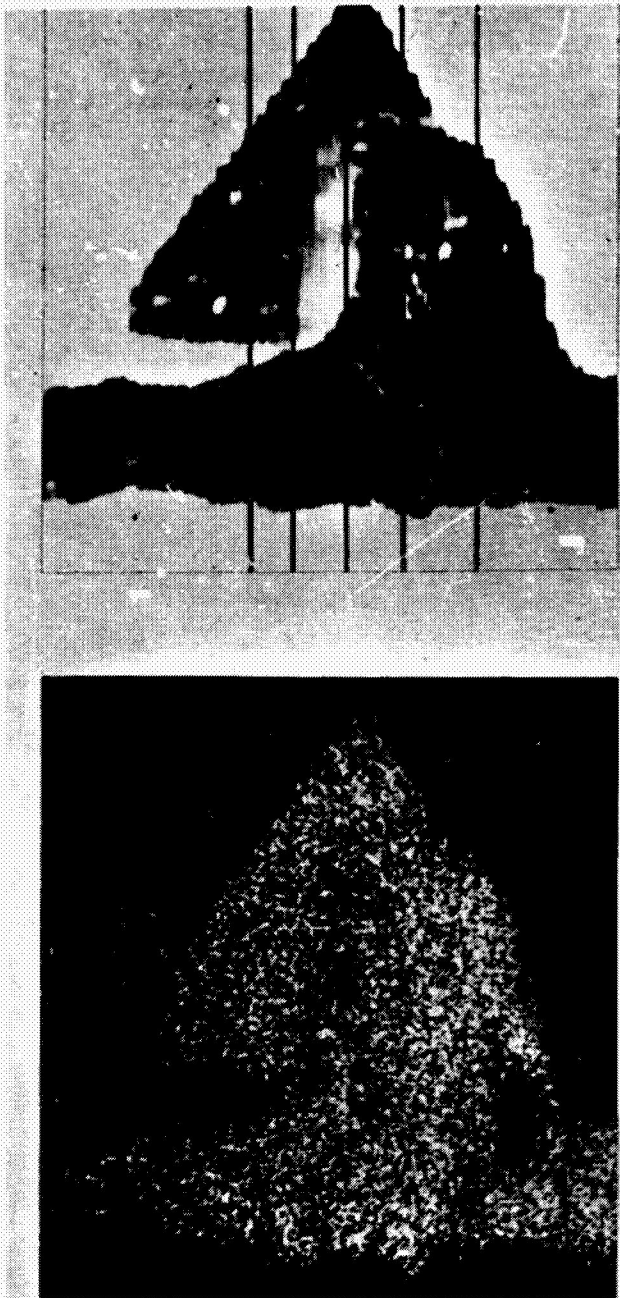


Figure 4-6—Area D of gold-molybdenum metallization after heat treatment at 600°C, 110 x 110 microns. (a) Electron micrograph with positions of 5 linear scans shown. (b) Gold L-alpha X-ray image.

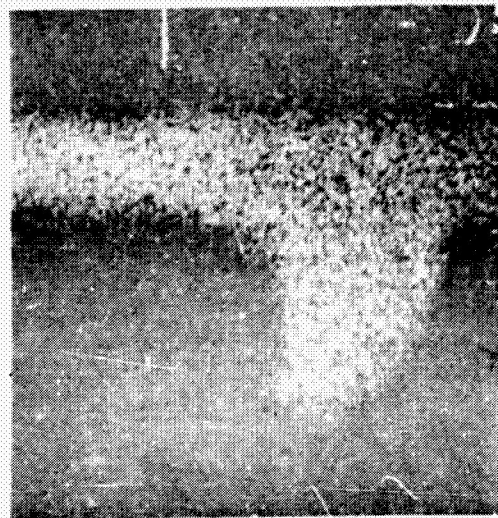


Figure 4-7—Area D of gold-molybdenum metallization before heat treatment, 130 x 130 microns. (a) Electron micrograph. (b) Gold L-alpha X-ray image. (c) Molybdenum K-alpha X-ray image.

A very surprising effect was observed when area B, shown in Figure 4-4 before heat treatment, was examined after 4 hours at 600° C. It was found that the four gold L-alpha and L-beta peaks did not appear in their usual places in the X-ray spectrum, but were shifted about 0.015 angstrom towards the longer wavelengths. In Figure 4-12, this shift can be seen by comparison of the spectrum of area B with that of the apparently unaffected area A very near it on the integrated circuit. The spectrum of area B is not only shifted, but is much lower in X-ray intensity. Efforts to explain this effect in terms of contamination or instrument error have not been successful, and the problem is still under investigation.

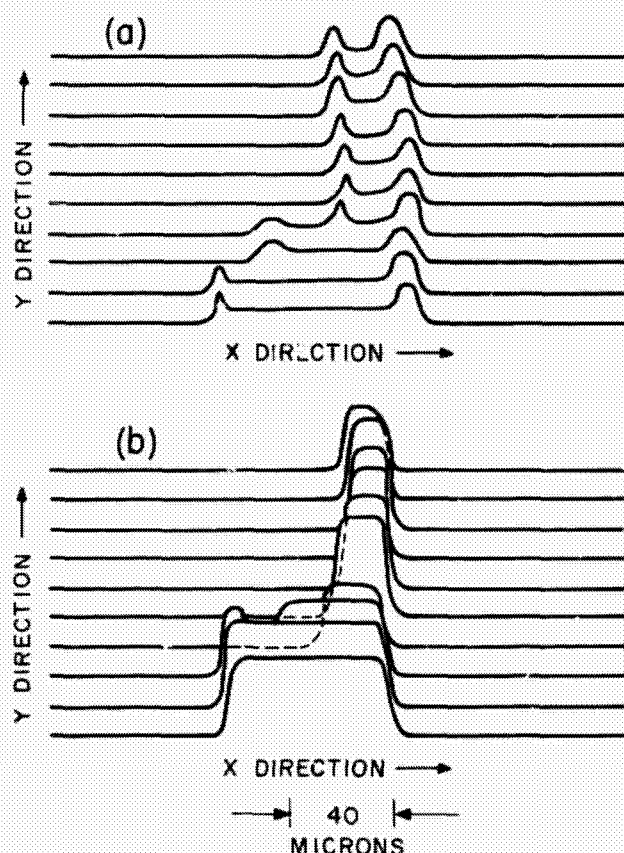


Figure 4-9—Contourograph of ten linear scans over gold-molybdenum metallization, with spacing of 7 microns between scans. (a) Molybdenum K-alpha scans. (b) Gold L-alpha scans.

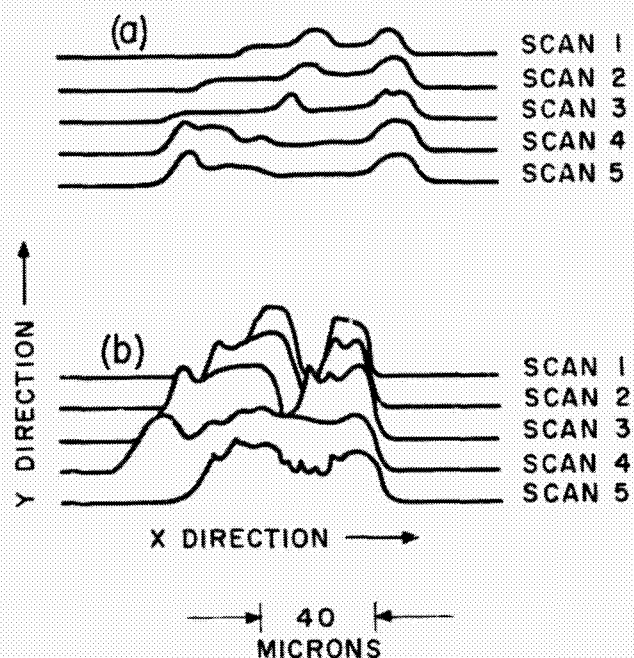


Figure 4-8—Contourograph of five linear scans over area D of gold-molybdenum metallization, with spacing of 10 microns between scans. (a) Molybdenum K-alpha scans. (b) Gold L-alpha scans.

Although wavelength shifts have previously been reported for aluminum K-alpha radiation from aluminum-nickel alloys, the magnitude of the effect observed for the gold L-line shift indicates approximately 25 times the energy change (approximately 100 to 150 electron-volts). Another region, area C, was found with a similar but smaller shift in wavelength. The positions of the gold L-beta lines for areas A, B and C are shown in Figure 4-13.

#### FUTURE RESEARCH PLANS

The investigation of X-ray wavelength shifts will be continued in an attempt to identify them with various types of compound formation. This effort may lead to a valuable tool for examining the microstructure of the metallization on integrated circuits. Back-reflection and transmission Kossel cameras, soon to be added

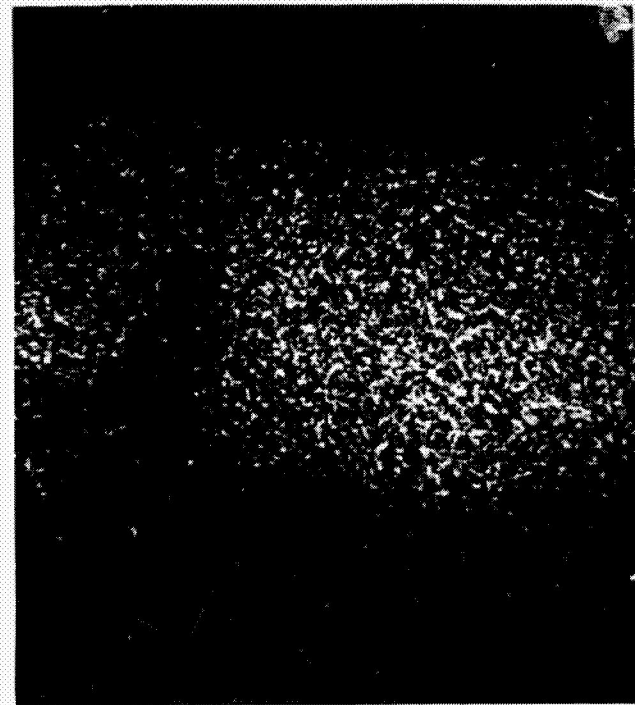
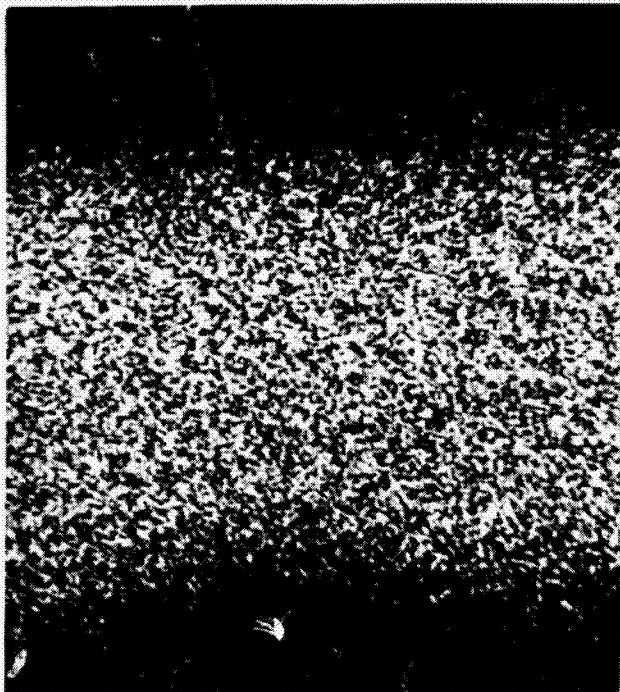
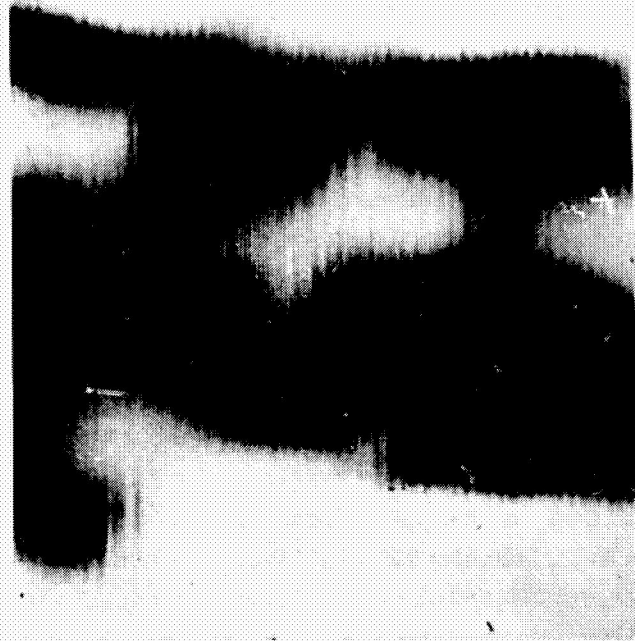


Figure 4-10—Area E of gold-molybdenum metallization before heat treatment, 22 x 22 microns. (a) Electron micrograph. (b) Gold L-alpha X-ray image.

Figure 4-11—Area E of gold-molybdenum metallization before heat treatment, 22 x 22 microns, after 600°C for 4 hours. (a) Electron micrograph. (b) Gold L-alpha X-ray image.

to the present electron probe equipment, will be used to study microscopic strains and stresses in monolithic circuits by X-ray microdiffraction techniques.

A hot-stage metallograph, now on order, will be used to study the structure and transformations of metals and alloys at elevated temperatures. The problems that will be investigated with this equipment include: grain nucleation and growth, phase transformations, corrosion and diffusion reactions, sintering phenomena, and plastic deformation and fracture.

A basic investigation of the reliable current-carrying capacity of integrated circuit metallization will be carried out on films deposited on oxidized silicon. The metallization will include aluminum, gold-molybdenum, gold-chromium, and other combinations being considered for practical integrated circuits. The effects of silicon oxide thickness, metal thickness, temperature, current density, and ambients on the metallization stability will be investigated.

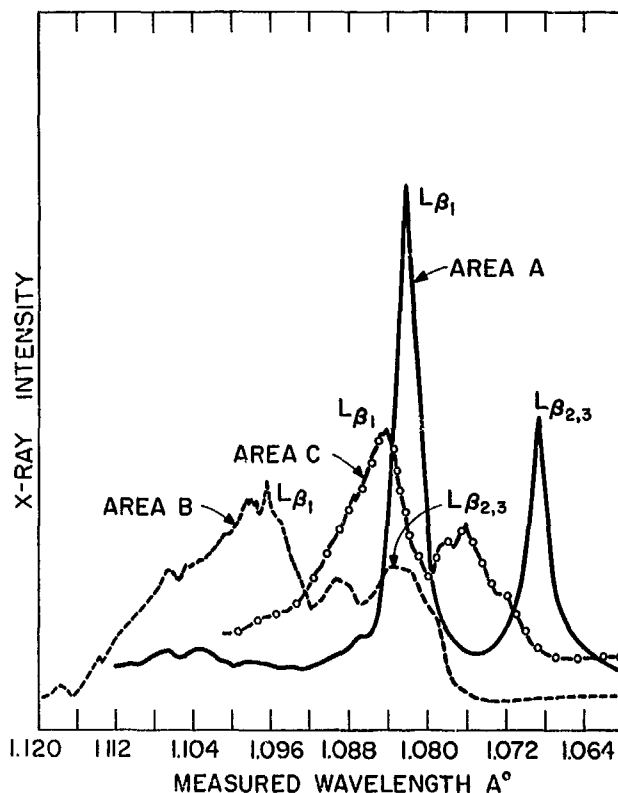


Figure 4-13—Comparison of positions of gold L-beta X-ray peaks. Area A is unaffected, area B shows a shift of .002 Angstrom, and area C a shift of .014 Angstrom.

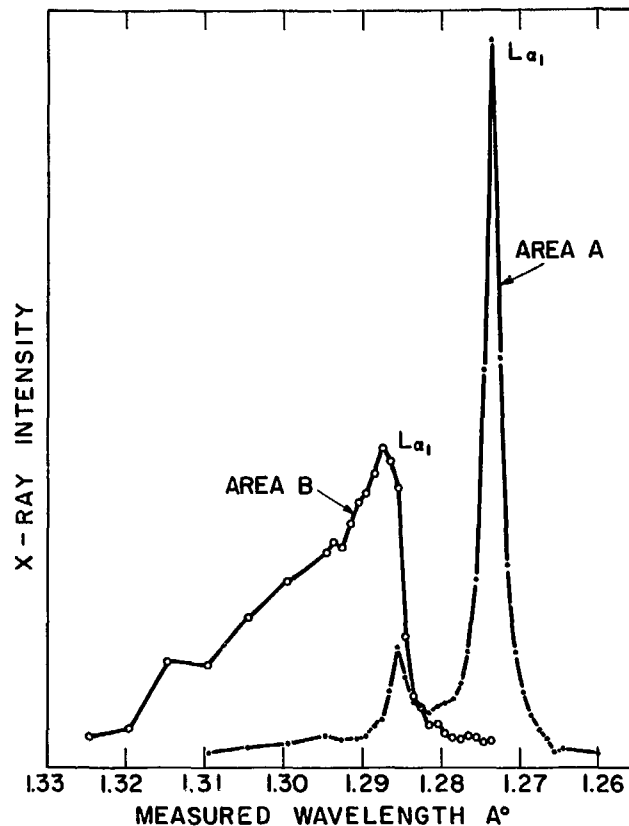


Figure 4-12—Comparison of position of gold L-alpha X-ray peaks. Peaks for area B is shifted .015 Angstrom from standard wavelength, while area A is unaffected.

#### ACKNOWLEDGEMENT

The writers wish to express their appreciation to S. Schwartz and J. Gerhard for their contributions to this investigation.

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## 5. FABRICATION OF SILICON DEVICES BY ION IMPLANTATION

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Techniques for forming controlled p-n junctions by implanting impurity atoms in silicon have been developed by Ion Physics Corporation for the fabrication of not only solar cells but bipolar and field effect devices as well. Not the least of the many inherent advantages is the elimination of the photoresist process. This process becomes unnecessary because the dopant is not impeded by the oxide coating over the silicon. The energy of the beam, which determines the implantation depth, can be varied in a manner to produce any desired junction profile. The particular work that forms the basis for this paper stems from Contract No. NAS8-20184 with Ion Physics Corporation (IPC). The effort under this contract has been directed toward focusing and controlling ion beams to achieve better resolutions than presently available in photoengraving processes. This is a first step toward the automating of integrated circuit fabrication.

### INTRODUCTION

Ever since the development of dendritic silicon, or silicon web, it has been the desire of semiconductor manufacturers to automate or computerize the process of fabricating transistors and integrated circuits. Silicon web can now be grown in widths of about 2 cm, with sufficient flexibility to be wound onto reels 1 to 2 meters in diameter. The web material could be fed through the various processing steps to produce the necessary junctions of the right geometry and then wound onto a takeup reel. The final step would be to dice the web and package the devices.

The technology that promises to make this system of integrated circuit fabrication feasible is called ion implantation. The current MSFC contract with IPC, a subsidiary of High Voltage Engineering Corporation, Burlington, Massachusetts, provides for preliminary work toward the goal of automatic transistor and integrated circuit fabrication using ion implantation. Specifically, the contract with IPC involves a study of the use of energy beams in the fabrication of semiconductor devices. Particular emphasis is placed on techniques to eliminate the several photoengraving steps now prevalent in the conventional planar process. Since beams can be controlled electronically, this system of fabrication should lend itself well to computer programming. Effort was directed toward carrying out as many of the operations as possible in the clean environment of a vacuum.



Under a recent extension of the contract, the scope of work has been expanded to include a demonstration of the feasibility of forming very sharp ion beams. The work is progressing satisfactorily and should result in ion beam spot sizes of approximately 0.25 micron. Another intent of the recent contract extension is to advance the state-of-the-art of ion beam technology by actually producing, by ion implantation, six sample three-input NOR gates for evaluation. It is hoped that superior lateral and vertical geometry control can be achieved through the use of beams, rather than conventional diffusion, for implanting the impurities. Effort will be directed toward minimum circuit size and power consumption. The active devices will be approximately 1 micron in size with a propagation delay of less than 1 nanosecond.

## ION BEAM DOPING

There are two distinct classes of direct dopant introduction into semiconductor materials by energetic ion beams: implantation and channeling. Implantation uses the known energy range relationship of ions in materials to obtain concentration profiles of any arbitrary form, up to the limiting energy of the particles available. Very high dopant concentrations can also be obtained. Concurrent radiation damage can be made an insignificant factor with the right procedures.

Channeling uses the property of some crystalline structures to allow ion penetration along certain preferred directions to a much greater depth than classical range/energy relationships permit. While this process permits greater doping depth for a given energy, the concentration profile is strictly limited, and not significantly different from, that obtained by diffusion. However, channeling cannot penetrate amorphous passivating oxide layers. Furthermore, channeling requires that the incident ions penetrate in a given direction (to within about  $\pm 1/2$  degree) to obtain significant penetration. In contrast, the implantation method is independent of the angle and unaffected by amorphous layers. For these reasons, it seems more attractive to employ the implantation technique rather than the channeling method.

## ION IMPLANTATION

Figure 5-1 shows the main components of the implantation apparatus currently being used. An electrostatic accelerator (50 to 400 kev) accelerates boron or phosphorus ions from an RF ion source to the energy level corresponding to the desired junction depth. The beam is then passed through an analyzing magnet to remove all impurities. This spectroscopically pure beam is scanned vertically and horizontally to a uniform cross section larger than the sample area (for large area devices). It finally strikes a silicon slice mounted in the target position. The silicon slice can be rotated continuously from a position normal to the beam to a position parallel to the beam. Since the ions have discrete ranges (Figure 5-2) independent of incident angle (no channeling), the distance  $x$  below the semiconductor surface at which the ions come to rest is determined by the angle  $\theta$ :



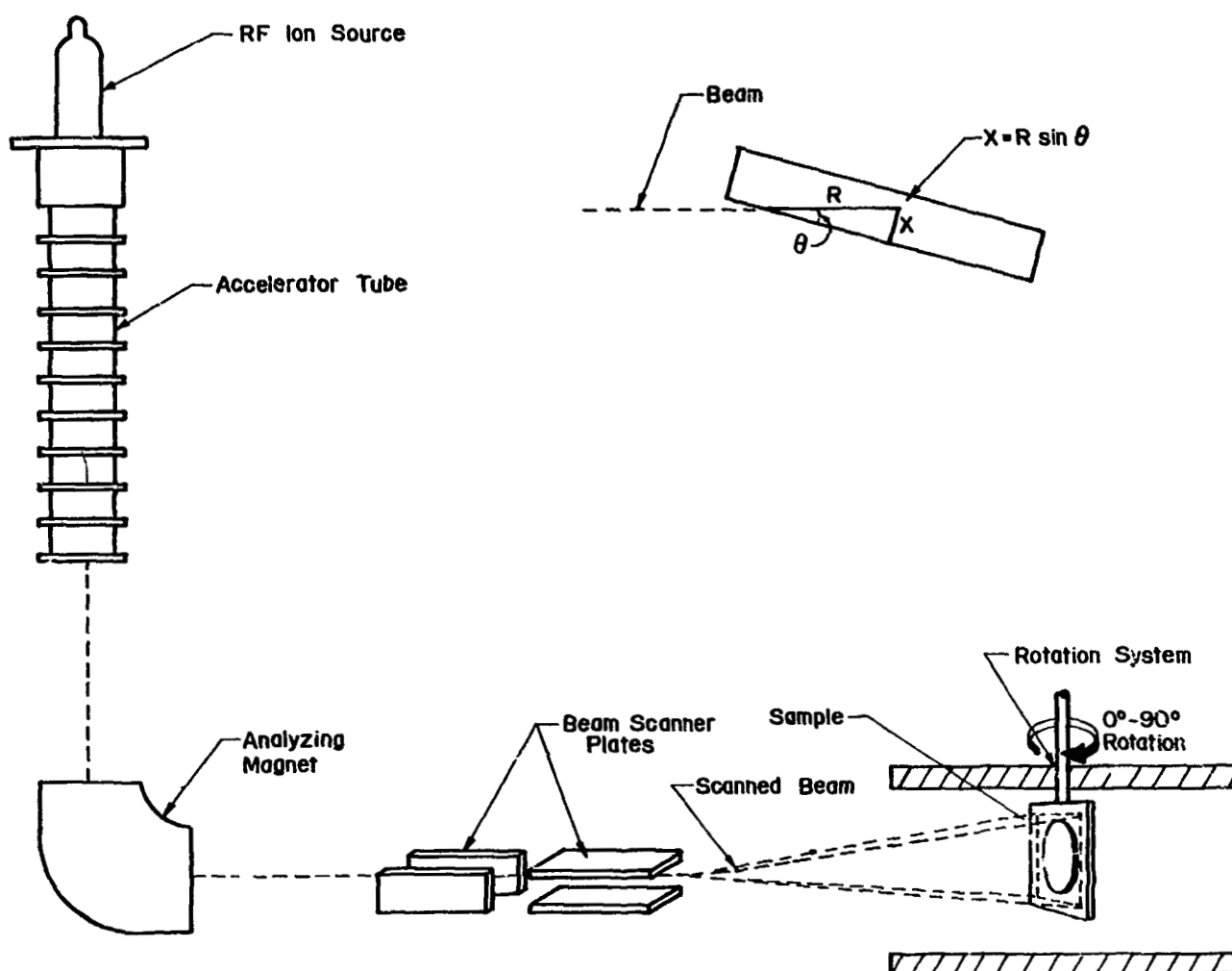


Figure 5-1—Implantation apparatus.

$$X = R_E \sin \theta,$$

where  $X$  = penetration depth perpendicular to the surface,

$R_E$  = range of the incident ions in silicon at incident energy  $E$  ( $2.15\mu$  for 1.5 Mev  $B^{11}$  ions),  
and

$\theta$  = angle between incident direction and silicon surface.

By rotating the sample continuously while the beam energy is held constant, a continuous implantation of ions is obtained from the surface to a depth corresponding to the maximum range. With constant beam current, the incident flux rate decreases as the angle between the incident direction and the cell surface decreases. A servo system is used to control the integrated flux at any given depth below the surface by controlling the speed of sample rotation. A variable program controlling the servo system is used to vary junction profiles by varying the concentration gradient.

An ideal ion implantation technique for the production of transistors and integrated circuits should exhibit the following characteristics:

1. Automatic operation; complete all process steps without manual handling; permit line changes with minimum complications; use continuous process material, such as silicon web.
2. No masking requirement.
3. Sufficient ion intensity range for formation of three-layer devices.
4. Accurate line resolution and control of junction geometry equaling or exceeding that provided by masking; control of base thickness to better than one micron for high frequency transistors.
5. Little or no interaction between different devices on one substrate. Primarily, this requires a technique in which the first junctions formed are unaffected by formation of later junctions.
6. Work through a passivating oxide or, conversely, complete all devices and surface-passivate them before their removal from the implantation chamber.
7. Capability of accelerating a variety of doping atoms for p and n type doping in silicon and for doping in III and V compounds. The capability to dope both classes of material helps to assure that the technique will not become obsolete with material advances.

The IPC implantation technique has been shown to satisfy criteria concerned with device fabrication by its successful use in the production of solar cells and radiation detectors. Not yet demonstrated are the beam control techniques required for the completely automatic process. The limited MSFC contract with IPC has been directed toward a demonstration of beam control, to show that ion implantation may be used to "write" complex devices with a highly resolved ion beam. The ultimate goal is resolution well beyond that possible with masking techniques.

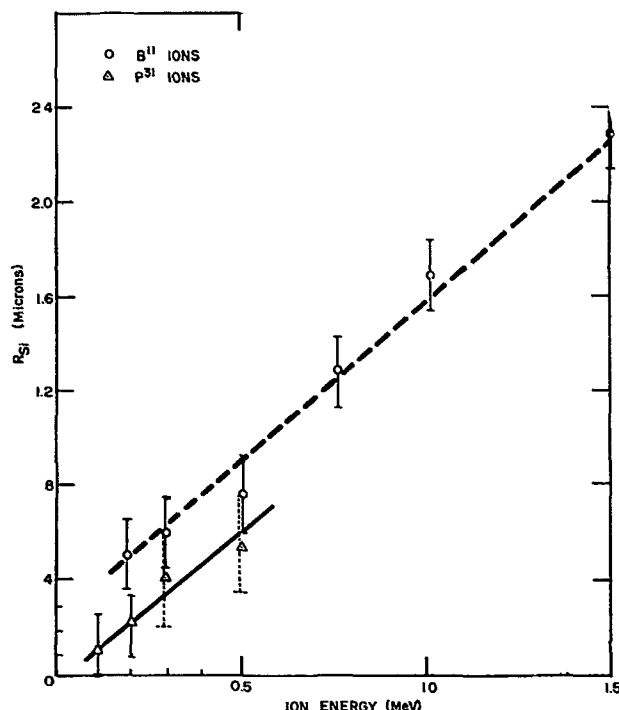


Figure 5-2—Range of boron and phosphorus ions in silicon.

## FORMATION OF OXIDE PASSIVATION LAYERS BY SPUTTERING

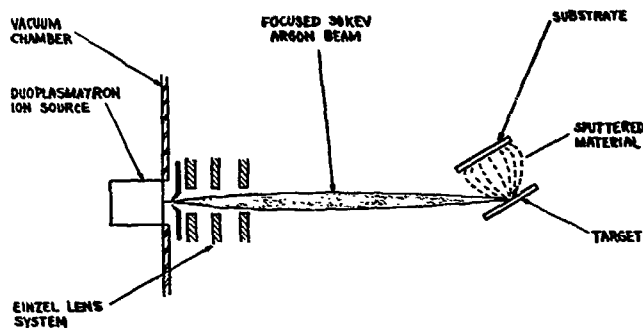


Figure 5-3—Sputtering apparatus.

A high vacuum method of applying oxide layers is needed to make the ion beam implantation technique complete in itself. This is accomplished as shown in Figure 5-3. The system consists of a refined duoplasmatron ion source and an electrostatic lens system giving a focused accelerated 30 keV argon beam. Oblique incidence of this beam on an appropriate target in the deposition chamber sputters target material onto a substrate mounted near and parallel to the target. Since the oxide in the implantation

process is used only for passivation and not for diffusion masking, thicknesses less than the conventional 5,000 to 10,000 Å may be used. In practice 1,000 Å has been found adequate. Implantations of boron or phosphorus may readily be made through this thickness.

## HIGH RESOLUTION IMPLANTATION TECHNIQUE

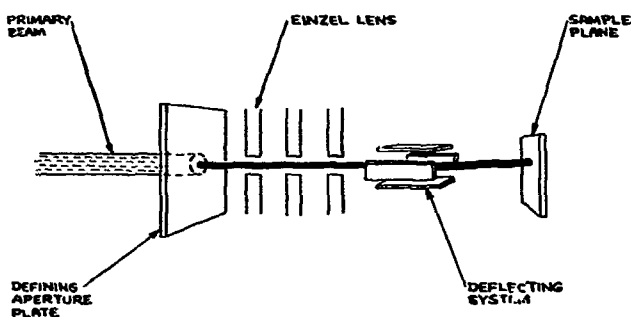


Figure 5-4—Basic high resolution implantation technique.

The technique being developed by IPC for generation of a high resolution implantation beam is shown in Figure 5-4. Basically, it involves insertion of a defining aperture before the deflection system shown in Figure 5-1. Future fabrication of many devices simultaneously on one sample plane will employ several apertures to develop an array of beams. With a nondivergent beam striking the aperture perpendicularly, the resulting beam would be, at worst, only slightly divergent with approximately

the same diameter as the aperture. An appropriate lens system focuses this beam on the sample plane. The beam is deflected by a scanning system to the appropriate spot or spots to be doped in the substrate. Penetration depth and concentration profile may be varied by programming ion energy rather than by rotating the sample, as previously described.

During the past nine months, work has progressed on a lens system and ion optical techniques compatible with an existing 400 keV accelerator and capable of resolution in the micron range. The basic design concept of the lens has been aimed at future versions capable of economic production of devices. The required type of lens was determined to be "strong focusing," since reasonably long focal lengths cannot be produced in cylindrical lenses without applying voltages comparable to the accelerating voltage. The strong focusing lens chosen was a three-element electrostatic quadrupole. An electrostatic lens was chosen, rather than an electromagnetic lens, because it

permits the use of various dopants without need for readjustment. It also avoids the problem of magnetic pole pieces which can locally saturate, thereby disturbing the field and increasing the aberrations of the lens. A 3-element lens with spaces equal to end electrode length  $L$  and center electrode length  $2L$  was chosen because it was believed to have the fewest aberrations of those lenses for which data are readily available.

A relatively large maximum aperture was chosen to give the lens reasonable versatility. The electrode spacing was set at one inch to permit experiments in which a multiple array of beams could be simultaneously deflected to produce multiple identical devices. The one-inch electrode spacing provides sufficient beam-electrode separation to prevent perturbation of the beam by electrode imperfections.

#### AUTOMATED HIGH RESOLUTION IMPLANTATION

Figure 5-5 shows how these techniques could be automated. The illustrated system is completely compatible with flexible silicon web, since the web material has the smooth surface required for the implantation process. Silicon slices could also be fed through the system on a rigid, indexed belt. Either approach allows completely automatic operation.

As shown in Figure 5-5, the silicon entering from the right is first subjected to argon beam sputtering to remove surface oxide and any surface contaminants. Next, the clean surface is passivated by application of a sputtered quartz layer. Implantations of boron and phosphorous are accomplished serially with one accelerator system by switching beams. Junction depth and

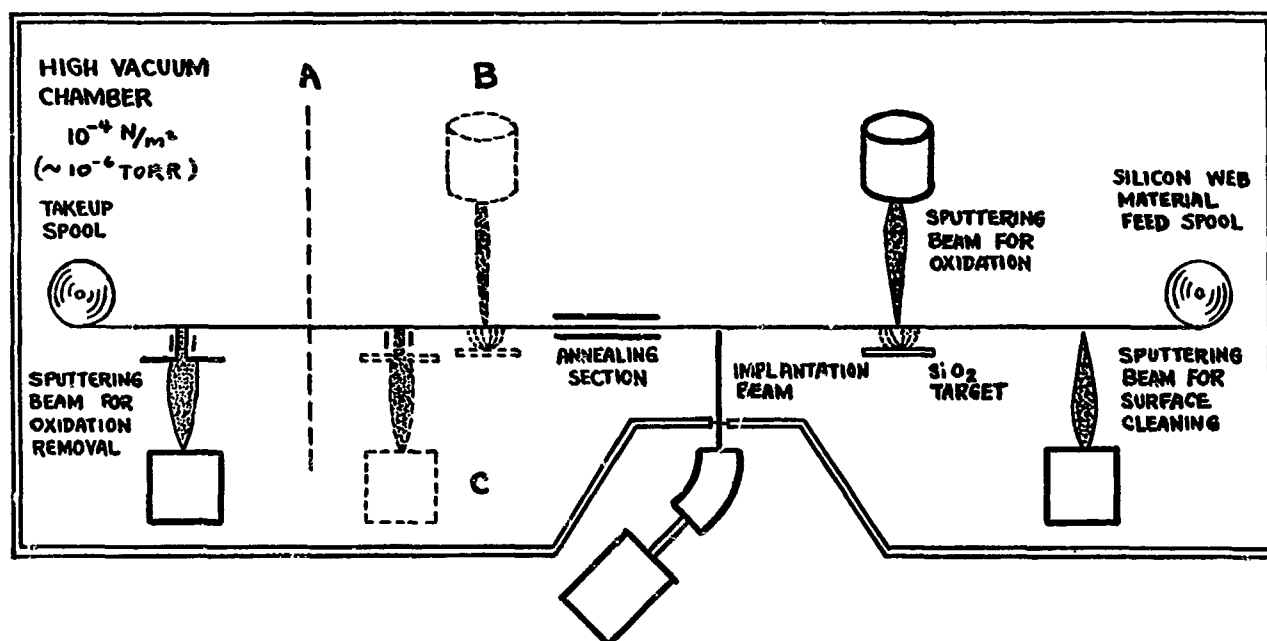


Figure 5-5—Automatic high resolution implantation technique.

geometry are controlled entirely by controlling beam characteristics. After heat treatment to anneal radiation damage, holes are sputtered through the oxide in appropriate spots for contacting, using a beam defining and deflecting technique. The material is then removed and diced. Finally, contacts are applied using photoresist masking techniques. A more sophisticated system would delay the sputtering of the passivating layer until position A, after the implantations are finished. Keeping in mind that the flow of work in Figure 5-5 is from right to left, contact material would be sputtered on the entire surface at position B and sputtered off, except in the contact areas, at position C. The final contact hole oxide removal would be performed following position A as shown. Thus, with the sole exception of final contacting outside of the manufacturing chamber, the entire fabrication process could be carried out in the clean environment of the vacuum chamber.

In conclusion, since the ion beam process is electrical, it is controllable by electronic and computer methods. Thus, automation, which is most difficult with the diffusion-masking method, can be readily applied to the ion beam process. The ion beam technique should make it possible to achieve doping profiles not possible with any other technique. The following advantages are foreseen for the ion beam process in the production of transistors and integrated circuits:

1. High yield and high reliability. Exposure to contamination is reduced to the vanishing point by exclusive use of high vacuum ambient.
2. Wide choice of materials. The process allows use of many substances which are not easily employed by current methods of device fabrication, but which have attractive properties for devices such as gallium arsenide transistors.
3. High productivity. All the steps in the fabrication process can be done in a short time, making possible high rates of manufacture.
4. Automation. About 90 percent of the process can be accomplished in one computer-controlled vacuum chamber.
5. More precise control of doping. Sharply focused beams and reduced diffusion should permit finer lateral resolution and base width, with reduced surface concentration variations.

Although the current IPC contract can only scratch the surface in the development of such an automated system, it is felt that the efforts to achieve high resolution ion beams will be applicable to whatever system might eventually emerge.

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## 6. THIN-FILM MICROCIRCUIT DEVELOPMENT AT MARSHALL SPACE FLIGHT CENTER

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To meet the need for smaller electronic circuitry as a means of reducing weight in space vehicles, a thin-film microcircuit program was initiated at Marshall Space Flight Center (MSFC) in 1960. A brief history of this program and progress on each task to date are discussed, including facilities and equipment requirements and cost. The levels of past and present technology at MSFC are compared. Microcircuit capabilities, tolerances, and limitations are enumerated; and new equipment, methods, and techniques are summarized briefly.

### INTRODUCTION

Vacuum-deposited, thin-film technology has early origins, dating from 1852 (Reference 1). The two methods of depositing thin solid films in a vacuum are evaporation and sputtering. The two basic processes for fabricating microcircuits using these methods are: the additive process whereby the circuit elements are vacuum evaporated onto the substrate in successive layers, or patterns, through a stencil mask which defines the shape of the element; and the subtractive process in which the entire surface of the substrate is covered with successive layers of thin films of different composition by evaporation or sputtering. These layers are selectively removed by photo-etching methods to define the circuit elements. This discussion is limited to the additive process, unless stated otherwise; and the term "thin film" as used here applies to vacuum evaporated thin films. It is assumed that the reader is conversant with the technology. Those desiring a more intimate knowledge of the subject are referred to Strong (Reference 1), and Holland (References 2 and 3) and the extensive bibliographies in their works.

Thin-film technology has wide applications in research on the properties of materials as well as extensive applications in industry, where it is used for decoration and for coating optical elements. It is a complex field which encompasses almost the entire spectrum of the physical sciences when applied to successful electronic circuitry. The use of thin-film technology as a tool in other research fields requires complete knowledge of the associated technologies to prevent costly errors of omission, which so often lead to false conclusions in research involving vacuum-deposited thin-films. The properties of these films are extremely sensitive to the conditions of formation. In brief, they are sensitive to the chamber pressure and the composition of residual gases; the

temperature and the composition of the source; composition, condition, and properties of the evaporant material; the cleanliness, structure, composition, and temperature of the substrate; the rate of film growth; and the thickness of the film. Failure to observe and record any of these conditions will, in most cases, lead to films of unknown properties, and hence to false assumptions where the results of investigations or electronic circuit performance hinges on the properties of such films.

Until 1960, most of the interest in microcircuits centered around the activities of the Diamond Ordnance Fuse Laboratory and the application of microcircuits to electronic fuses, such as the proximity fuse. Much of the industry effort in this direction was closely related to this activity (Reference 4). The advent of the guided missile and space vehicles enhanced this interest, and the technology which was developed in the fuse field was used extensively in the missile and space fields.

The application of thin-film technology to the production of electronic capacitors and resistors dates from the 1930's. Beginning around 1940 and during World War II, intensive effort was directed toward the development of thin-film nichrome resistors. By 1950, thin-film resistors and capacitors were standard electronic components. From 1950 to 1960, intense interest was generated in the possibility of making integrated thin-film circuits; by 1959, practically every electronics manufacturer had entered the field and had established a thin-film activity. On the surface, the process appeared simple and inexpensive and seemed to offer such huge bonuses in low cost and high production that it created a heavy demand for vacuum evaporation equipment. Large outlays were made for thin-film facilities and production equipment. In some cases, companies were soliciting circuit orders before facilities were complete. During this period some circuits of modest quality were produced, but they were expensive because of low yields and poor tolerances which required manual adjustment. These circuits were, in effect, hand-built circuits produced in a step-by-step process. A satisfactory, continuous, single-cycle process that would produce precision circuits without subsequent adjustment did not emerge. The overwhelming majority of circuit production efforts were unsuccessful.

By 1963, most thin-film facilities had been abandoned or drastically cut back to small research activities. The two major causes for this decline in activity were: the success achieved in development of monolithic semiconductor circuitry that promised to be the panacea for all of the problems of microcircuitry, and the difficulties encountered in thin-film circuit production. Disillusionment with the latter can be traced to three basic causes: lack of personnel experienced in the technology, underestimation of the problems of thin-film circuit production, and adoption of an unrealistic production philosophy. At the beginning of the interest in thin-film microcircuit technology, probably fewer than a dozen scientists in this country had adequate theoretical and practical knowledge backgrounds in thin films to properly evaluate the technology and its application in terms of production. When confronted with apparent insurmountable problems, many thin-film activities, starting with a sound single-cycle production plan, shifted to a multicycle plan with post-deposition adjustment of components in search of a short cut. This led to cost and other problems just as difficult as those originally encountered.



At present the focus of interest in microcircuit technology has gone the full cycle. Monolithic semiconductor circuit technology has suffered from the same disillusionment that beset thin-film technology, but to a lesser extent. All microcircuit technologies have theoretical, practical, or economic limitations. Monolithic circuit technology is the best process for production of microcircuits, within its limitations. Monolithic microcircuits are limited in the related functional areas of voltage, noise, parasitics, power, speed, precision, and temperature stability. Design latitude is further limited by the range of component values and types and the lack of isolation between elements. Thin-film circuits also have limitations but can exceed monolithic circuit limits in all of these areas. Monolithic circuits are cheaper than thin-film circuits, within their functional and design limits, in large quantities. On the other hand, the thin-film circuits are economical in lots of a few thousand or less because of the great difference in the design, tooling, and capital costs. Interest is being revived in thin-film technology because it can fill requirements that cannot be met by the monolithic and other technologies.

#### HISTORY OF MSFC THIN-FILM MICROCIRCUIT PROGRAM

In 1960, a thin-film microcircuit development program was initiated at MSFC. This program was motivated by the need for smaller electronic circuitry to reduce the weight of space vehicles. This program began with exploratory investigations to determine the status of the technology and the feasibility of producing thin-film circuits that could meet the requirements of space vehicles. These investigations were continued through 1961 and determined that precision thin-film circuits for prototype use could be produced. The production philosophy adopted at this laboratory is that the realization of the full potential of thin-film technology in microcircuit production depends upon the development of a continuous single-cycle process which will produce microcircuits within desired tolerances without subsequent operations. It was further determined that the evaporation process was the only process that could meet this requirement and economically produce high quality thin-film circuits in a continuous process. It was realized that the difficulties inherent in the process were greater than those encountered in other processes and would probably delay circuit production a year or more; however, the advantages appeared to outweigh the disadvantages.

The most significant objection to the evaporation process has been the high cost of masks. This objection cannot be sustained under a thorough cost analysis which reveals that over 90 percent of the cost of the mask is in the artwork. There is little significant difference in the costs of the artwork in any of the microcircuit production methods, including printed wiring, if one considers the art cost per circuit function.

#### THIN-FILM PROCESS DEVELOPMENT PROGRAM OUTLINE

The main objective of this program is the development of an integrated continuous process for depositing thin-film electronic circuits. Each operation and step in the process will be continuously reviewed to determine its effect on the circuit, especially those operations in the evaporation cycle.

Evaporation conditions and techniques that influence the properties of the films, such as the properties, condition and composition of the evaporation material; evaporation temperature; condition, and cleanliness; and rate of film growth will be continuously monitored. Special investigations will be initiated to determine the best evaporation conditions for each evaporant used. The deposition process was analyzed, and specific areas needing further development or improvement were defined into the following projects:

1. **Development of Evaporation Sources.** There is a need to develop evaporation sources that will give longer continuous operation without replacement; will emit vapors at a uniform rate without explosive discharge of solid particles and loss of charge, and will give better directional distribution of the evaporant. This development will lead to greater economy in source replacement cost of the evaporant and will reduce damage to the substrate.
2. **Development of More Suitable Dielectrics.** All of the dielectric materials currently used in thin-film circuitry have undesirable characteristics either in performance or in circuit fabrication. The aim of this task is to examine the many dielectric materials and find a more suitable material or combination of materials.
3. **Development of Thin-Film Resistors.** The present state-of-the-art allows the deposition of low-value resistors of good stability with relative ease; however, higher value resistors of comparable stability are difficult to deposit. The purpose of this task is to develop higher value resistors with high tolerances and stability.
4. **Development of Conductor Materials.** The deposition of thin-film conductors presents no difficult problems; however, the adhesion, conductivity, and cost of conductors could be improved.
5. **Development of Interconnection Methods for Thin-Film Circuits.** The objective of this task is to simplify and improve present methods of intracircuit and interconnecting thin-film circuits.
6. **Development of Masking Techniques.** The purpose of this task is to simplify present methods of mask making. Making precision masks for resistors will be the primary objective. Other masks present no serious problem at this time.
7. **Development of Interim Methods for Use in Hybrid Circuits.** All suitable methods and techniques of circuit fabrication will be explored while thin-film methods and devices are under development.
8. **Improvement of Cleaning Methods.** This task is the simplification and improvement of methods for cleaning thin-film elements and materials to assure uniform results.

9. **Development of Substrate Materials.** The purpose of this task is to develop substrate materials for thin-film circuitry which are compatible with the thin films and the circuitry operating environment.
10. **Development of Suitable Thin-Film Capacitors.** This task is to develop a process that will yield high quality capacitors consistently and accurately.
11. **Development of Thin-Film Induction Devices.** In the past, the lack of good induction devices has imposed severe limitations on the design and performance of thin-film circuits. Efforts will be made to develop induction devices of such quality and capacity that this limitation may be removed.
12. **Development of Methods to Measure Thin-Film Thickness.** The quality and the capacity of thin-film capacitors is governed by the ability to deposit dielectric films of precise thickness. The purpose of this task is to improve the accuracy of film thickness measurements.
13. **Development of Uniform Methods of Testing Thin-Film Adhesion.** A method of measuring film adhesion that can be used to compare the relative adhesion of various thin films is needed.
14. **Development of Equipment, Controls, Processes, and Monitoring Devices for the Thin-Film Process.** The purpose of this task is the improvement of thin-film reproducibility by development of equipment and process controls that will allow the deposition of thin films under standard conditions and the development of monitoring equipment to monitor the process.
15. **Development of a Package for Thin-Film Circuits.** One of the most troublesome problems encountered in thin-film microcircuit fabrication is providing good mechanical support for, and a means of connecting, the circuits to the outside. The purpose of this task is to develop packages that will alleviate this difficulty.

## **EQUIPMENT AND FACILITY REQUIREMENTS**

The requirement for microcircuits as MSFC was surveyed, and it was determined that most circuits needs would fall into the category of custom circuits in prototype quantities of less than 100 except for digital applications, which in most cases would be best met by the use of semiconductor monolithic circuits. It was estimated that specialized production equipment costs, excluding instruments for general use, should not exceed \$50,000. Facility requirements could be met with 600 to 1000 square feet of white room facility. A clean room facility was considered highly desirable but not necessary if a reduction in yield could be tolerated. Experience to date supports these original estimates of cost and space since they do fall within the estimated cost. The

evaporation process centers around mask definition of the circuit, this being the most important part of the deposition apparatus.

### Mask Production

An analysis of mask production and costs disclosed that high quality masks can be bought cheaper than they can be made in-house. It is not feasible to produce high quality masks in-house unless the photographic, arts, and chemical facility cost, can be shared by other production operations. Furthermore, this is a highly specialized technology not easily mastered.

This analysis led to the decision to purchase masks at a cost of \$400 to \$1000 per master circuit. This results in a tooling cost of from \$4 to \$10 per substrate, without active devices, for

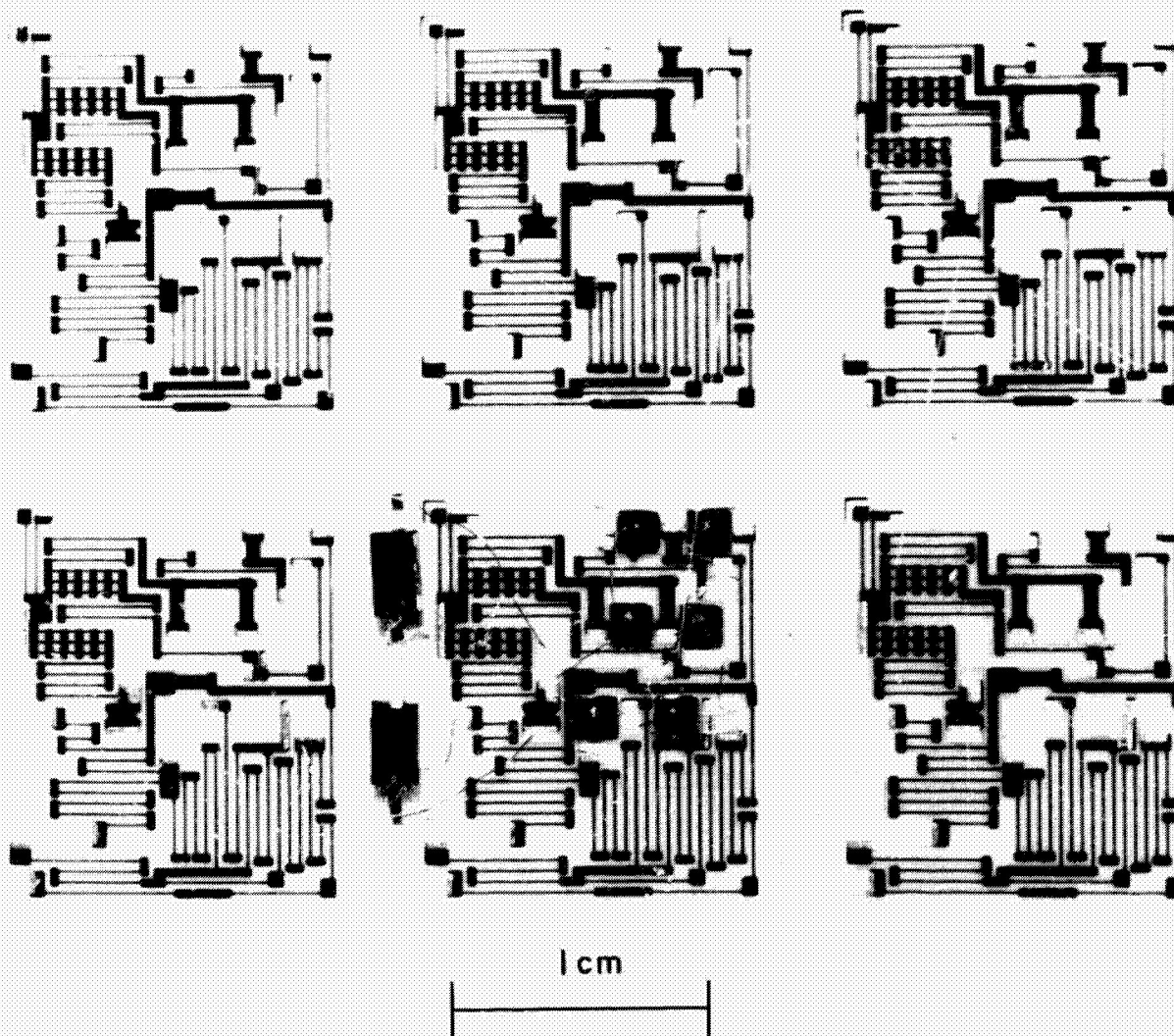


Figure 6-1—Substrate with six amplifier circuits deposited.

a run of 100 substrates. Individual circuit cost is further reduced in cases where multiple circuits are deposited on a single substrate, as shown in Figure 6-1.

Based on the current technology the following tentative production capability and tolerance standards were established in 1962 as a starting point.

#### Component Dimensions, Limitations, and Tolerances

##### Conductors: Copper, Gold, or Aluminum

- a. Minimum width -- 0.75 mm
- b. Minimum spacing -- 0.75 mm
- c. Current capacity -- approximately 75 ma/mm

##### Resistors: Nichrome

- a. Sheet Resistivity -- 300 ohms/sq
- b. Tolerance --  $\pm 10$  percent normal
- c. Temperature coefficient -- 60 ppm
- d. Power dissipation -- 0.5 watts/cm<sup>2</sup> of total resistive area
- e. Operating temperature -- -55 to +200 °C
- f. Minimum width -- 0.25 mm
- g. Maximum length -- 12.5 mm
- i. Minimum spacing -- 0.75 mm

##### Capacitors: SiO-Aluminum

- a. Maximum capacitance -- 1600 pf/cm<sup>2</sup>
- b. Tolerance --  $\pm 20$  percent
- c. PWV -- 35V

In 1963 it was found that the results of studies at this laboratory and the current state-of-the-art were in substantial agreement with procedures and design guidelines adopted by the U.S. Naval Avionics Facility, Indianapolis, Indiana, in proposed NAFI-TR-132. These design guidelines were adopted at this laboratory with modifications.

#### PRESENT STATUS OF THIN-FILM MICROCIRCUIT DEVELOPMENT PROGRAM

Precision thin-film circuits of high reliability can be fabricated and hermetically packaged at MSFC. Thin-film circuits (not assembled and packaged) can be produced at a rate of 24 circuits per hour at dimensions, tolerances, and limitations shown below and improved as follows:

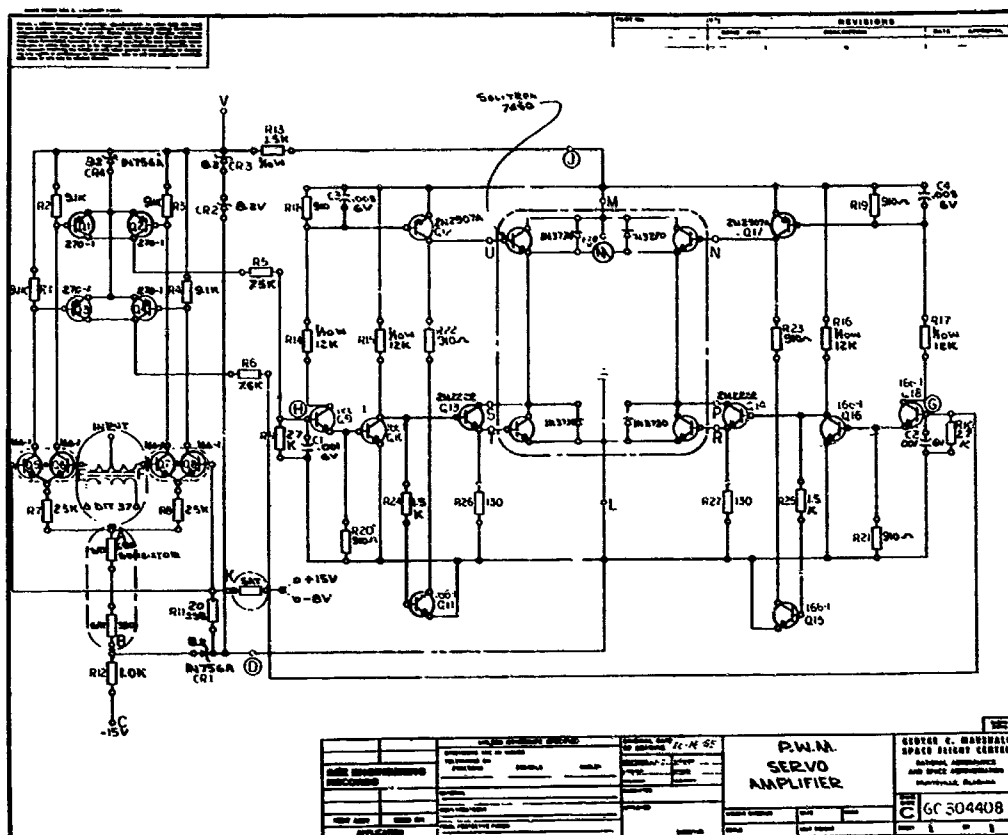


Figure 6-2—Electrical schematic servo amplifier.

1. All formal dimensions, tolerances, and limitations except those which apply to resistors and capacitors have been removed since they are governed by the voltages, currents, and power requirements of the individual circuit. Experience shows that the capabilities at this laboratory can exceed any reasonable requirements of transistor circuits, in general, except power dissipation. The servoamplifier circuit shown in Figures 6-2, 6-3, and 6-4 is an example of the power handling capabilities of thin-film circuits produced at MSFC. The circuit in Figure 6-2 is shown packaged in two stages in Figures 6-3 and 6-4. This amplifier has an output of 75 watts operating on 28 volts dc and has a power dissipation of about 2 watts at full output. A minor modification of two resistors allows the circuit to operate on 56 volts dc with a power output of 250 watts and maximum power dissipation of 5 watts. The four power transistors (inset Figure 6-2) are mounted in the circuit package for 28-volt operation. For 56-volt operation, the power transistors are mounted in a separate 1 by 1 cm flatpack on a heat sink. In those cases where power dissipation becomes a serious problem, it has been found that it is illogical to design for microcircuitry in the first place.
2. Resistor tolerances have been improved as follows:

Material: Nichrome (80/20)  
Sheet resistance: 500 ohms/sq



Tolerance:  $\pm 5$  percent standard - 1 percent special \*  
TCR: 30 PPM/ $^{\circ}$ C standard - 10 PPM/ $^{\circ}$ C special  
Minimum width: 0.1 mm standard - 0.05 mm special  
Aging change: less than 1 percent  
Other specifications not changed.

3. Capacitor tolerances have been improved as follows:

Maximum capacitance: 0.16 mf/cm (minimum voltage 10 volts)  
PWV maximum: 56 volts  
Other specifications not changed.

\*When special tolerances are required, there is a corresponding reduction in the production yield of good circuits.

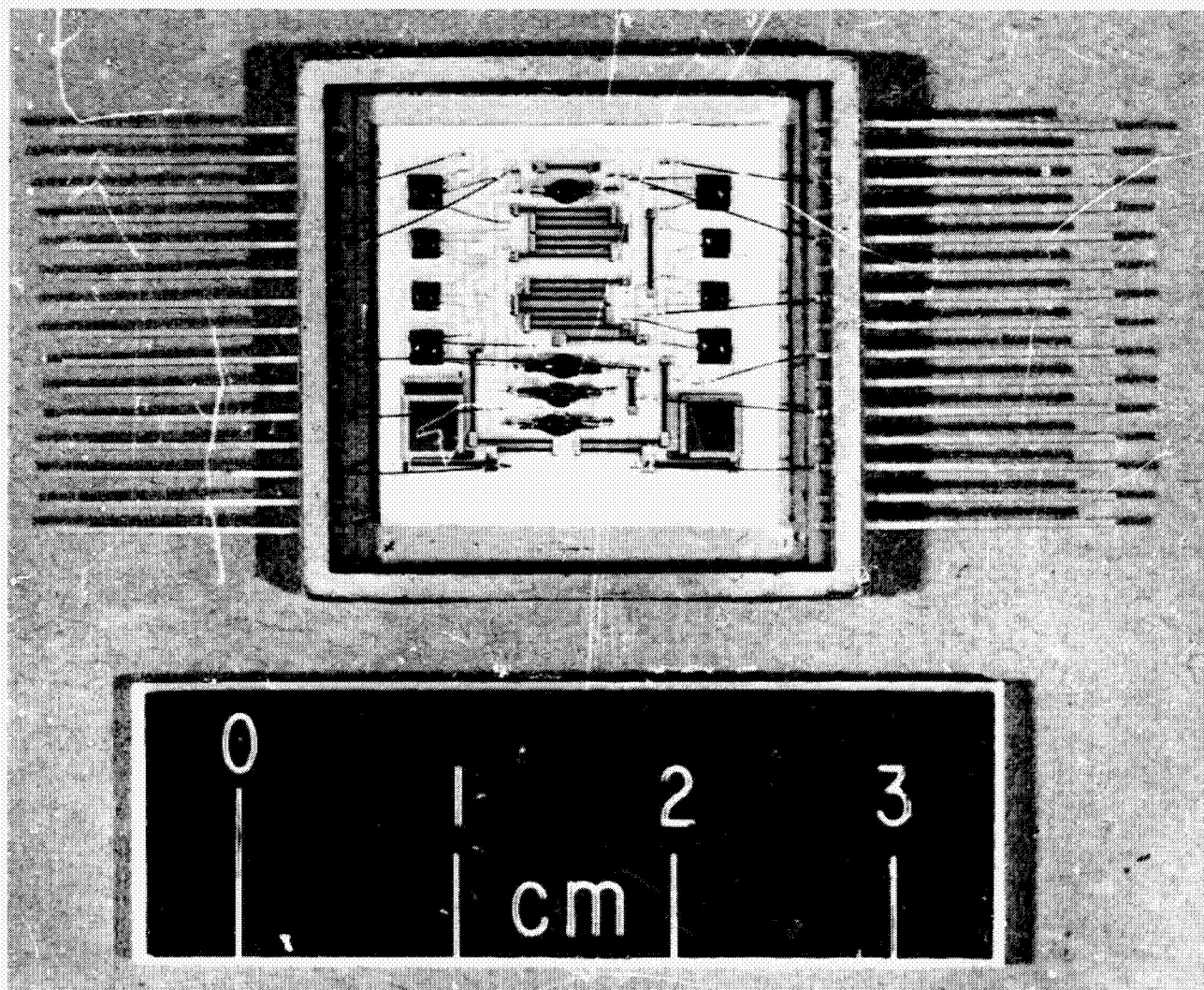


Figure 6-3—Amplifier stage, servo amplifier.

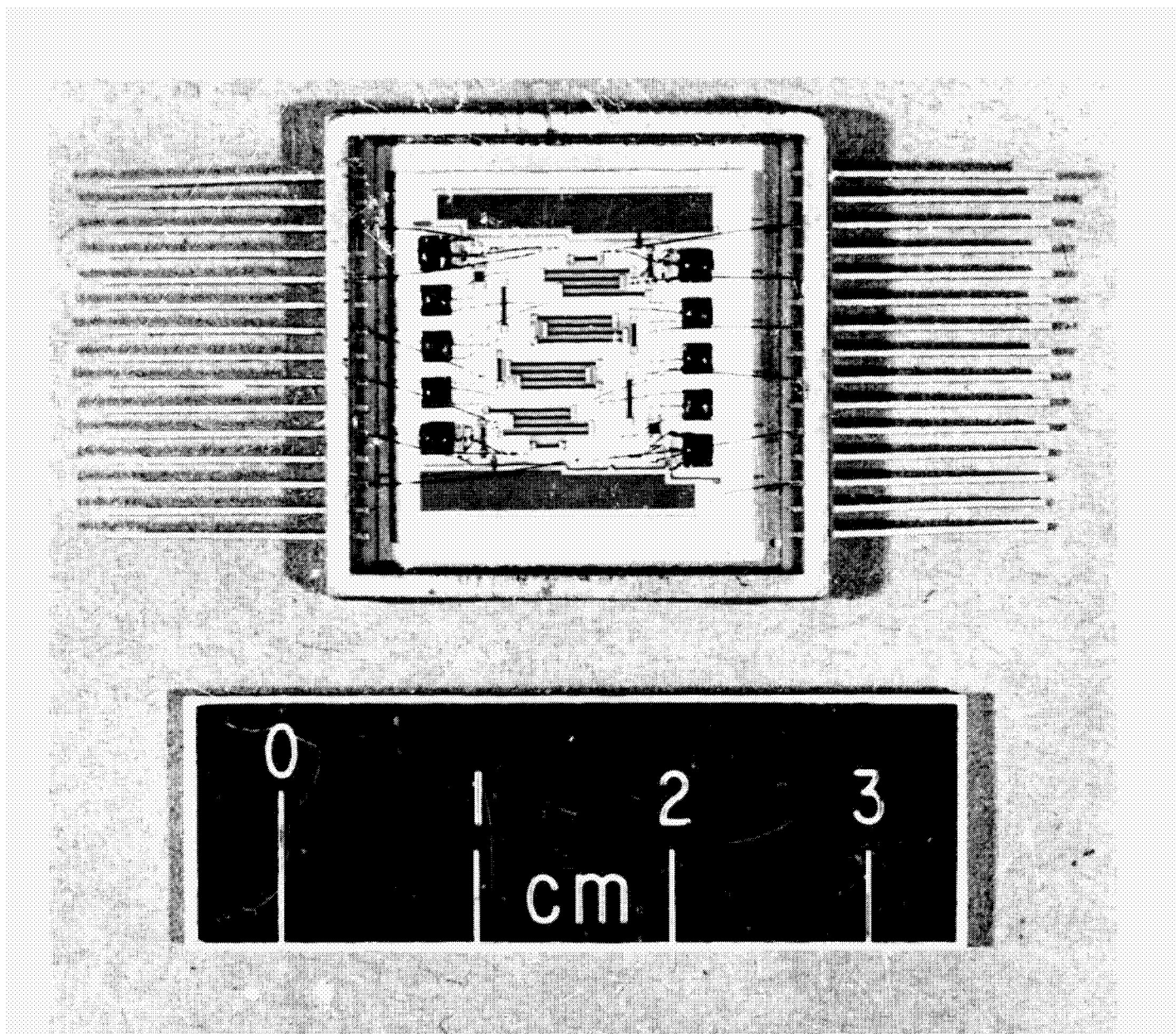


Figure 6-4—Power stage, servo amplifier.

#### Progress on Specific Development Projects

1. **Development of Evaporation Sources.** A series of improved evaporation sources have been developed in-house and placed in use. Two of the most significant sources are high capacity spatterproof sources (Reference 8) which are simple to fabricate and have a dual purpose. They may be used as bake-out ovens for the evaporant. After bake-out, the material may be evaporated without removal from the chamber. In addition, a broad line of commercial sources have become available, including boron nitride and its inter-metallics.



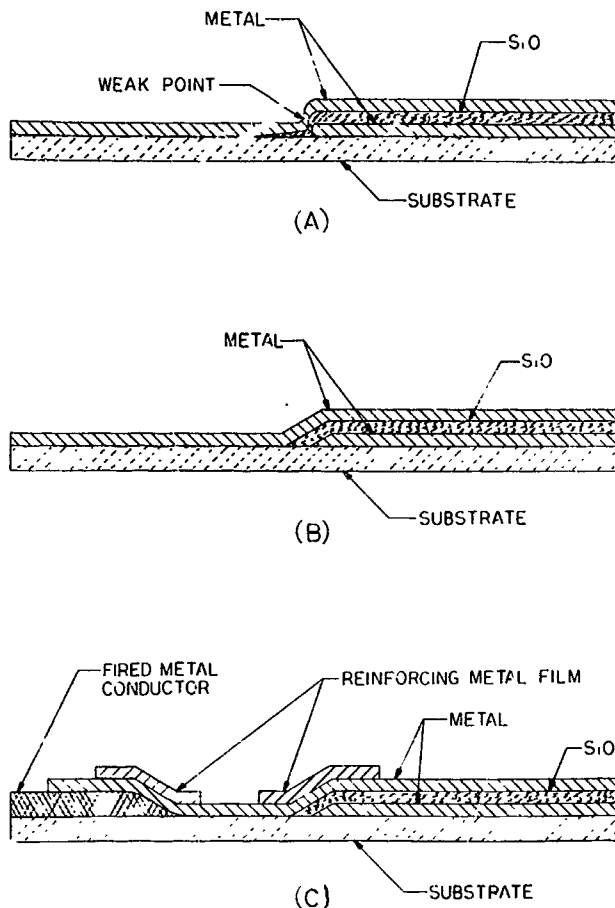


Figure 6-5—Thin-film connection.

2. **Development of More Suitable Dielectrics.** Some progress has been made under Contract NAS 8-20061, "A Study of the Properties of Dielectrics," at Auburn University. Work has been done in-house on a number of dielectrics; the more significant, in addition to silicon monoxide, are cerium oxide, magnesium fluoride, titanium dioxide, and tantalum pentoxide. Each of these materials has shown distinct promise as a dielectric material; however, the materials have not been used in the production of circuits because enough work has not been done on some of them to establish the best deposition methods. On others, the difficulty of depositing them properly is not compatible with production methods.
3. **Development of Thin-Film Resistors.** This task is less important as a result a reduction of resistor width to 0.1 mm standard and the capability of reducing it to 0.5 mm in special cases. In addition, in-house improvement of nichrome sheet resistance to 500 ohms/sq has enabled us to meet more than 90 percent of all resistor requirements with nichrome. In-house improvement of resistor characteristics is presented in Reference 9. In addition, work is being performed under contract NAS 8-20072, "A Study to Improve Thin Film Resistors," at the Georgia Institute of Technology. Some progress has been reported on this contract.
4. **Development of Conductor Materials.** Conductor lines and connection pads are being predeposited onto the substrate by the silk-screen process and subsequently fired in. This is an economical and accurate method of depositing conductors. This method is used where an accuracy of  $\pm 0.05$  mm is sufficient. Where greater accuracies are required, the conductors are vacuum deposited. The silk-screened conductors are used where high current conduction and adhesion is needed. An in-house investigation is being conducted to develop a method of diffusing thin films into the substrate to enhance adhesion. Good results have been achieved, but the methods used are not presently compatible with the production process.
5. **Development of Interconnection Methods for Thin-Film Circuits.** Intra-circuit connection of thin-film components and elements has been solved satisfactorily by the method shown in Figure 6-5. (A indicates the weak point at thin-film connections; B shows alleviation

of this condition by the shadowing technique; and C shows the method developed to eliminate the above condition and the difficulty in making connections to fired silver pads) (Reference 5). This connection is made by first selecting and adjusting the viscosity of the silver ink so that the silver will flow to a feather edge when fired and, second, vacuum depositing the high conductivity film over the connection joint. The fired silver pads are used as weld pads at all points where wire connections are needed in the circuit. This ink must be selected for its welding qualities.

Microbond welding has been developed for connecting to thin-film circuits. This process is described in Reference 10. Ultrasonic bonding has also been successfully tested and material combinations are being developed for applications in thin-film circuits. The active metal and the molybdenum methods of ceramic metallizing show great promise of replacing organic firing inks, which create problems in substrate cleaning.

6. Development of Masking Techniques. Mask development has been successfully completed under contract and ultra-high precision masks may be purchased at a reasonable cost.
7. Development of Interim Methods for Use in Hybrid Circuits. Development work under this task has led to the development of the planar gap welded circuit described in Reference 10. In addition, the in-house capability for fabricating silk-screened circuits has been established.
8. Improvement of Cleaning Methods. An excellent cleaning process has been developed as outlined in Appendix 1.
9. Development of Substrate Materials. Suitable substrates in the form of glazed ceramic and fine surfaced glass have been developed commercially. There is room for improvement, and this task is continuing.
10. Development of Improved Thin-Film Capacitors. Intensive efforts have been directed toward this task in-house and out-of-house. Capacitors have been greatly improved in-house by refinement of techniques and processes as indicated in capabilities above. In addition, progress has been made toward a better understanding of the breakdown mechanism in thin-film capacitors. Some significant in-house findings are being prepared for publication. Valuable information has been gained as a result of Contract NAS 8-11279 at Auburn University "A Study of the Failure Mechanism in Thin Film Capacitors"; this final report is in preparation. Contract NAS 8-20061 previously mentioned at Auburn University is also providing valuable information.
11. Development of Thin-Film Induction Devices. A major breakthrough has been made in this area by the development of an apparatus (Figure 6-6) which will deposit induction devices to several millihenries. The apparatus can be used to deposit tapped transformers and complete LC circuits in a single device. This apparatus is described in Reference 11.

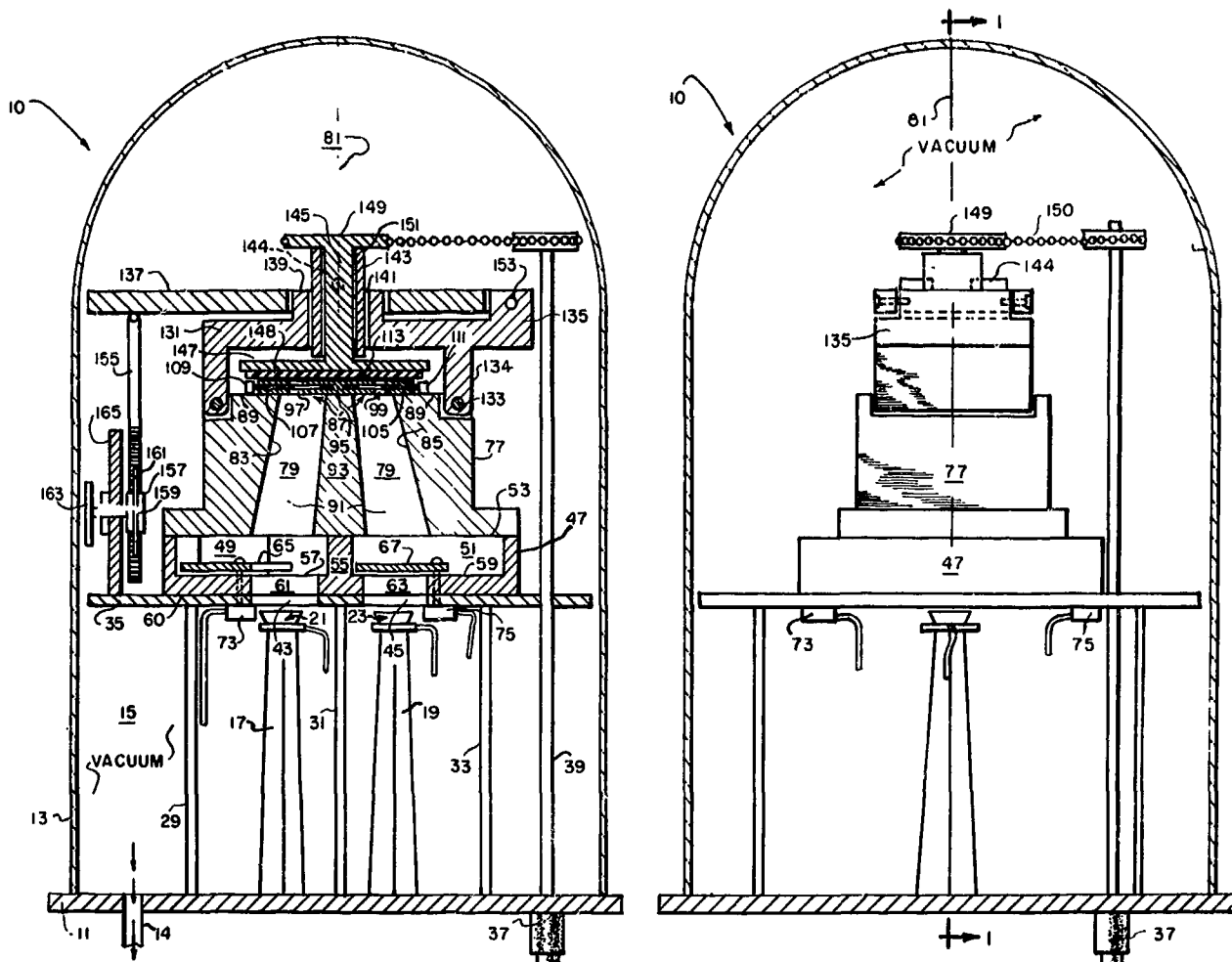


Figure 6-6—Thin-film inductor deposition apparatus.

12. **Development of Methods to Measure Thin-Film Thicknesses.** Little progress has been made on this task except by refinements of techniques. Static measurements are currently being made with a crystal oscillator with a capability of measuring to an accuracy of  $\pm 2$  atomic layers of gold equivalent, or by use of the Tolansky method with an accuracy of  $\pm 35$  angstroms. Dynamic measurements during deposition are accurate to about  $\pm 10$  atomic layers of gold equivalent.
13. **Development of a Uniform Method of Testing Thin-Film Adhesion.** No progress has been made on this difficult task.
14. **Development of Equipment, Processes, Controls, and Monitoring Devices for the Thin-Film Process.** A precision resistance monitoring bridge was built to monitor resistance during deposition. This device has an accuracy of  $\pm 1$  percent and could be preset to automatically monitor resistance and close the shutter at the proper value. This device was abandoned in favor of a digital ohmmeter with a preset function which is simpler to operate and has an accuracy of  $\pm 0.01$  percent (Figure 6-7 left). Thickness and rate monitoring

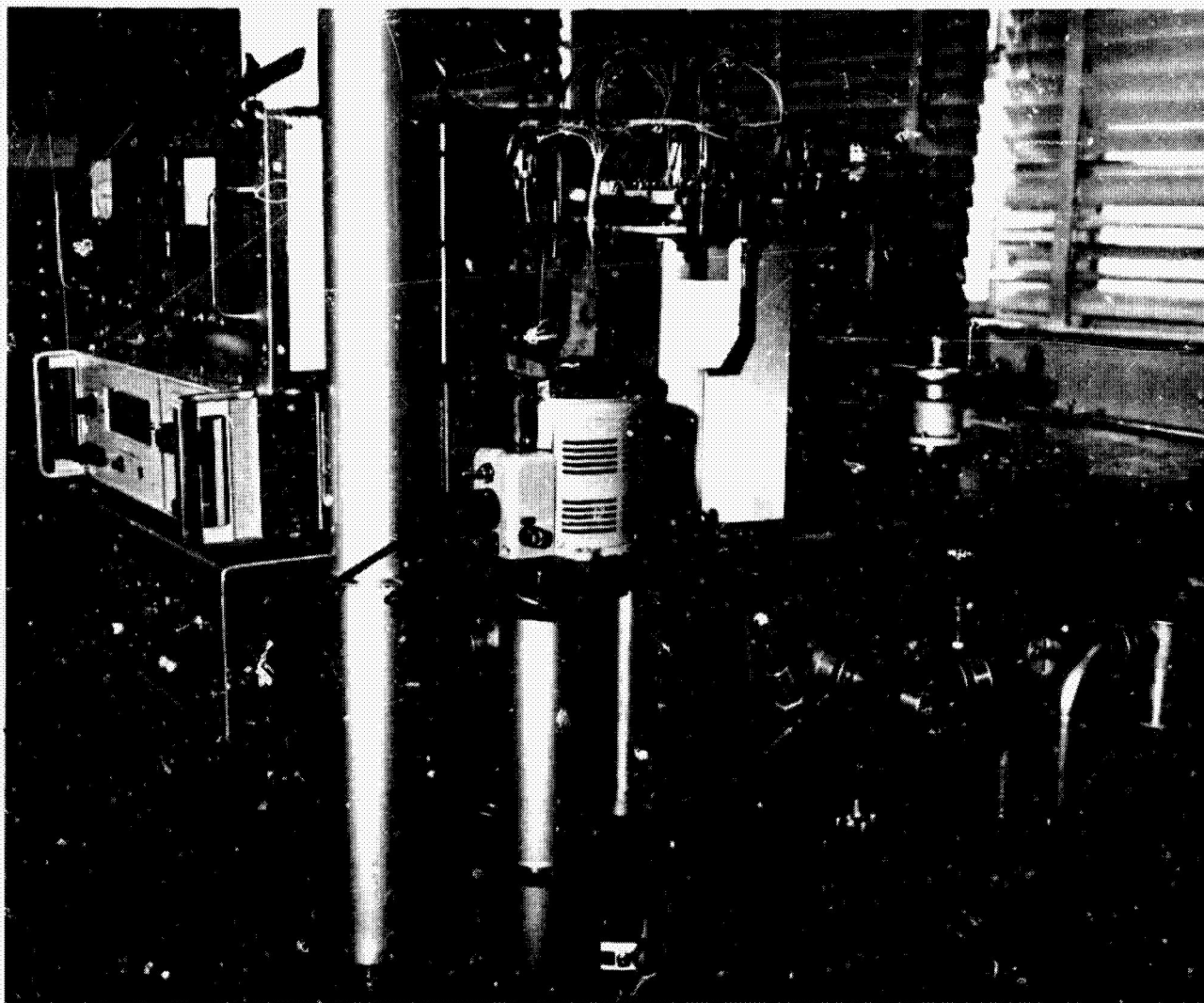


Figure 6-7—Thin-film microcircuit deposition system.

are performed by a Sloan crystal monitor (Figure 6-7 left) which has proven satisfactory.

A new thin-film microcircuit deposition unit (Reference 12) has been developed and built (Figure 6-7). This unit has been production tested and is currently in use.

15. Development of a Package for Thin-Film Microcircuits. The package shown in Figure 6-8 has been under development in-house; however, this effort has been abandoned since simultaneous development commercially has yielded the package shown in Figures 6-2 and 6-3 which is presently available. This package has been adopted as a tentative standard.

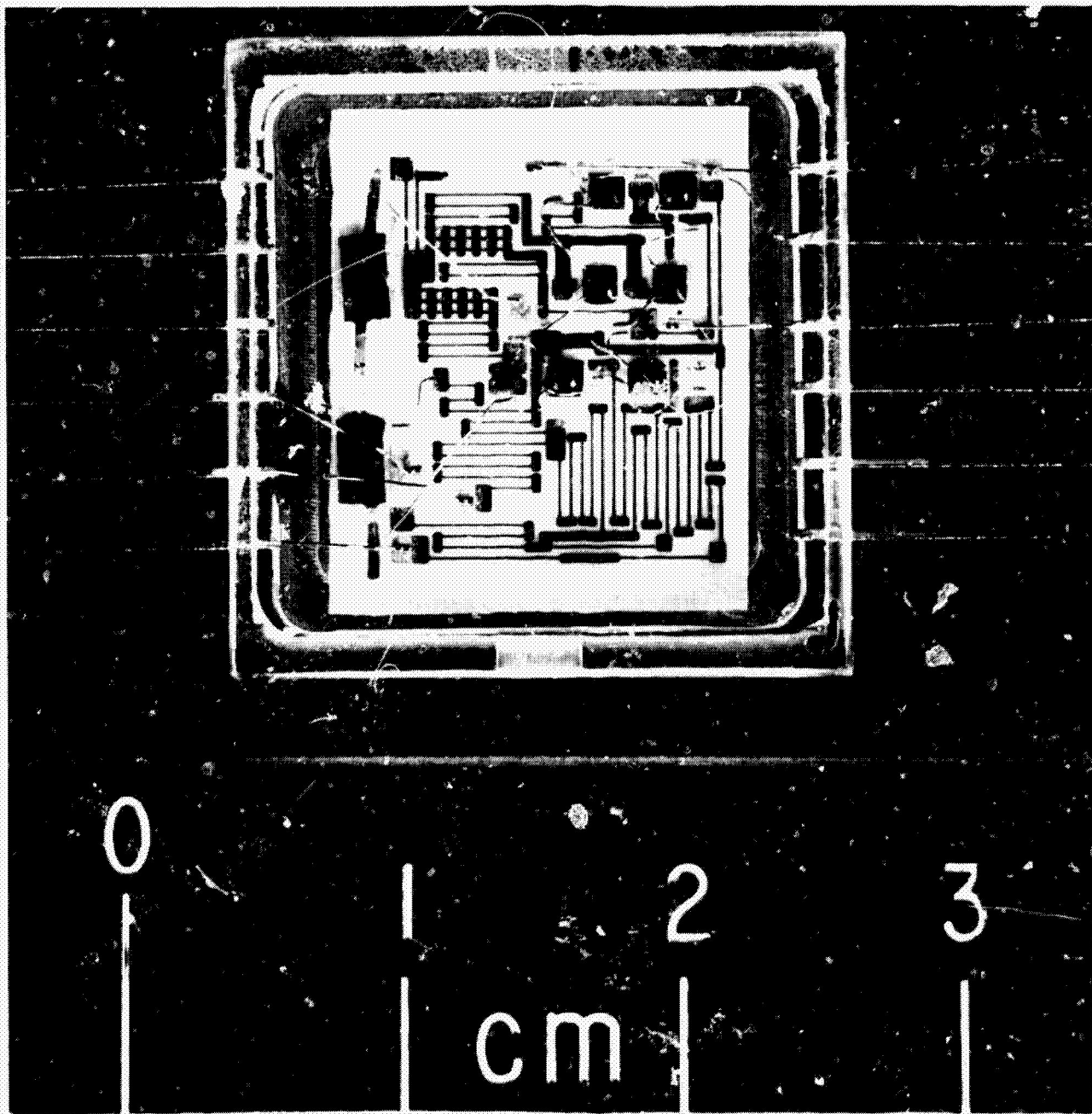


Figure 6-8—Thin-film microcircuit flatpack.

#### PRODUCTION CAPABILITIES

Sufficient progress has been made in all areas of the development program to enable MSFC to produce prototype quantities of thin-film microcircuits which are on a par with the best circuits available. On the basis of work done by three major commercial organizations on thin-film circuitry, this facility can produce smaller circuits to higher tolerances, and at a fraction of the cost of the commercial counterpart. Thin-film circuit, as used in this discussion of cost, refers to the passive thin-film circuit without active devices and packaging. Estimates of direct cost among the

three companies ranged from \$40 to \$70 per circuit, at a tolerance of  $\pm 20$  percent. This same circuit was produced at MSFC at a direct cost of \$5 and with a tolerance of  $\pm 5$  percent. The capital investment in production equipment compares at about the same or greater ratio since the whole MSFC operation is performed in an 18-inch bell jar vacuum system (Figure 6-7) supported with a small cleaning operation. The major difference in cost can be attributed to the difference in production philosophy. This laboratory has maintained the philosophy that successful thin-film circuit production could only be achieved in a single precision operation without post-deposition adjustments. Therefore, we have concentrated on precision deposition. Most other operations have used approximate depositions and depended on post-deposition adjustments which require expensive labor and in most cases expensive equipment. Some operations use the subtractive process or blanket deposition and selective etching. It is apparent that this operation is expensive because of the number of operations involved and the labor and equipment needed in addition to the deposition system. At MSFC the production labor is so small that it is not counted as a part of cost because there are only from 3 to 15 minutes of labor per circuit. A flat cost of 50 cents per passive circuit is used in estimating labor cost.

Present production capacity of the MSFC facility is from 4 to 20 thin-film circuits per hour with a yield of better than 80 percent which is more than adequate for prototype requirements, seldom exceeding 25 circuits. If all tolerances are held standard, the capacity, if needed, could be raised 6 to 36 circuits per hour, with minor modifications. This capacity could be raised to 200 circuits per hour with a modified deposition unit and added ancillary support at an approximate cost of \$35,000. Assembly and packaging capacity is limited and is adjusted from time to time to meet actual needs.

## FUTURE OF THIN-FILM MICROCIRCUITS

The potential of semiconductor monolithic circuits to meet all microcircuit requirements has not been realized. There is a trend toward custom microcircuitry, except in digital applications, particularly in space applications. The demand for these circuits is in lots of less than 10,000 and most fall in the area of 1000 circuits. This quantity is below the economical break-point of semiconductor monolithic technology which seems to be around 2500 to 5000 circuits. Thin-film circuits can be produced economically in lots of 100 to 500 circuits, depending upon the complexity of the circuit. From this, we can see that thin-film circuitry will have a definite place in space electronics.

Recent fundamental work in the field of amorphous semiconductors and on the various thin-film transistors has indicated the possibility of a major breakthrough in thin-film transistors and diodes. Grant NGR 01-003-012, Investigation of Electrical Conductivity in Amorphous Semiconductors, being conducted by Dr. A. T. Fromhold, Jr., at Auburn University was awarded to extend recent findings in this field. In-house investigations are being directed toward the geometrical problems associated with thin-film active devices. These investigations were initiated because of the unique in-house capabilities in micro-fabrication and manipulation which is one of the major

problems associated with some of the thin-film transistors. Another indication of the state-of-the-art in this field is the recent introduction of ultra-fast thin-film transistor switches and diodes to the commercial market. The development of a successful process for fabricating thin-film microcircuits with integrated active devices would lead to a greater electronics revolution than the development of the transistor. Such a development would put microcircuit production capabilities in the hands of the smallest circuit manufacturer.

#### APPENDIX — SUBSTRATE CLEANING PROCEDURE

1. Degrease in carbon tetrachloride.
2. Degrease in isopropyl alcohol.
3. Wash 15 minutes in warm detergent bath in ultrasonic cleaner.
4. Rinse in warm tap water.
5. Rinse 10 minutes in distilled water (ultrasonic).
6. Rerinse 10 minutes in distilled water (ultrasonic).
7. Vapor degrease in isopropyl alcohol.
8. Cycle through soxhlet extractor (2 cycles).
9. Leave stored in spectro grade isopropyl alcohol in extractor until used.
10. Just prior to use, slides are thermally etched in vacuum at 600° F for 15 minutes.

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N67-31569

## 7. A NEW THIN-FILM APPARATUS FOR DEPOSITING INDUCTION DEVICES AND LC CIRCUITS

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A new apparatus has been designed and built to provide a method for depositing thin-film inductors, transformers, and LC circuits. This device and its application show promise of providing inductance in the range of several millihenries per square cm. A means is provided for making transformers with center taps. This paper describes a method of depositing distributive parameter LC circuits as a single device and explains construction and operation of the mechanism along with a number of possible modifications. Also discussed is a method of using the apparatus to deposit high-value capacitors.

### INTRODUCTION

The thin-film apparatus relates in general to methods and devices for fabricating thin-film electrical components and other microcircuitry. More specifically, it is an apparatus used to fabricate, quickly and simply, thin-film inductive windings, transformers, integrated inductor-capacitor circuits, and large-area capacitors having improved characteristics in a continuous process utilizing vacuum deposition.

Thin-film electrical components and related microcircuitry are of vital importance to the space program in reducing the size and weight of manned and unmanned payloads. For example, an electronic device formerly occupying a 15-cc package fabricated with conventional components and high-density packaging techniques can now be fabricated on a thin piece of substrate material approximately one square centimeter. Thus, complex electronic circuits incorporated in on-board space vehicle equipment can be reduced in size and weight, bringing about a corresponding reduction in size and weight of the on-board equipment. Two of the most difficult problems encountered in the fabrication of vacuum-deposited, thin-film circuits are those of depositing inductors and capacitors of sufficient values for general application. The present apparatus greatly facilitates fabrication of these components, as well as many other electrical components, such as multiple-tapped transformers of both air and metal core types. The use of this method can increase the power-handling capacity of thin-film components and related circuits to a considerable extent.

Previous methods and apparatus used for the deposition of thin-film capacitors have not been entirely satisfactory because numerous layers must be deposited to achieve greater capacitance values. This involves a substantial number of separate operations and recycling of an apparatus to obtain the needed plate area, since the layers are not deposited continuously; that is, they are not formed in a continuous ribbon. The apparatus under discussion avoids the disadvantages previously mentioned and provides an accurate method for quickly depositing thin-film electrical components, including inductors, in a continuous ribbon-like fashion. The apparatus can also be employed in industries other than the space industry wherein microcircuitry incorporating thin-film components can solve problems of size and weight. For example, hearing aids and other bio-electronic devices are readily suited to the use of microcircuitry.

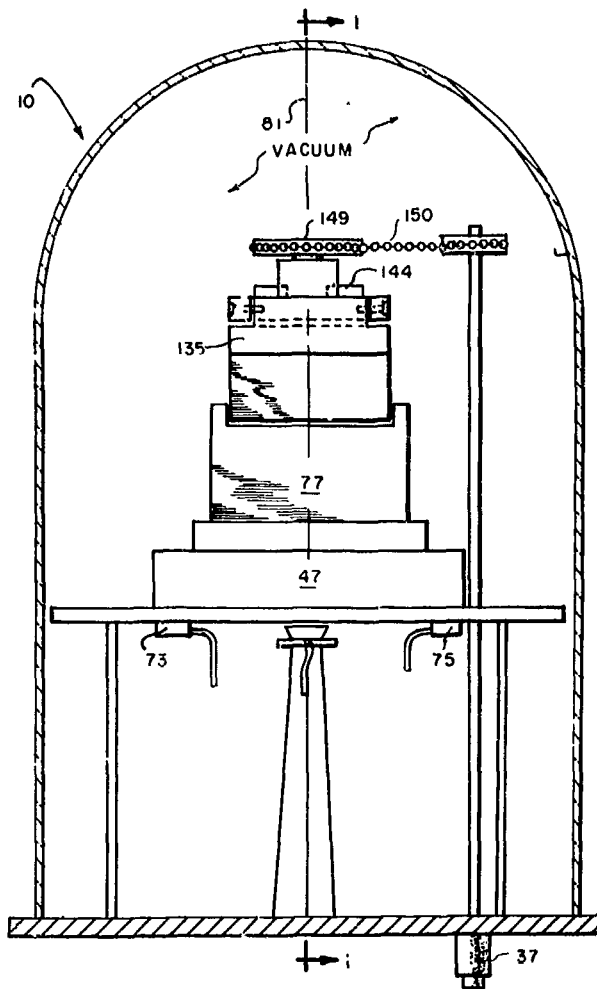
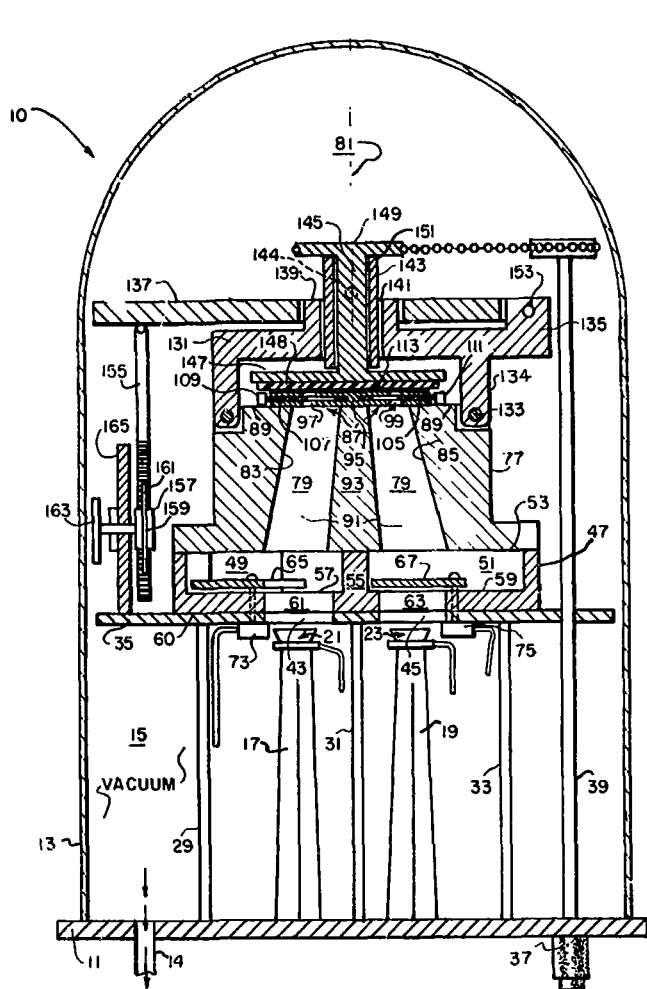
#### DESCRIPTION OF THE APPARATUS

Vacuum deposition using this apparatus is the basis of the following procedure for fabricating electronic circuitry and components. A substrate upon which the circuit or component is to be formed is rotated above a mask having openings which are controlled by an aperture control. The entire assembly is placed in a vacuum chamber above a source of conductor vapor and a source of insulator vapor. These sources are disposed in separate chambers below the mask so that portions of the substrate are exposed to the vapors as the substrate rotates. When these sources are heated, alternate and continuous layers of conductor and insulation are deposited on the rotating substrate.

This method has the following advantages:

1. Continuous helical layers of conductor and insulator material are deposited to form superimposed windings on the same radius or concentric windings.
2. Inductive windings are deposited to form inductors valued in the henry range, whereas previous methods limited inductors to the microhenry range.
3. Windings which may be tapped at desired points produce transformers of various forms and uses.
4. Distributive parameter-integrated LC circuits and large area capacitors are deposited in a continuous operation.

Other objects and attendant advantages of the present method will become more apparent when considering the following detailed description in conjunction with Figures 7-1 through 7-9.



**Figure 7-1—Apparatus for depositing thin-film induction devices and capacitors, sectioned elevation.**

**Figure 7-2—Apparatus for depositing thin-film induction devices and capacitors, side elevation.**

## CONSTRUCTION

Figures 7-1 and 7-2 show an apparatus (10) for depositing thin-film electrical components by a continuous process. It includes a circular-chamber base plate (11) that supports a transparent bell jar (13), defining a chamber (15) which is adapted for evacuation through a port (14) in the base plate by conventional means (not shown). Elongated supports (17 and 19) rest upright upon base plate and support sources (21 and 23) which contain materials to be vaporized and deposited. For example, source (23) contains insulator material. These sources can be any conventional type.

Three vertical supports (29, 31, and 33) extend upward to support a circular support plate (35) upon which the greater part of the apparatus rests. The base plate (11) supports a motor (37) exterior to the chamber (15). The shaft (39) is connected to the motor which rotates the shaft and the sprocket (41) attached to the shaft. The support plate (35) has rectangular openings (43 and

45) extending through the material; the openings direct the rising source vapors. Attached to the support plate is a rectangular plate (47), also shown in Figure 7-3, having rectangular cavities (49 and 51) formed therein that are located symmetrically with, and on opposite sides of, a partition (55) that divides the rectangular plate into halves, as measured along its longest dimension. The rectangular plate (47) has openings (61 and 63) formed therein that extend downward from bottom surfaces (57 and 59) of recessed cavities (49 and 51) to the bottom (60) of plate (47). Openings (61 and 63) are aligned with openings (43 and 45) in plate (35), respectively, so that vapors from sources (21 and 23) may rise through them.

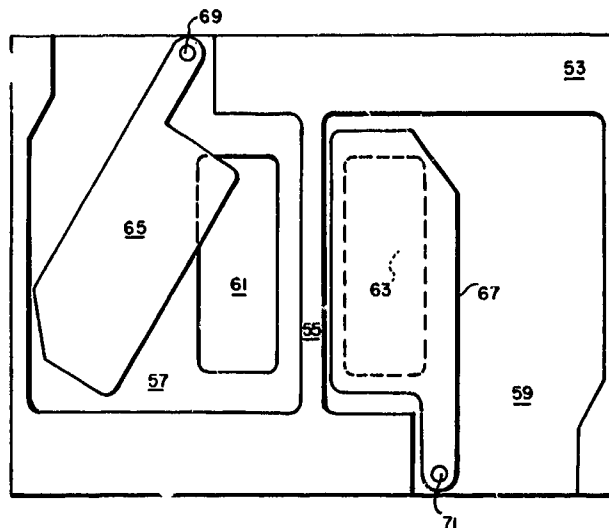


Figure 7-3—Source shutters.

Referring to Figures 7-1 and 7-3, bottoms (57 and 59) of cavities (49 and 51), respectively, serve as pivot planes upon which source shutters (65 and 67) are attached and pivoted. Shutters (65 and 67) fit flush with bottoms (57 and 59) of cavities (49 and 51), respectively, and may be rotated about pivot points (69 and 71) by electrically-operated rotating switches (73 and 75) to close openings (61 and 63) and thus prevent the source vapors from rising further. Bottoms (57 and 59) of cavities (49 and 51) form areas sufficient for the rotation of source shutters (65 and 67) in the opened and closed positions.

A rectangular block (77) is attached to, and rests upon, top surface (53) of plate (47). Block (77) includes a truncated conical chamber (79) which is symmetrical about a central axis of rotation (81) normal to plate (35). Sides (83 and 85) of chamber (79) slope inwardly so that upper end (87) of chamber (79) is smaller than bottom opening (91) in block (77). Chamber (79) is shown divided into two equal chambers by a wall or partition (93). Chamber (79) can be divided into four equal chambers when necessary for certain depositing operations. A type of flue arrangement (not shown) may be incorporated so that only two sources, one of conductor and one of insulator material, are employed to supply four chambers with vapors.

A mask carrier (Figure 7-1) is attached to, and rests upon, top surface (89) of block (77). Mask carrier (95), shown in detail in Figures 7-4 and 7-5, is symmetrical about central axis (81) and is a disc having two arc openings (97 and 99) located equal radial distances from central axis (81) and diametrically opposite one another. Mask carrier (95) is also provided with horizontal slots (101 and 103) in which slide aperture controls (105 and 107) are actuated by solenoids (111 and 109). Mask (113) is attached to, and rests upon, the mask carrier (95). The mask is circular in shape and approximately 0.7 mm thick with slotted exit apertures (115 and 117) located therein in a circular pattern about the axis (81).

pivot platform (137) so that when pivot platform (137) is rotated in a vertical plane, bearing (143), together with shaft (145), remains parallel with axis (81), and thereby with the plane of mask (113), when the height of the substrate above the mask is adjusted by a mechanism discussed later.

Pivot platform (137) is a flat plate which is pivotally connected by pin (153) to pedestal (135) of the pivot table; the other end of platform (137) is in contact with an adjustment post (155). Adjustment post (155) is vertical and can be raised or lowered to pivot platform (137); thus, because of the pivot connection between platform (137) and bearing (143), the substrate and mask remain parallel with respect to each other when platform (137) is pivoted. Post (155) is held secure by a cylindrical bracket (157) which has a lateral dimension. Slot (159) provides an access opening through which a gear (161) operates. Gear (161) is shaft-connected to adjustment nut (163). Bracket (157) is attached to, and supported by, a vertical member (165) which is attached to, and supported at its lower end by support plate (35). Post (155) has teeth (158) formed thereon which are engaged by gear (161), so that rotation of gear (161) will raise or lower post (155).

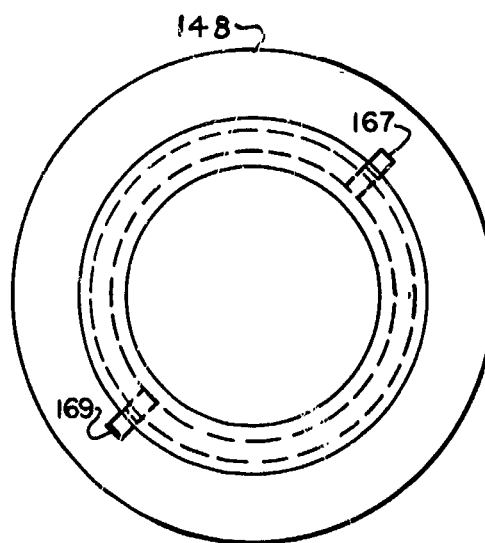


Figure 7-6—Substrate with deposited windings connected to connection lands.

## OPERATION

The apparatus is prepared for depositing a single insulated winding on a substrate in the following manner: Substrate (148) is prepared to receive the winding by predepositing metallic starting and ending connection lands thereon before the winding is started. The mask (113) used is shown in Figure 7-4. Substrate (148) is then attached to substrate holder (147) and aligned with starting connection land (167) (Figure 7-6) located above conductor aperture (115) (Figure 7-4). The thickness of deposited films is determined by the evaporation rate of sources (21 and 23, which may be referred to as a source unit), the arc length of exit apertures (115 and 117), and the speed of rotation of substrate (148). Adjustment post (155) is adjusted to bring substrate (148) within the proper distance above mask (113). Vacuum chamber (15) is evacuated to the proper point for evaporating the materials used (normally  $5 \times 10^{-5}$  Torr).

Source shutters (65 and 67), mounted between sources (21 and 23) and mask (113) to allow opening and closing the vapor path to substrate (148), are now closed, and sources (21 and 23) are brought to a proper temperature for a desired evaporation rate. Aperture controls (107) are adjusted by solenoid (109) to expose connection aperture (119) by means of aperture (129) and close exit aperture (115). Aperture control (105) is adjusted by solenoid (111) for the desired insulator deposition. Shutter (65) is opened by the rotating switch (73); the connection to connection

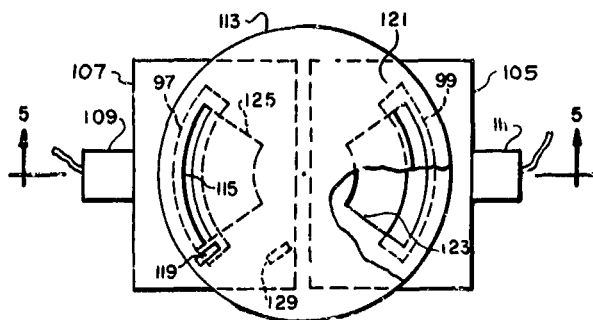


Figure 7-4—Mask carrier, top sectioned view.

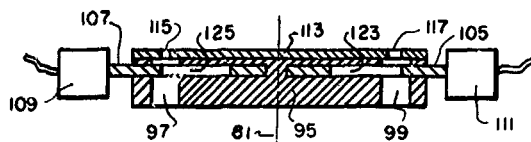


Figure 7-5—Mask carrier, sectioned elevation.

Exit apertures (115 and 117), being narrower than exit aperture (117), through which insulation material is deposited, form arcs and are located above their respective sources with exit aperture (115), through which conductor material is deposited. Exit aperture (117) is wider than exit aperture (115) to ensure proper insulation of the conductor film as it is deposited in a continuous process. A connecting aperture (119) is also located in the mask (113). It is rectangular and located at the end of conductor arc (115). Its function is to deposit connections from the windings to the connecting lands so that the elements may be connected in thin-film circuits or microcircuits.

Aperture controls (105 and 107) are rectangular tabs with pie-shaped openings (123 and 125) centrally located therein so that the arc length of exit apertures (117 and 115) may be shortened or lengthened, respectively, as controls (105 and 107) are pulled out of, or pushed into, slots (103 and 101) provided in the mask carrier (95). Connection land opening (129) is provided in aperture control (107) and exposes connection land opening (119) in the mask to permit the passage of vapors only when exit aperture (115) is completely closed off by pulling control (107) out a proper distance by operation of solenoid (109). This allows connections to be made from conductor to connection lands, and there is no interference with the deposition of the conductor or insulation since that phase of the method is stopped.

Figure 7-1 shows a pivot table comprising a horizontal plate member (131) from which two vertical supports (132 and 134) extend downward at right angles to the horizontal plate member, with vertical support (134) being pivotally attached to block (77) by pivot connection (133). Rectangular pedestal (135), integral with the pivot table, provides a means for mounting pivot platform (137). The pivot table includes a raised annular shoulder (139) located symmetrically about central axis (81). Shoulder (139) has a circular opening (141) extending through plate member (131) to allow a shaft bearing (143) mounted therein to move along axis (81) with some degree of freedom.

Bearing (143) encloses a drive shaft (145), connected at its lower end to a substrate holder (147). The substrate holder is rotated by drive shaft (145) having sprocket (149) mounted thereon. Sprocket (149) is rotated by chain (150), which is driven by electric motor (37), shaft (39), and sprocket (41). Sprocket (149) rides on surface (151) of bearing (143). Substrate holder (147) is a flat disc to which substrate (148) is attached. Bearing (143) is pivotally connected by pin (144) to

land (167) (Figure 7-6) is deposited, and shutter (65) is closed. Aperture control (107) is adjusted by solenoid (109) to expose exit aperture (115) through which the conductor is deposited. Shutters (65 and 67) are opened, and substrate (148) is immediately placed in controlled rotation by an electric motor (37) which drives sprockets (41 and 149) through shaft (39) and chain (150). As the apparatus operates, each vapor source (21 and 23) deposits a thin-film helix on substrate (148). The radius of the helix deposited is determined by the radial distance of exit apertures (115 and 117) from axis (81). With apertures (115 and 117) at equal radial distances from axis (81), multi-turn helices of conductor and insulator are deposited one upon the other, with each succeeding source (either 21 or 23), in the direction of rotation, depositing a layer upon the preceding layer. The operation is continued until the desired number of turns are deposited. Each revolution of substrate (148) deposits one turn. It is then stopped in line with ending connection land (169) (Figure 7-6), and shutters (65 and 67) are closed. Connecting the end of the winding to connection land (169) may be done by a separate operation after removing substrate (148) from the vacuum chamber, or it may be carried out by operating solenoid (109) to move aperture control (107) to a position wherein aperture (129) is aligned with connection aperture (119) in mask (113). Shutter (65) is opened and conductor vapor rises through exposed openings (43, 61, 79, and 97) and is deposited upon substrate (148) through aperture (119).

Figures 7-7 through 7-9 show masks with aperture configurations for depositing other components. Certain modifications (not shown) of the apparatus shown in Figure 7-1 may be made to operate the apparatus using masks shown in Figures 7-7 through 7-9. The masks may be used without aperture controls, or aperture controls may be incorporated. A flue arrangement (not shown) may be incorporated when four separate chambers, that is two source units, are required.

Multiple insulated windings on the same radius are deposited with the mask shown in Figure 7-7 which requires a source unit and a pair of connection lands for each winding. Exit apertures

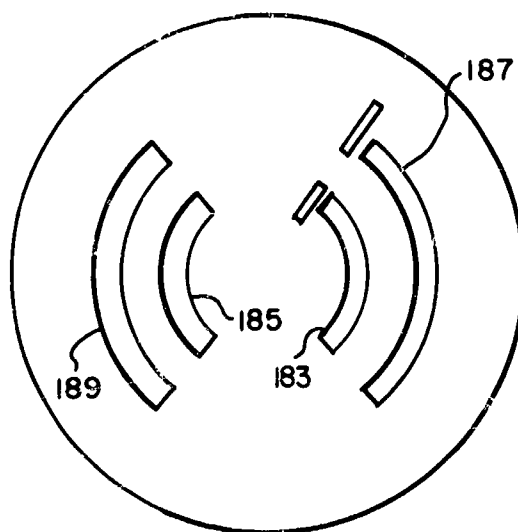
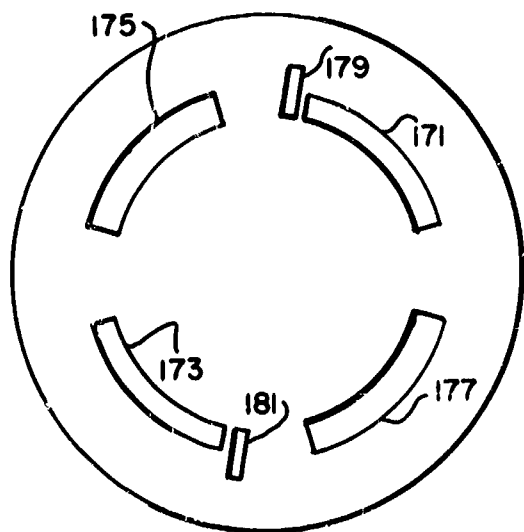


Figure 7-8—Mask, aperture configuration for depositing multiple windings on same radius.

Figure 7-7—Mask, aperture configuration for depositing multiple winding on same radiums.

(171, 173, 175, and 177) are placed on the same radius and are alternated, each conductor aperture (171 and 173) followed by an insulator aperture (175 and 177, respectively), in the direction of rotation. Connection lands are so located on the substrate that alignment of the starting land for the first winding with the conductor aperture will align each succeeding conductor aperture with the appropriate starting land. The same applies to the ending connection lands. Connection apertures (179 and 181) are provided in the mask and may be used if aperture controls are used to expose the apertures at the necessary times.

Concentric windings on different radii are deposited, using the mask shown in Figure 7-8 by the same procedure as described previously, except that the apertures (183 and 185) form one of the concentric windings, and apertures (187 and 189) form another of the concentric windings. Only one source unit is required. Each pair of apertures (183 and 185) are located on the same radius but on a different radius than the other pair (187 and 189).

Capacitors are deposited by the same procedure except that a different mask, shown in Figure 7-9, is used. Exit apertures (191, 193, 195, and 197) are wider to provide a greater area per turn, and only starting connection lands are required. Connection apertures (199 and 201) are provided therein.

Integrated LC circuits are easily deposited by the use of the procedure described for single insulated windings. The desired inductance and capacitance being known, the winding area and number of turns to achieve the desired inductance are determined. The capacitance is adjusted to the desired value using the area-per-turn from the inductance calculations, the dielectric constant, and the thickness of the insulator. The width of the conductor is then adjusted to give the desired distributive capacitance between any two turns.

## CONCLUSION

This apparatus provides a continuous and simple method utilizing vacuum deposition for fabricating thin-film electrical circuit components and microcircuitry. Numerous modifications and variations of the present method are possible.

## ACKNOWLEDGMENT

The author wishes to thank Mr. G. L. Filip for his invaluable assistance in building this apparatus from sketches.

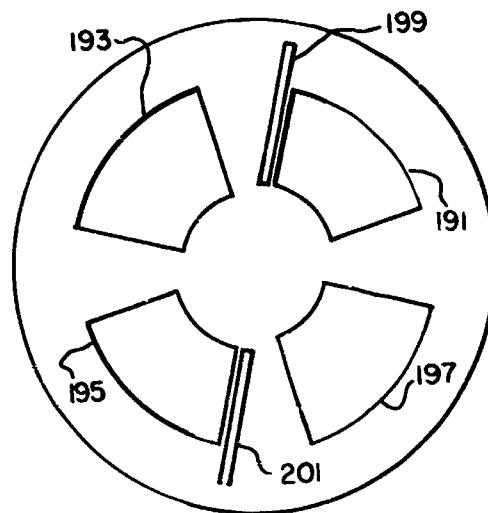


Figure 7-9—Mask, aperture configuration for depositing helical capacitors.



N67-31570

## 8. AN IMPROVED SPATTERPROOF VACUUM EVAPORATION SOURCE

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This report presents a new design concept for an improved spatter-proof vacuum evaporation source for use in depositing thin solid films on a substrate. Construction details designed to prevent emission of high-velocity solid particles that would damage the deposited film are described and illustrated. Simplicity and economy of construction and modest operating power requirements, as compared with presently available sources, are also discussed. This design has been proven in production use.

### INTRODUCTION

Spattering of evaporation source material, with the resultant damage to films being deposited, has long been a problem for workers engaged in vacuum deposition of thin solid films (References 1 through 6). Film damage is caused by large solid particles that leave the source at high velocity and strike the film. This type of damage is particularly detrimental to the formation of dielectric films in thin-film capacitors. Several sources have been developed in an attempt to eliminate this problem, but they are complicated to fabricate and require an excessive amount of operating power. The source described here consists of a thin-gauge evaporant cartridge with a dimpled top on which a series of small vapor-vent holes circle the outer edge of the dimple (Figures 8-1, 8-2, and 8-3). A baffle strip with an exit port is welded over the perforated dimple in such a manner that the vapor stream from the vent holes is deflected to preclude direct-line emission of solid particles from the exit port in the baffle.

This source is easily fabricated, gives excellent thermal transfer, requires modest operating power, and results in excellent spatter suppression.

### DESCRIPTION

The source is made from two strips of refractory metal foil. Tantalum is chosen as the material for most applications because it is easily worked with conventional forming tools and, in many cases, the thin foils may be worked by hand. One strip is formed into a rectangular cartridge (Figure 8-1). The second strip is welded over the perforated dimple to act as a baffle.

The formed sleeve is filled with the evaporant material, crimped at each end, and the ends are clamped with the electrode clamps. When the source reaches the operating temperature for the material being evaporated, vapors fill the cartridge and escape through the exit holes into the dimple cavity. There they are reevaporated or reflected through the baffle port. Most of the large particles ejected from the bulk evaporant are trapped in the cartridge. The few that manage to pass through the exit holes are trapped in the dimple cavity. Occasional particles may escape by passing in a line through the exit holes and baffle port. Their low trajectory, however, will not permit them to strike the substrate overhead. This construction has been found to be satisfactory for most applications.

In those cases where complete trapping is necessary, the dimple and baffle construction shown in Figure 8-2 may be used. It may be noted from the figure that particles passing from the exit holes cannot pass directly through the baffle port. It should be further noted that the contour of the dimple does not affect the angular distribution of the vapor particles. It was found by Knudsen (Reference 7) that the reflection or reevaporation of vapor particles is random and has no relationship to the angle of incidence.

## CONSTRUCTION

The source is constructed by spot welding two strips of refractory metal (Figure 8-1). One strip is folded to make the main body, or sleeve, while the other strip forms the baffle. Source dimensions are determined by the distance between the clamping electrodes, the power limitations, and the desired evaporant capacity. The size of the dimple is governed by the required evaporation rate and source size. The dimple may extend over the greater part of the sleeve length if an extended source is desired, or it may be reduced to an approximate point-source, which will limit the evaporation rate. The exit holes surrounding the dimple should be kept as small as practicable to limit the size of the particles that may escape into the dimple cavity. The exit holes are placed so that they are around the rim and just inside the dimple.

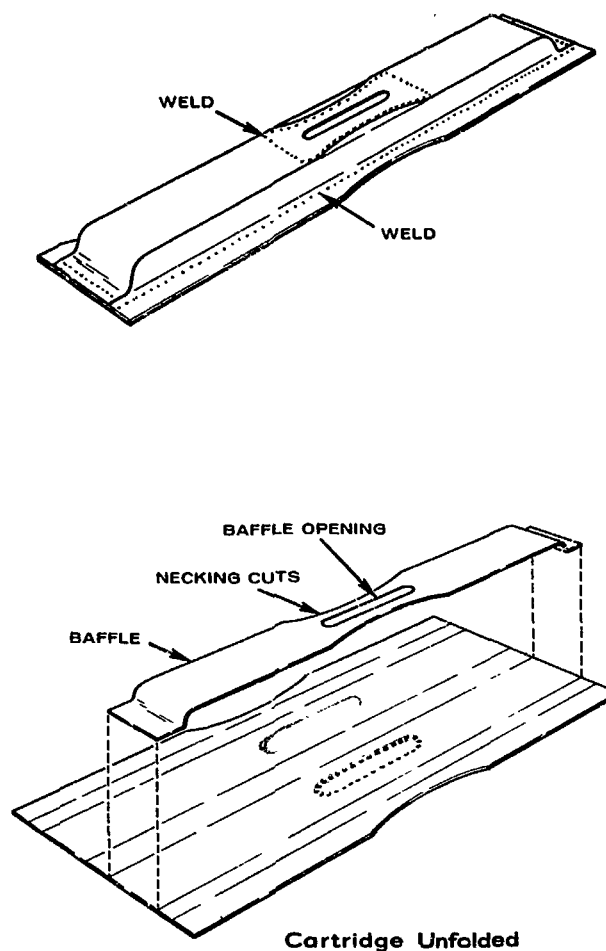


Figure 8-1—Spatterproof evaporation source.

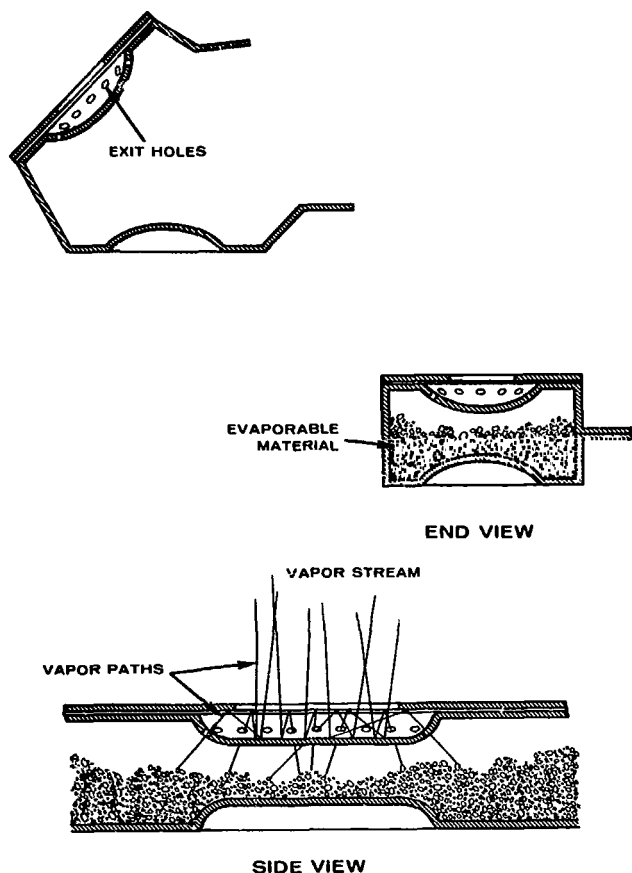


Figure 8-2—Cartridge construction.

clogging of the exit holes during operation. The bottom dimple reduces the amount of evaporant in the vicinity. The completed source is crimped together at one end and welded. The crimp is made along the line of the side welding flange to present a uniform cross section the clamping electrode. The source is then filled with the evaporant material from the open end, which is then crimped. This end is not welded, to provide a means of refilling the source by spreading open the crimped end.

## OPERATION

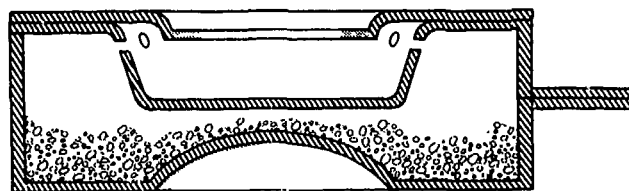
The source is filled with the evaporant material through the unwelded end, which is then crimped closed, and the source is inserted between the clamping electrodes. The evaporant material may be of any suitable grain or particle size, since the thermal transfer is uniform throughout. The heating current is passed through the source to bring it to the proper operating temperature. Those evaporants that require a bake-out before evaporation may be baked out in the source, thus eliminating the separate bake-out operation. When the source is brought to the proper operating temperature, the vapors pass through the exit ports in the dimple cavity and are reflected or re-evaporated upward to the substrate. Gross particles explosively ejected are trapped in the

The baffle strip is made the same length and width as the sleeve to insure uniform resistance over the length of the source. The baffle opening is made smaller than the dimple to provide a covering over the exit holes, thus preventing particles from escaping in a vertical direction and striking the film being deposited on the substrate. Low-angle trajectories are possible with the dimple construction shown in Figure 8-3, but particles cannot reach the substrate in a direct path.

In those applications where complete particle trapping is desired, the dimple construction shown in Figure 8-3 is recommended. It should be noted that there is no line-of-sight in this construction from the dimple cavity through the baffle port. A sleeve constructed from straight strips will heat uniformly over the full length when a current is passed through it. The necking cuts (Figure 8-1) are made to reduce the cross section of the source in the dimple area. This creates a hot spot in the dimple area which is required to prevent

dimple cavity by the baffle strip. There is little probability that the few that escape at low trajectories will reach the substrate and damage the film being deposited.

In the dimple design shown in Figure 8-3, it can be seen that particles cannot escape from the dimple cavity without at least two rebounds, resulting in the loss of much of their kinetic energy. This design is recommended for complete trapping of gross particles.



END VIEW

Fig. 8-3—Dimple detail for small angle distribution.

## CONCLUSIONS

The evaporation source described in this report is a satisfactory method for controlling particle spatter encountered in the vapor process for depositing thin films. Variation of the dimple contour permits versatility of design applications to cover a broad range of particle trapping requirements. Because of simplicity of fabrication, operating power economy, and reusability of the cartridge, this source is preferred to other available systems.

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N67-31571

## 9. A NEW THIN-FILM MICROCIRCUIT DEPOSITION MECHANISM

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A new thin-film circuit deposition mechanism was designed and built. The mechanism handles six 5 by 5-cm substrates, six masks, and 12 vapor sources. The substrate and mask selection mechanism has only one moving part. The mechanism will fit into a 45-cm glass bell jar and features six automatic resistance and thickness monitoring strips, water cooling, individual substrate heating at each station, and a registration accuracy of 0.0125 mm.

### INTRODUCTION

One of the basic requirements of a microcircuit deposition process is a mechanism which can operate with any combination of substrates, masks, and evaporation sources. The mechanism must be extremely precise in locating the mask over the substrate. It must provide electrical power, instrumentation, and water cooling for components where required. The mechanism must be able to function at high temperatures in a vacuum without malfunctioning. The mechanism should be simple to operate and be easy to clean and maintain. The thin-film microcircuit development program at MSFC created a demand for such a device.

Examination of commercially available, and number of custom-built, thin-film circuit deposition units revealed that all of the units suffered from deficiencies that would impair thin-film circuit development. One of the more promising units was purchased and tested. After extensive modifications, this unit was made to operate satisfactorily until a suitable unit could be designed and built. Most of the units examined suffered from the same deficiencies. The most common deficiencies encountered were the following.

1. The elaborate mechanical arrangements require frequent repairs and adjustments. This situation makes the machines difficult to maintain and makes cleaning a formidable task.
2. Unidirectional indexing deprives the operator of the flexibility of repeating operations without going through the full deposition cycle, which includes a larger number of operations.

3. Most source-to-substrate distances are too short for good line definition without excess shadowing.
4. Most source holders are too small and require breaking the vacuum in midcycle to recharge the small sources.
5. Registration accuracies are generally poor. One machine was advertised as having an accuracy of  $\pm 0.0025$  mm registration in one plane; however, the accuracy was no better than 0.02 mm in the other two planes. This situation was further aggravated by poor substrate positioning in its holder. This error must be added to the registration error.
6. Some of the machines are difficult to load and unload because the substrate holding fixture could not be released, and the substrate carrier could not be disengaged from the drive mechanism to allow rapid loading.
7. Substrate and mask carriers cannot be separated sufficiently to allow easy masks changing.
8. Machines using a multiple source carrier suffer from sliding contact problems at high currents. These problems lead to arcing and galling between the contact shoes and the slip ring.
9. Machines using resistance monitors generally have contact problems because of poor design or contamination from the sources.
10. Machines are not properly shielded for cross-contamination of source material.
11. Most of the machines have minor deficiencies that require modification before satisfactory operation could be expected.

The experience gained from this study and subsequent operations was utilized to design and build a new thin-film circuit deposition unit (Figures 9-1 through 9-6) which eliminated or minimized the difficulties encountered. This machine, a completely integrated carousel-type unit, requires no attachment to the vacuum system other than four clamps which seal an "O" ring around the base after the unit has been inserted into the vacuum chamber. The unit can be inserted into any suitable overhanging vacuum chamber (Figure 9-5) within a few moments without major modification to the system. This arrangement allows maximum access from top, bottom, and three sides, which greatly facilitates cleaning, adjustments, modifications, and repairs. Any conventional vacuum system can be adapted to this unit by removing the bell jar and installing an overhanging metal chamber as shown in Figures 9-5 and 9-7.

The machine is designed to handle six 5 by 5-cm substrates, six masks, and 12 sources. It is divided into six isolated evaporation chambers effectively baffled to prevent cross-contamina-

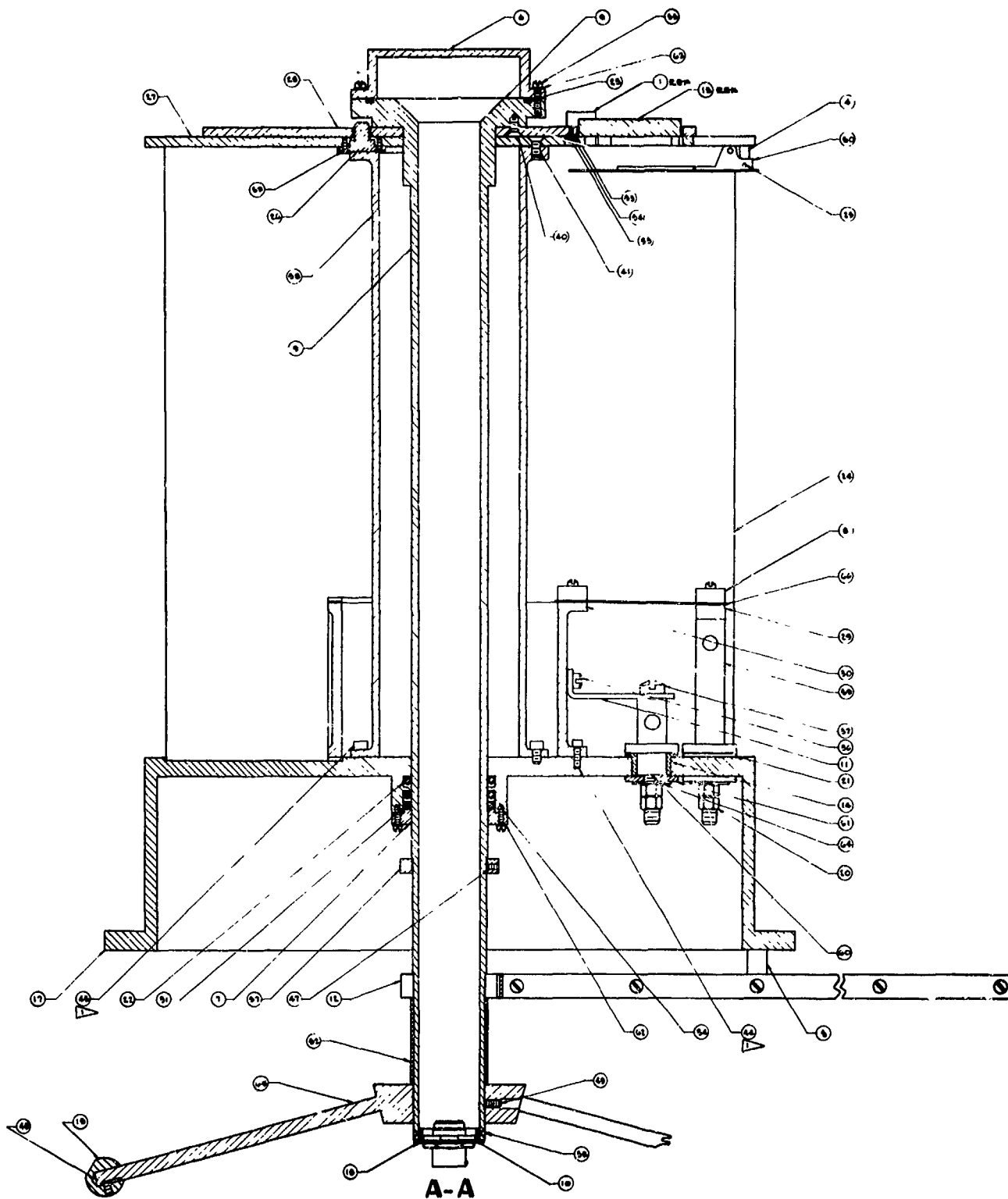


Figure 9-1—Thin-film microcircuit deposition unit assembly drawing, sheet 1 of 2.

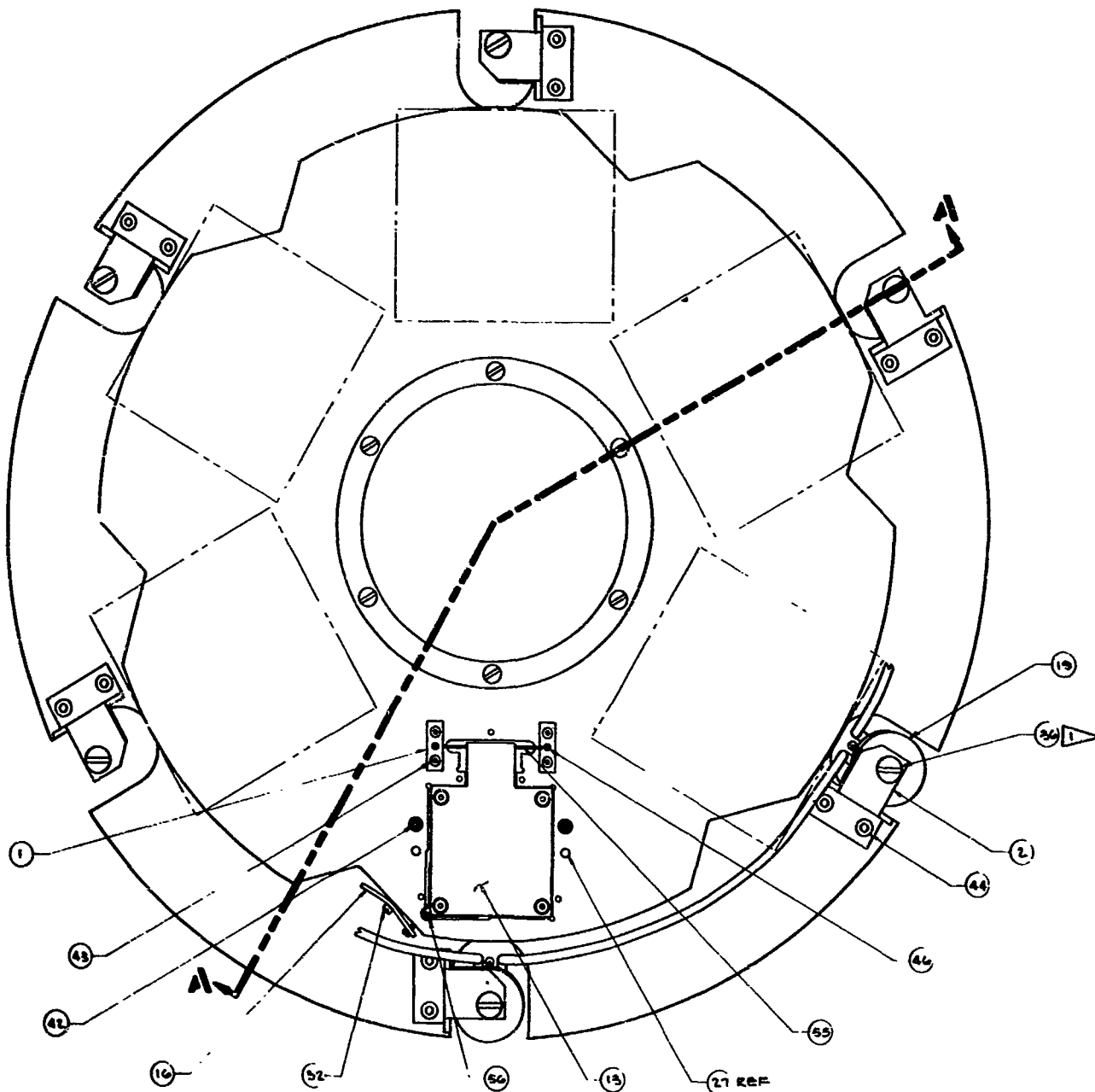
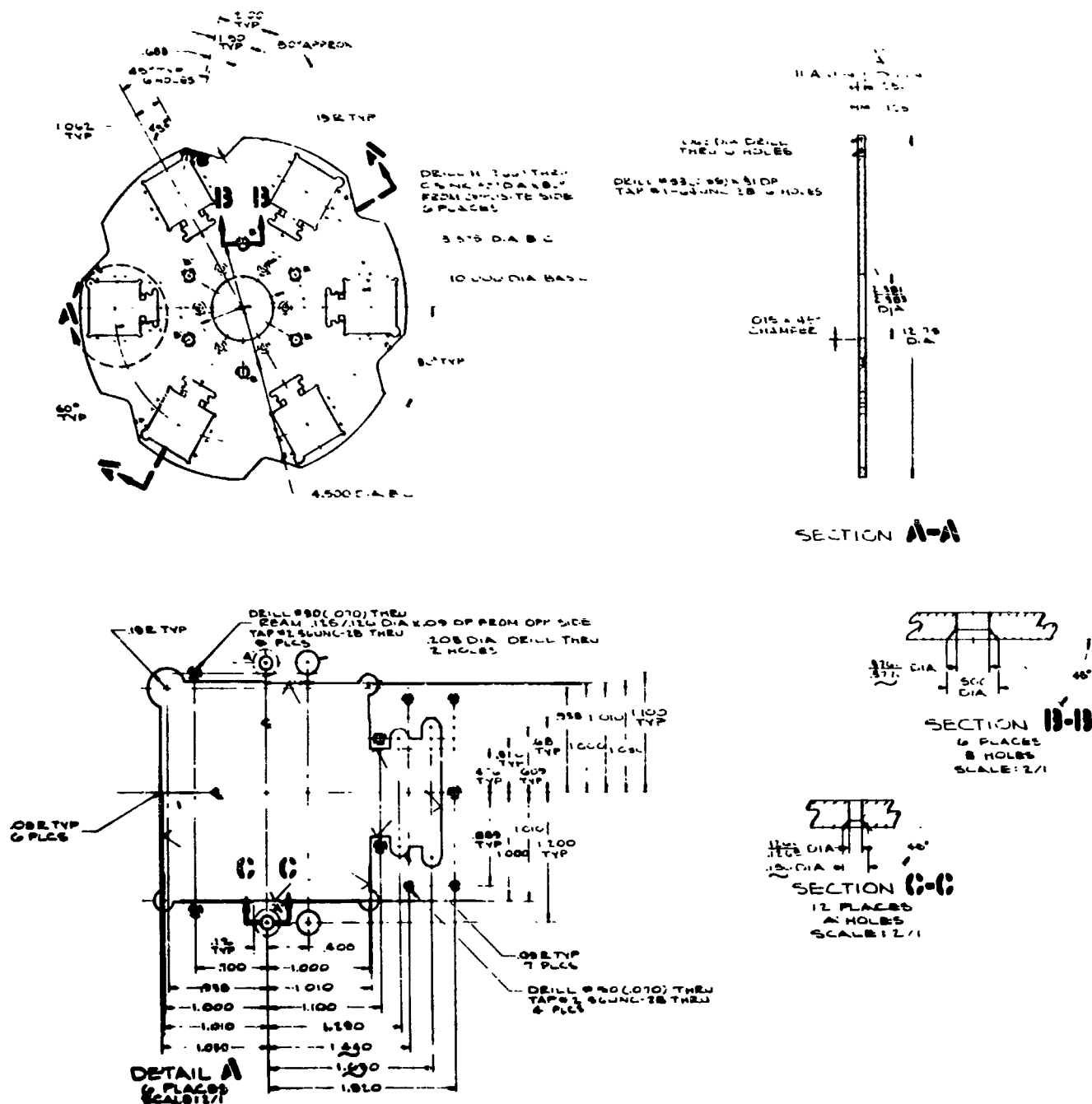


Figure 9-2—Thin-film microcircuit deposition unit assembly drawing, sheet 2 of 2.

tion between chambers; however, the baffling is designed so that it does not interfere with the flow of gases to the pump since each chamber opens directly into the vacuum chamber from the bottom. This arrangement has the effect of providing six independent vacuum evaporation chambers. Each chamber is individually equipped with a mask, an electrically controlled shutter, two evaporation sources, and a water-cooled crystal monitor (Figures 9-5 and 9-6). Each of the six substrate positions is individually equipped with a resistance monitor assembly, a heater, and a thermocouple. Mechanical feedthrough provides for vertical and rotational motion as well as electrical power and instrumentation wiring for the resistance monitors, heaters, and thermocouples.



"REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR."



**Figure 9-3—Substrate carrier plate (top plate) drawing.**

## CONSTRUCTION

Construction details are shown in Figures 9-1 and 9-2, the index numbers for which are given in the following list.

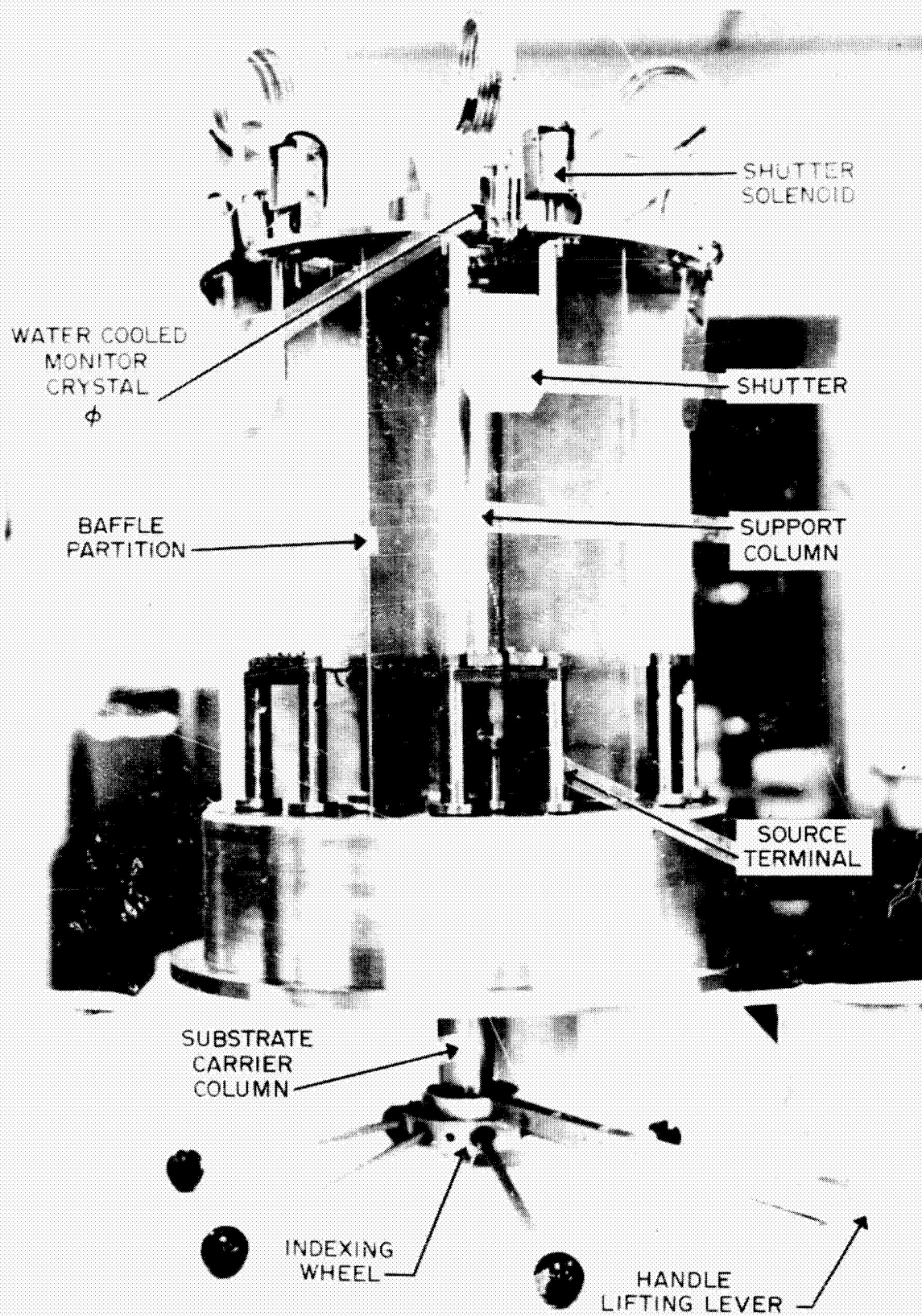


Figure 9-4—Basic assembled thin-film microcircuit unit.

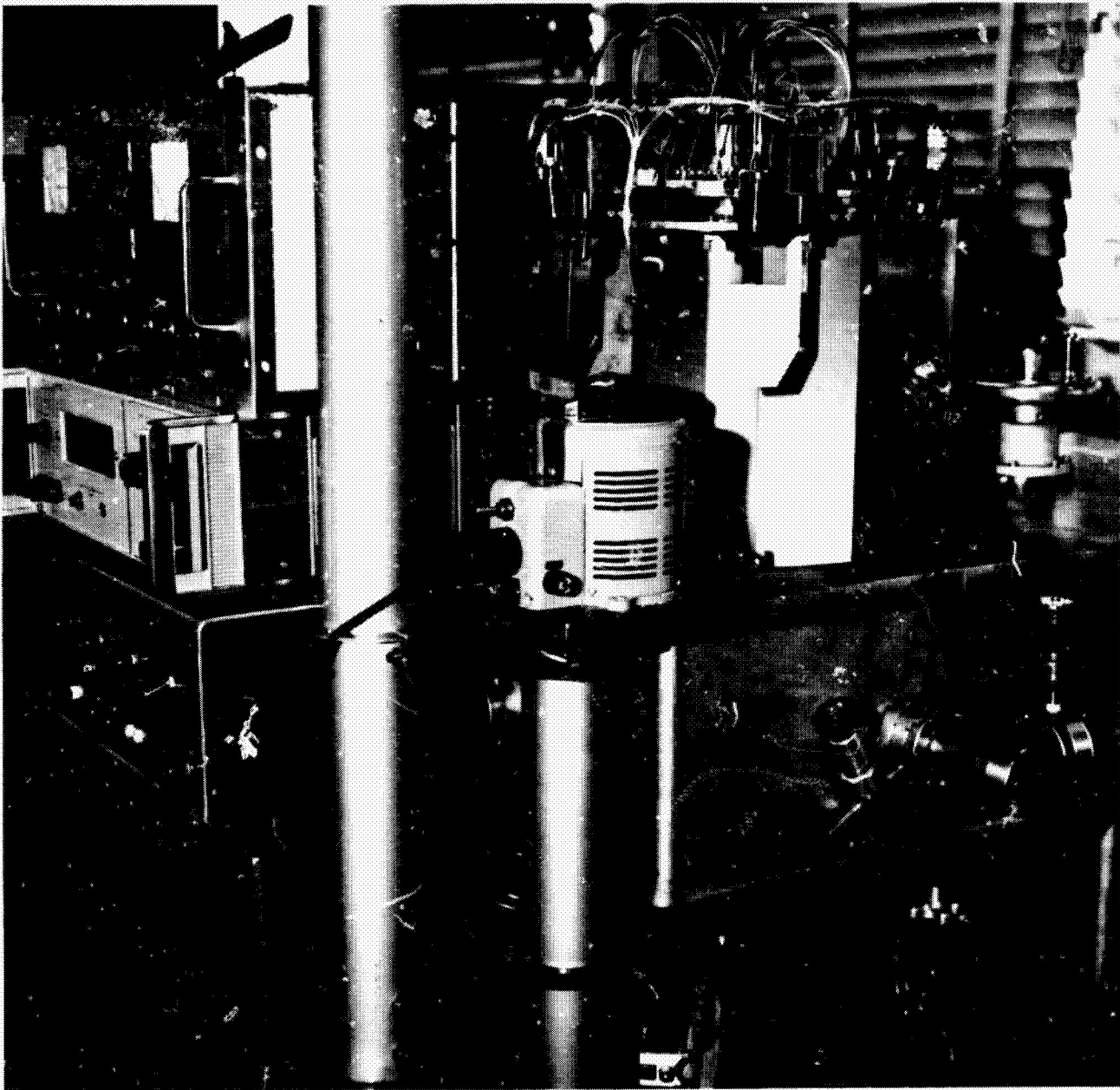


Figure 9-5—Thin-film microcircuit unit installed in overhanging vacuum chamber.

Index Number	Description	Index Number	Description
1	Block, contact	34	Screw, #6-32 fil. hd.
2	Bracket, monitor	35	Screw, #8-32 fil. hd.
3	Bracket, pivot	36	Screw, 1/4-20 fil. hd.
4	Bracket, shutter	37	Screw, 3/8-16 fil. hd.
5	Bracket, solenoid	38	Screw, #4-40 flat hd.
6	Cap, feedthru	39	Screw, #4-40 flat hd.
7	Cap, o ring	40	Screw, 1/4-28 flat hd.
8	Clamp	41	Screw, 1/4-20 flat hd.
9	Column, substrate carrier	42	Screw, #2-56 sock. hd.
10	Connector	43	Screw, #2-56 sock. hd.
11	Connector, grd	44	Screw, #8-32 sock. hd.
12	Lever, lifting	45	Screw, 1/4-20 sock. hd.
13	Heater assy.	46	Set screw, #2-56
14	Insulator	47	Set screw, #6-32
15	Knob	48	Set screw, #8-32
16	Lever, spring	49	Set screw, #10-24
17	Mount, base	50	Shutter
18	Mount, connector	51	Solenoid
19	Monitor, crystal	52	Spacer column
20	Nut	53	Space, insulation
21	O ring	54	Spacer, screw
22	O ring	55	Spring, contact
23	O ring	56	Spring, substrate positioning
24	Partition	57	Stop, column
25	Pin	58	Column, center support
26	Pin, dowel	59	Terminal
27	Plate, mask carrier	60	Terminal
28	Plate, substrate carrier	61	Washer, insulator
29	Post, extension	62	Washer, lock
30	Ring, terminal	63	Washer, lock
31	Ring, teflon	64	Washer, plain
32	Screw, #1-64 fil. hd.	65	Wheel, locator
33	Screw, #2-56 fil. hd.	66	Wire

The new mechanism is a carrousel-type assembly as shown in Figures 9-1 and 9-2. The fixed structure is a tubular column (58), mounted in the center of the base mount (17); it supports the mask carrier plate (27), which carries the masks, the water-cooled crystal monitor heads, and the shutters. The moving substrate carrier assembly is made up of the locator wheel (65), the substrate carrier column (9), the release lever (12), the feedthrough cap (6), and the substrate carrier plate (28) the resistance monitor assemblies, the substrate heaters, and the thermocouples.

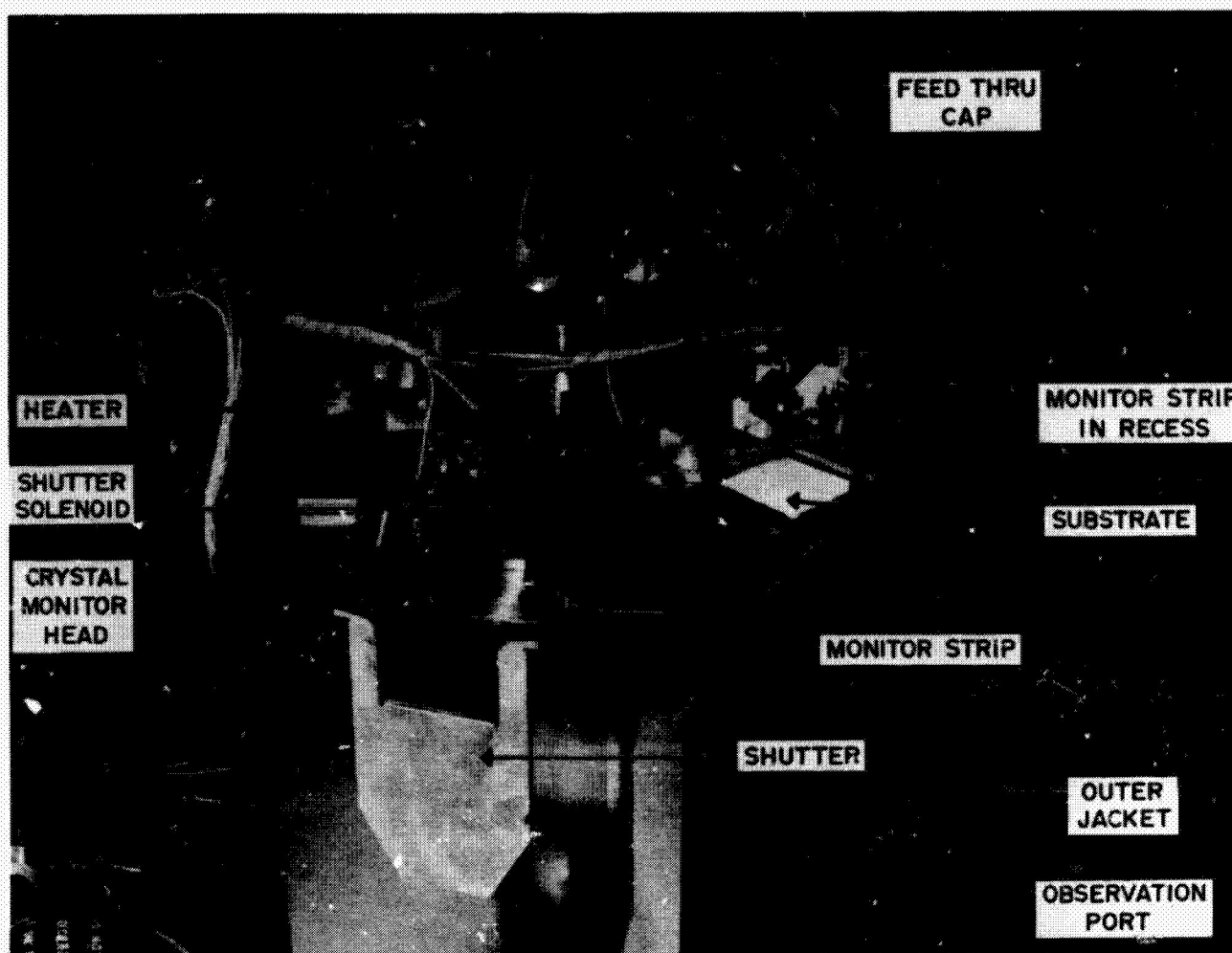


Figure 9-6—Top view of thin-film microcircuit unit.

The substrate carrier column (9) passes through the mask carrier plate (27), the center support columns (58), and the base mount (17), where it is sealed with a double O-ring seal. The mask carrier plate acts as a loose fit pilot bearing for the substrate carrier column during rotational motion. The moving electrical wiring passes through the feedthrough cap, the substrate carrier column, and the connector (10) to the control console.

The substrate carrier plate (Figure 9-3) has six recesses for carrying six substrates and six resistance monitor strips which are carried in the small recess extending from the substrate recess as shown in detail A, Figure 9-3. The substrate heater (13) fits into the substrate recess and rests on the substrate and the monitor strip. The monitor strip is a small glass or ceramic strip of the same material as the substrate, which has silver tabs at each end. These tabs are separated by a measured distance. The monitor strip is dropped into position in the recess with the silver contacts down. Two beryllium copper spring contacts (not shown) mounted in contact blocks (1) pass around and beneath the monitor strip where the spring contact points are located beneath the silver contacts, approximately 0.375 mm above the recess bottom.

The weight of the heater forces the monitor strip down against the contact points and bottom stops (not shown). This arrangement compresses the spring contacts and establishes a firm contact between the spring contact and the silver contact tabs. The substrate is held in position against the bottom stops by the weight of the heater. It is held in horizontal position by the action of the quick-release spring mechanism (16 and 56), which forces the substrate against three alignment bosses on the sides of the substrate recess (detail A, Figure 9-3).

Twelve indexing holes ("A" holes, Figure 9-4) are aligned with indexing pins (not shown) in the mask carrier plate (27). These holes and pins are located within a tolerance of  $\pm 0.0125$  mm. These pins also serve as the mask alignment pins.

The mask carrier plate carries the masks, which are aligned by alignment pins, shutter mechanisms, and the water-cooled crystal monitor heads. The shutter (50) is operated by a solenoid as shown in Figure 9-4. The shutter has a cutout at the pivot edge to allow the crystal monitor to be exposed to the vapor stream when the shutter is in the opened or closed position. This arrangement allows the operator to establish the evaporation rate before the shutter is opened. The source heaters are installed between the terminals (59) and the common ring terminal (30). Provision is made for two source heaters in each compartment. Four feedthrough parts (not shown) are provided for electron beam and induction-heated sources.

Electrical wiring for power and instrumentation is terminated in a control console (not shown) which houses the power supplies and instruments. Resistance monitoring is performed either automatically or manually by a digital ohmmeter. Signals from the crystal monitor head are sent to a crystal oscillator control which automatically regulates, deposition rates and thickness. The instruments shown on the left in Figure 9-5 are the instrument breadboard which will be replaced by a console. In addition to housing the instrumentation, the console will also support the end of the vacuum chamber. This arrangement will allow the removal of the existing supports and will greatly improve the accessibility of the entire system.

## OPERATION

The unit is placed in operation by first loading it with the appropriate sources, masks, substrates, and monitor strips. To load the masks, raise the substrate carrier plate (28) by unlatching and pressing down on the lifting lever (12). After the masks are loaded, the substrate carrier is lowered back into place. The sources are loaded by clamping them between terminals (29 and 30) with clamp (8). The substrates and resistance monitor strips are loaded by removing the heaters from their recess and placing the substrates and monitor strips in their respective

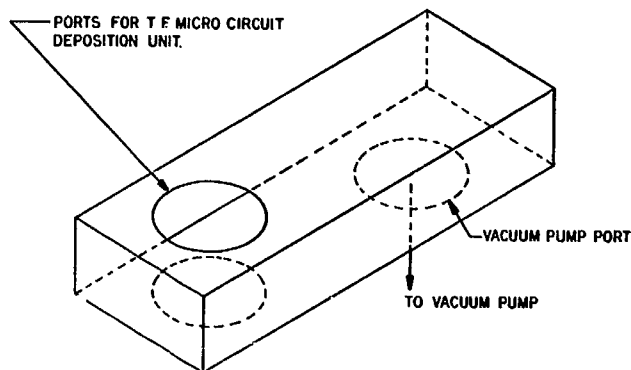


Figure 9-7—Overhanging vacuum chamber adapter.



recesses, making sure that the silver contacts on the monitor strip are facing down. The heaters are then replaced, the bell jar is lowered into place, and the vacuum cycle is initiated. Since the sources are fixed along with the appropriate mask, subsequent operations only involve moving the appropriate substrate over the proper mask in the predetermined sequence. This is accomplished by raising the substrate carrier over the indexing pins as previously explained and rotating it to the desired position by use of the locator wheel (65).

## CONCLUSION

The moving parts of the indexing mechanism have been reduced to a single, jam-proof moving part. Moving electrical and mechanical motion feedthroughs have been effectively reduced to a single mechanical feedthrough. Precision indexing has been established in three planes. The unit is simple in construction and easy to adjust and clean. Effective baffling is provided to minimize cross-contamination of source materials. Rotational motion is provided in either direction and any substrate, mask, or source combination can be obtained in a single motion. Source-to-substrate distance is long and can be easily shortened, if desired, by extending the source terminals. Provision is made for two large sources in each chamber. Loading and unloading the unit is made easy by use of a quick-release substrate holder and by the provision of adequate space between the substrate carrier plate and the mask holding plate. High current sliding contacts have been eliminated. Positive resistance monitor contacts which are free from contamination are provided. The unit is completely integrated and may be used in any vacuum system without modification by use of an overhanging vacuum chamber, as shown in Figures 9-5 and 9-7. The unit has been proven in production.

## ACKNOWLEDGMENT

The authors wish to express appreciation to Mr. William A. Boshers, who made the drawings for this apparatus, and provided helpful suggestions in the final design.

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N67-31572

## 10. GAP WELDING PROCESSES AND APPLICATIONS

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The gap welding process has been studied, and procedures have been established to achieve maximum results. The process is shown to be dependent upon the control of materials and geometry. The application of gap welding to a wide range of electronic interconnection problems is described. The technique used in welding wires and ribbons ranging from 0.025 to 0.5 mm in size with a single welder is also described as is welding thin films, thick films, and printed wiring boards. A sample circuit utilizing a new design concept, planar gap welding, for component assembled circuits is shown, beginning with the electrical schematic to the finished circuit.

### INTRODUCTION

Because of its simplicity, ease of production, high strength, and because it can be visually inspected, gap welding is proving to be the greatest advance in electronic interconnections during the past 50 years. The technique is a modification of the 3-electrode, series resistance weld (see Reference 1). The similarity of the two types of welds is illustrated in Figure 10-1. The split electrode used in gap welding is shown in Figure 10-2, and a weld head for gap welding is shown in Figure 10-3. Bywaters (Reference 2) first suggested the gap welding technique as a means of interconnecting flat integrated circuit packages. As a result of the Bywaters paper, the Microelectronics Unit at MSFC began a study of the technique in 1962 for the purpose of developing the technique for general application to microcircuit interconnections. The preliminary study revealed that it was possible to develop the method into a nearly ideal

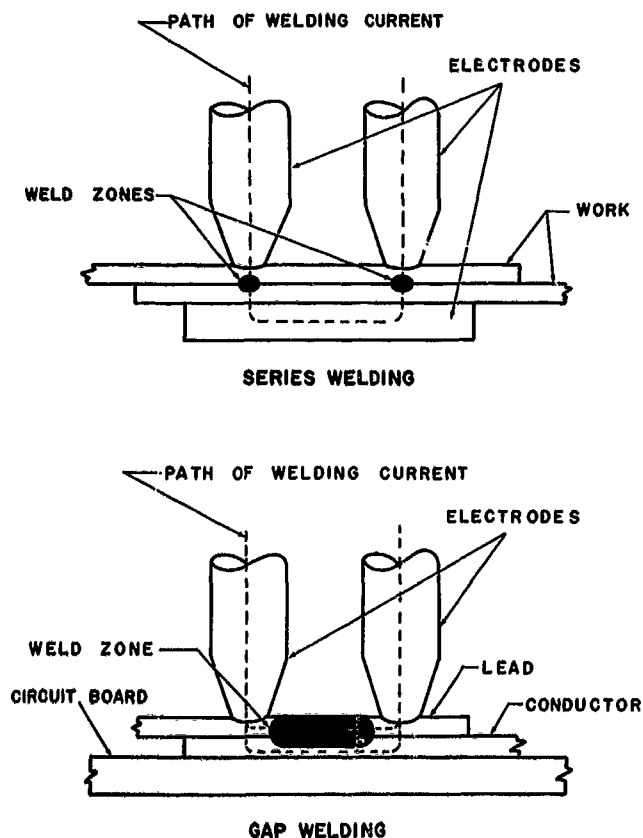


Figure 10-1—Comparison of series welding and gap welding.

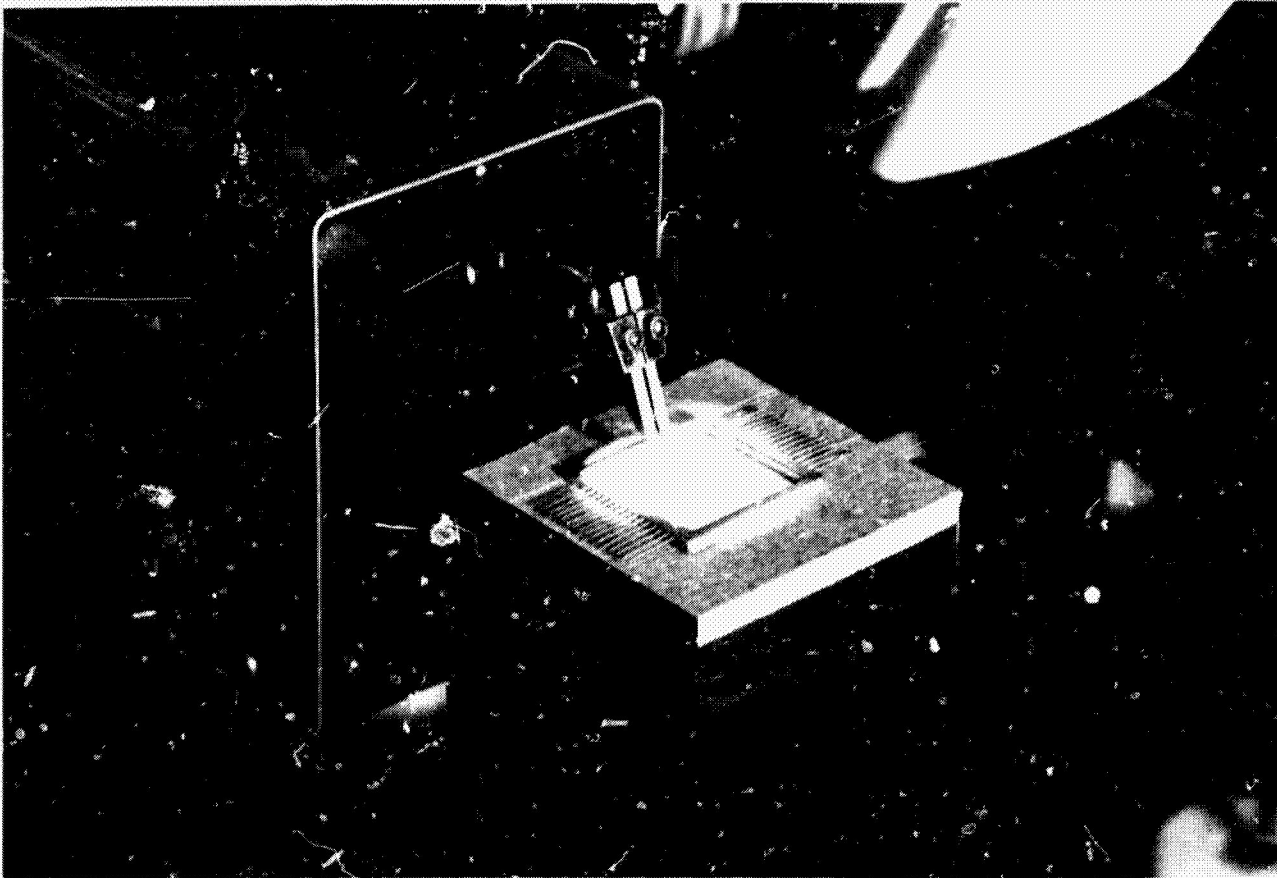


Figure 10-2—Split electrode used in gap welding.

interconnection process. This process could be performed by unskilled operators; the results could be visually inspected for quality; there would be negligible variation in weld strength between welds; welds would closely approach the strength of the parent material; and the welding process would not affect the adjacent components.

#### GAP WELDING PROCESS

Unfortunately, mathematical treatment of the dynamics of resistance welding electrothermal phenomena defies solution, primarily because of the transient nature of the process and the number of variables involved. In the normal resistance spot weld, the variables are the resistances, tip pressure, welding current, and time. Each of these variables is dependent upon the others and also upon the reaction of the welding circuit to its variations. If a fixed-weld power pulse is assumed, the most important variable is the tip pressure and its influence on contact resistance. The resistance weld is strongly dependent on the selection of the proper pressure as illustrated in Figure 10-4. Mayo (Reference 3) has shown that there is a broad variation of contact resistance between measurements when the same materials and a fixed pressure are used. This variation increases as the applied force is reduced. From Figure 10-4, it can be seen that increasing

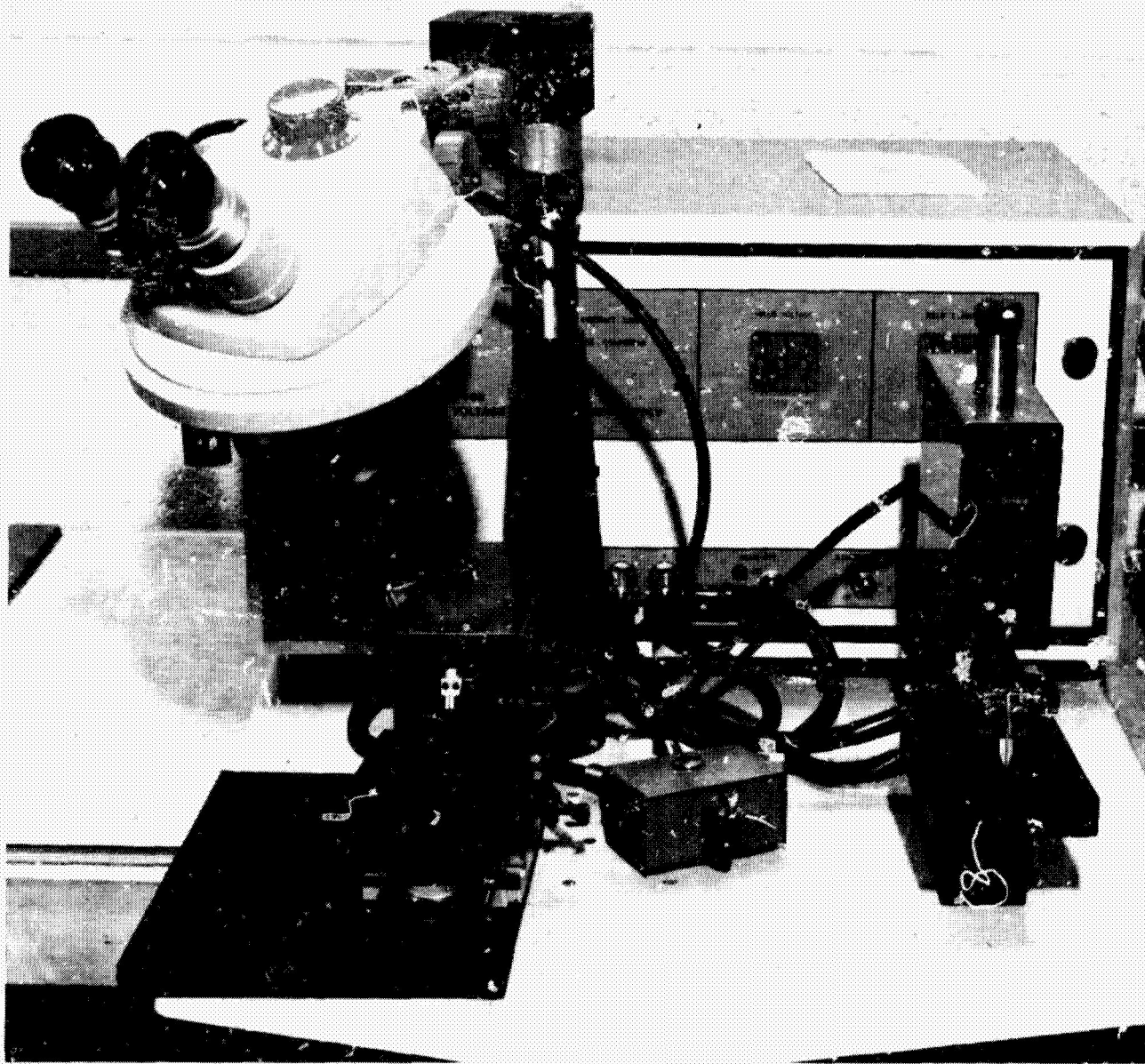
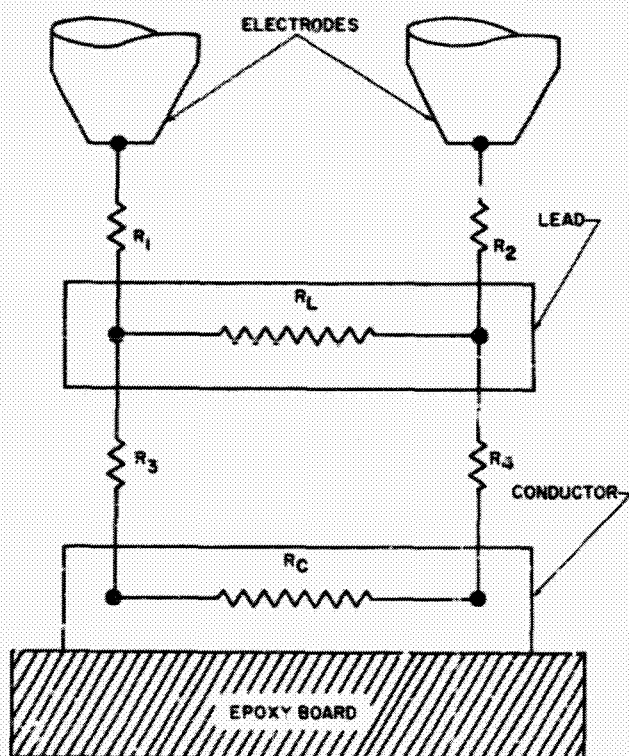


Figure 10-3—Gap welder.

the pressure decreases the contact resistance and, at the same time, reduces the resistance spread. Operating at high pressure is not practical in resistance spot welding because contact resistances are necessary to initiate resistance heating at the joint. However, in gap welding flat ribbons, the heating resistance is solely dependent upon the intrinsic dynamic resistance of the weld materials. Referring again to Figure 10-4, it is necessary to apply sufficient pressure to reduce the contact resistance to a minimum. This practice will allow only negligible heating under the electrode tips, provided that the resistance of the work is much higher than the contact resistances. The resistive circuit of the gap welding arrangement is illustrated in Figure 10-5. In this illustration, contact resistances  $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$  are low because of the pressure applied;

$R_L$  and  $R_C$  are the intrinsic resistances of the upper (lead) and lower (conductor) work pieces, respectively. These two resistances should be approximately equal. Comparing Figure 10-5 and Figure 10-6, it can be seen that if a current is passed between the electrodes and through the work, the highest current density is in the upper part of the top work piece  $R_L$  and the lowest density is in the lower work piece  $R_C$ . This current distribution is governed by the interplay of surface conduction, the geometry of the system, and the blocking action of the contact resistance ( $R_3$  and  $R_4$ ) between the work pieces.

When a high-current weld pulse passes through the foregoing system, the approximate current density (Figure 10-6) is such that it will



$R_1$  AND  $R_2$  - CONTACT RESISTANCE OF ELECTRODE  
 $R_3$  AND  $R_4$  - CONTACT RESISTANCE OF UPPER AND LOWER WORK PIECES  
 $R_L$  - RESISTANCE OF LEAD  
 $R_C$  - RESISTANCE OF CONDUCTOR

Figure 10-5—Resistive network of gap weld.

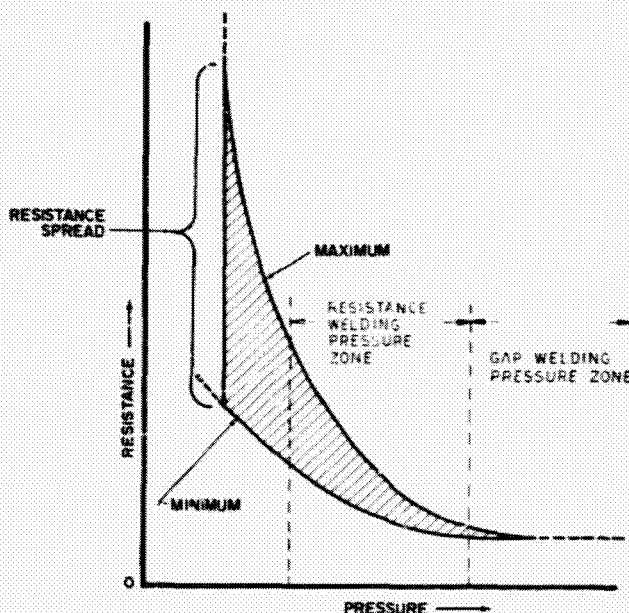


Figure 10-4—Welding pressure vs. resistance curve.

cause rapid heating of the upper work piece. As the heating progresses in the upper work piece, the resistance in that piece rises accordingly, and the current is progressively shunted into the lower work piece, which also heats. The current is continued until fusion takes place. The thermal properties of the copper electrodes and the dielectric circuit board act to confine the hot zone to an area bounded by the electrodes and the upper part of the lower work piece. The growth of the fusion zone from the top center, outward and downward is shown in Figures 10-7 and 10-8. This growth has been studied by use of the high-speed motion picture camera, and the method of growth has been confirmed. Figure 10-9 shows weld growth in 10 percent increments, starting at 50 percent of weld energy on the left and ending at 100 percent weld energy on the right.

Gap welding is suggested as a means of connecting small Kovar leads on integrated circuits by Bywaters (Reference 2). Many printed wiring (PW) board materials have been

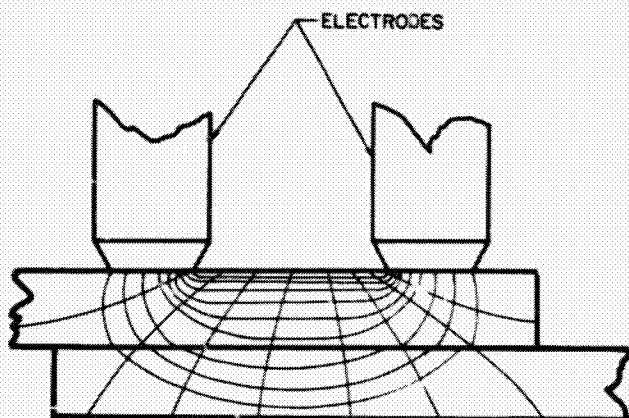


Figure 10-6—Equipotential and current density in the gap weld flat lead.

tested at this laboratory, and it has been determined that Kovar-to-Kovar welds are ideal for gap welding applications. Nickel PW material makes excellent welds, but these welds cannot be inspected for reasons given later. The testing of gap welds made on printed wiring boards presents some difficulties, primarily because the quality of the welds has far exceeded expectations. All of the welds tested to date, for 0.125 x 0.35-mm Kovar leads welded to a .015-mm Kovar PW board having a 5-kg peel strength, were found to meet the minimum quality standard; i.e., the weld must never break under any type of pull test. This standard was adopted as

a result of repeated tests at this laboratory and can be explained by the fact that the work pieces before welding are in the soft, annealed condition. The welding process leaves the work in the full hard condition in the weld zone. This situation leads to a weld that is stronger in the weld zone than the parent materials.

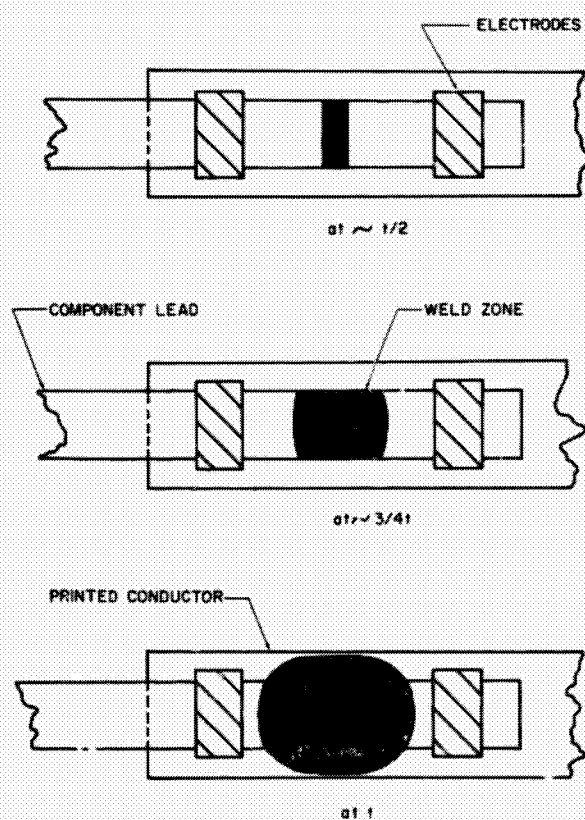


Figure 10-7—Weld growth, top view.

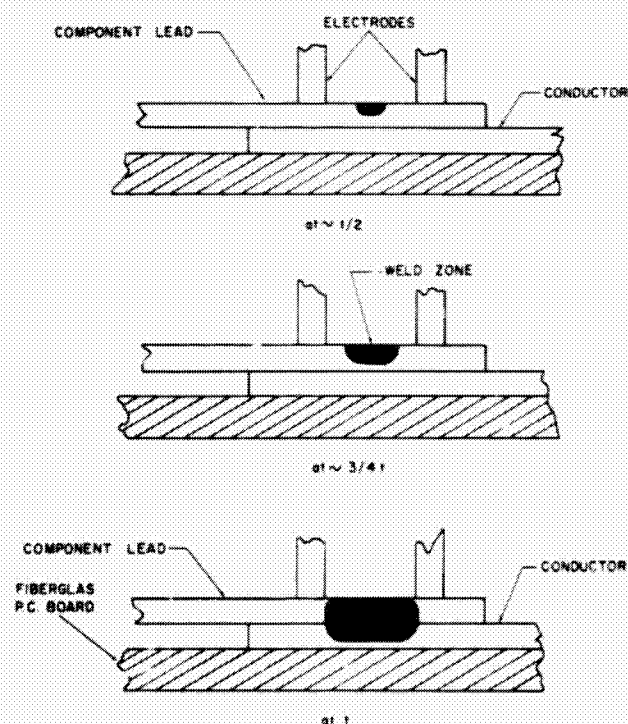


Figure 10-8—Weld growth, side view.





Figure 10-9—Weld growth in 10 percent increments.

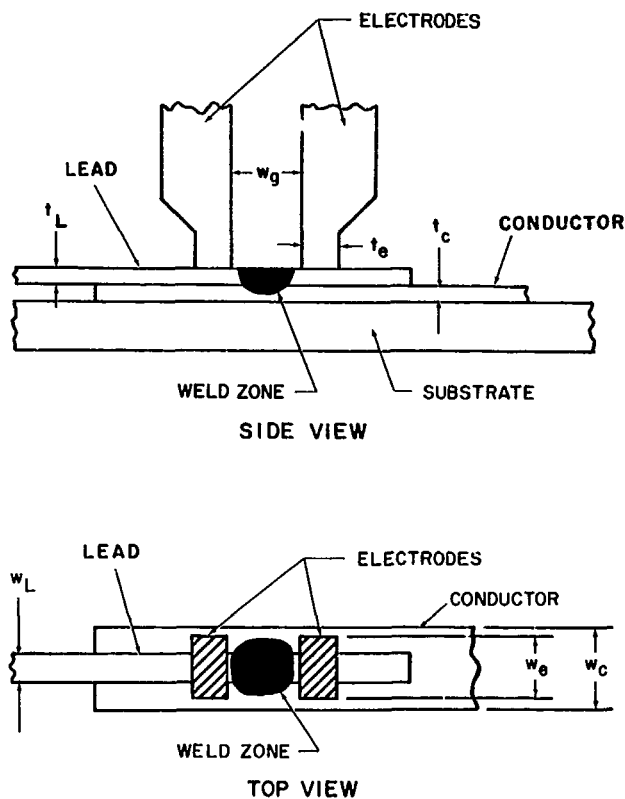
During welding investigations, it was found that gold-plated nickel/iron alloys tend to blacken in areas where the temperature reaches the softening point of the alloy. This condition is caused by diffusion of the gold plating into the base material, thereby exposing the hot iron to the atmosphere and forming a black iron oxide film in the fusion zone as illustrated in Figures 10-7 through 10-9. It was found that gold plating thicker than 3.75 microns did not diffuse completely. Therefore the gold plating should be between 1.25 and 3.75 microns thick. This discovery suggested a method of indirectly inspecting gap welds and led to the establishment and testing of an inspection criterion. This criterion assumed that if the gold diffusion marked the bounds of the fusion zone of the weld, a good weld should show gold diffusion completely over the upper work piece and on the surface of the lower work piece in the area of contact between the two work pieces. This assumption was tested on several thousand welds, using a pull tester; in all cases where this condition existed, the welds were excellent. With the use of gap welding and inspection in accordance with the criterion described, joint failures can be reduced to below two failures per million joints. At this writing, more than 100,000 welds have been made and tested, and no defective welds have been found. The inspection criterion established at this laboratory is as follows (Reference 4).

- (a) The darkened area must extend over an area of not less than 80 percent of the electrode gap covering the entire upper work piece in this area; the area must be clearly visible on both sides of the lower work piece under 30x magnification, and must extend along the lower work piece by not less than 50 percent of the electrode gap.
- (b) The weld must show no visible mechanical defects.

Gap welding is not limited to the welding of integrated circuits. It has a wide range of application. Using this technique, we have consistently made good welds on a wide range of materials varying from 1.75 mm by 5-mm material down to 0.025-mm wire. As indicated earlier, gap welding is a geometric process related to the geometry of the weld materials and the welding tips. A study of the geometry of the system has led to the establishment of the following dimensions (Figure 10-10).

Thickness of lead .....	$t_L$	$= x$
Width of lead .....	$w_L$	$= (3 \pm 0.4) x$
Thickness of lower conductor .....	$t_c$	$= (.7 \pm 0.1) x$
Width of lower conductor .....	$w_c$	$= w_c + (0.075 \text{ to } 0.175 \text{ mm})$
Thickness of electrode tip .....	$t_e$	$> 1.7 x$
Width of electrode tip .....	$w_e$	$> 3.5 x$
Width of electrode gap .....	$w_g$	$= (4.5 \pm 0.5) x$

MSFC-SPEC-270 establishes lead sizes and tolerances. With reasonable quality control over the weld materials, all of the variables of welding can be brought within a range that is easily controlled. Tests indicate that a tolerance of  $\pm 10$  percent in any of the variables in the process will not affect weld quality. Consequently MSFC Procedure 429 has been adopted to establish gap welding as the standard technique for welding materials to weldable PW boards.



## GAP WELDING APPLICATIONS

### Microbonding

The gap welding process has been extended to microbonding round wires from 0.02 to 0.2 mm in diameter to small structural welding up to 0.5 cm thick with equal success. Microbonding by the gap welding process can be best described as a resistance-heated thermocompression bond and is restricted to those materials which readily diffuse. As in thermocompression bonding, the best material for the process is gold. The dynamics of the process are closely related to the ribbon weld previously described. The major difference is that the contact area does not remain constant when welding the round wire as it does in the ribbon weld; thus a finer balance between the pressure and energy adjustments must be maintained. Fortunately, as in ribbon welding, the process

Figure 10-10—Gap welding arrangement and dimensions.

is somewhat self-regulating. Another difference in the two welds is that of the temperature required to make the bond. Ribbon welds are fusion welds in the sense that the weld is made at the plastic temperature of the work, whereas the microbond, being a diffusion bond, can be made below the plastic temperature. In fact, care must be taken in microbonding to avoid melting the work and causing it to separate and ball up at each end through the action of surface tension. Furthermore, the microbond requires more time for diffusion across the interface. The time for bond formation in the ribbon weld is between 5 and 9 milliseconds, whereas the time required for the microbond is between 100 milliseconds and 1 second, dependent upon the temperature in the hot zone. This situation is in agreement with the Jost diffusion equations for liquids and solids (Reference 5). In practice, we operate very near the liquidus temperature, and the best setting for microbonding has been found to be 200 milliseconds.

Microbonding is best accomplished with a constant-voltage welder as will be shown later. The weld pressure is set by observation since the delicate pressures are very difficult to measure accurately. The method used by the author is to start the pressure setting at zero and to alternately increase the pressure and bring the tips down on the wire until the wire is deformed sufficiently to present a flat surface about  $1/3$  the diameter of the wire. Then set the weld timer at 200 milliseconds, and the weld energy at zero. Press the tips onto the wire and alternately fire the welder while increasing the weld energy in small increments until the wire begins to collapse. The weld energy is increased in small increments until the wire has collapsed to approximately 50 percent of its original diameter. Move to a new weld point on the wire and make finer adjustments until the desired collapse is achieved. The pressure setting is then recorded. Gold wire on thin films gives the highest strength when collapsed to approximately 40 percent of the original diameter. This practice provides a larger contact area and thus results in a higher joint strength since film adhesion is the weak point in the structure. However, these benefits are achieved at the expense of the wire strength in the pinch at the edge of the weld zone; therefore, a balance must be established between the strength of the film and the strength of the wire at the pinch by pull test.

From the preceding arrangement, it can be seen that if the electrodes are pressed to the work and the welder is fired, the approximate current density will be as shown in Figure 10-11. Comparing this with Figure 10-6 shows that the current is shifted upward and passes a narrower gap with the major part of the current confined to the upper work piece; thus the heating is confined to the upper work piece, which is the desired condition. At the start of the weld pulse, the major part of the heating is under the electrode tips as in resistance welding because of the reduced contact area at that point. As this contact heating progresses, the work begins to collapse at the contacts, and the heating rate is damped to stability by the increasing area of the

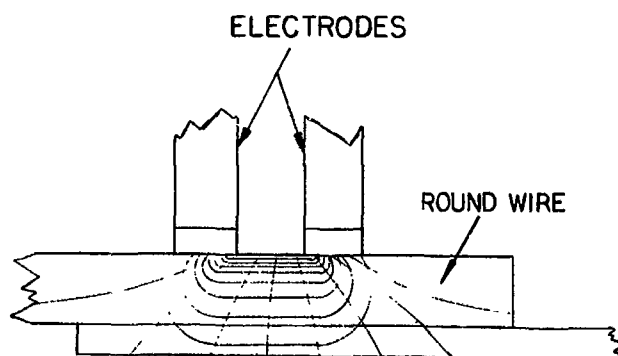


Figure 10-11—Current density in gap welding a round wire.



contacts. If the weld pulse is a constant-voltage pulse and the pressure-voltage adjustment is correct, heating will stabilize to a fixed rate at a temperature just below the plastic range of the work, and the collapse of the round wire will cease. This stable heating will continue until the end of the weld pulse. This time should be long enough to allow good diffusion across the weld interface. This takes place above 100 milliseconds and is characteristic of the diffusion properties of the work (Reference 5). Capacitor discharge welders do not have sufficient pulse width for making diffusion bonds.

### **Lap Welding of Heavy Sections**

Another application of gap welding is lap welding of materials of structural size by the substitution of a high-strength ceramic support such as carborundum for the circuit board shown in Figure 10-1. Figure 10-12 shows a small lap weld being made on carborundum support. This technique may be extended to materials up to, and possibly above, 0.5 cm in size.

### **Planar Gap Welding**

As suggested previously (Reference 6), the gap welding process has been extended into a new design and production technique, termed "planar gap welding" to distinguish it from the well known "swiss cheese" and "dot" concepts. They differ only in the method of interconnecting and in the design technique. The latter two concepts use conventional PW board design techniques and solder for interconnections. However, the planar gap welding technique uses gap welding for interconnections (Figures 10-13 through 10-16) and a straight line, point-to-point layout of the conductors. This concept was adopted with an eye toward computer-controlled design and assembly, which would require only two-dimensional control. Refer to the flight control computer circuit in Figures 10-17 through 10-22; this circuit was designed in the following steps:

1. The electrical schematic is first drawn to scale; actual component outlines are used with the component symbol drawn inside the outline, and all crossovers are disregarded.
2. All crossovers are diverted beneath insulated components or under flying leads of uninsulated components (Figure 10-13) by the most direct path, using straight horizontal and vertical lines. Crossovers that cannot be made this way can be made by using insulated jumpers over a conductor, or through the board and back.
3. The conductor pattern is then defined in heavy lines; this is the preliminary PW board pattern.
4. The dimensions and components are refined, and lead sizes and weld pads are defined.
5. The design is simplified wherever possible.

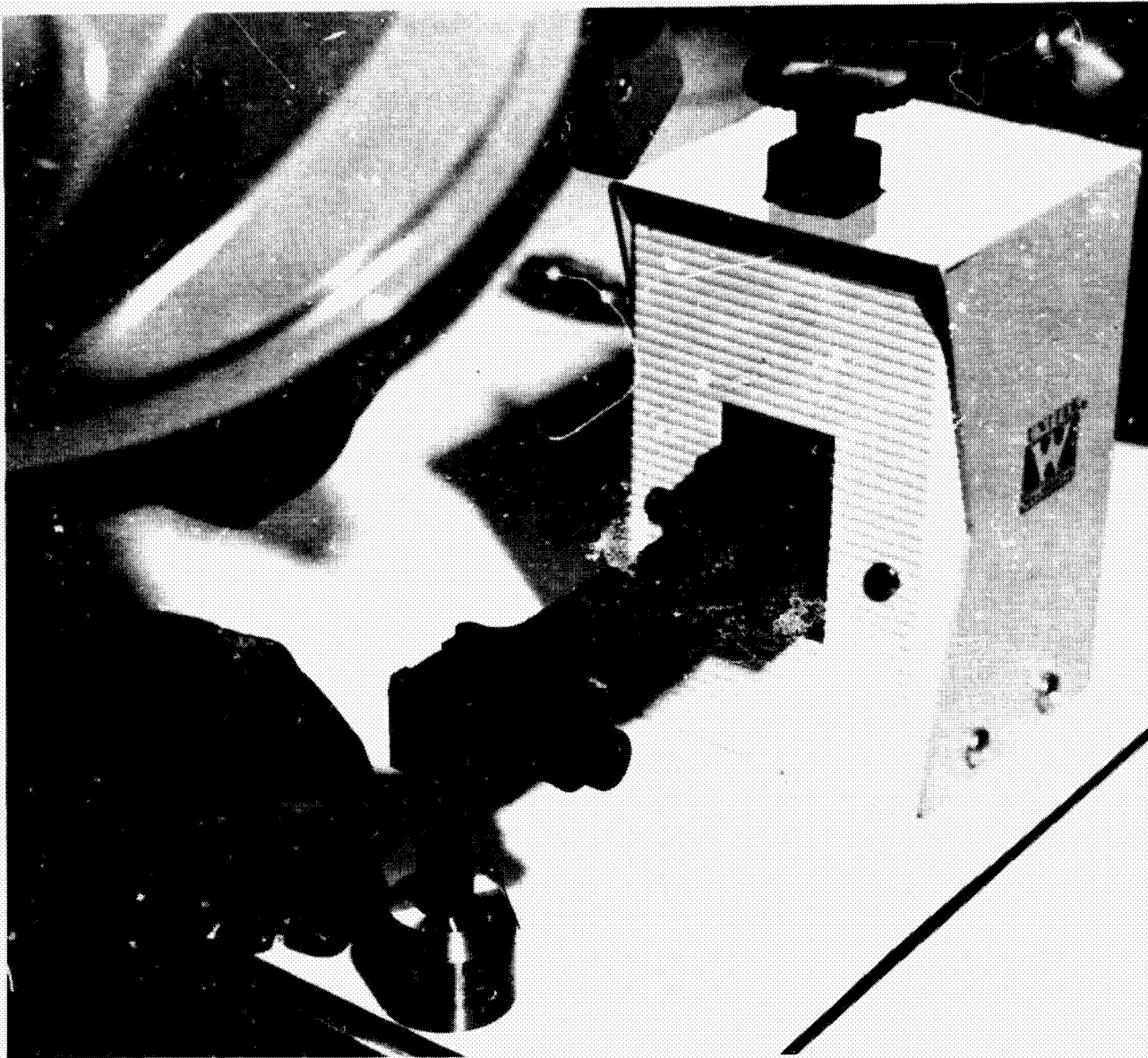


Figure 10-12—Lap welding using a ceramic support.

6. The conductor pattern is defined, and dimensioned drawings are made for coordinagraph cutting of the PW board master.
7. The assembly drawing is made.

Figure 10-13 shows some of the components available for gap welded circuitry.

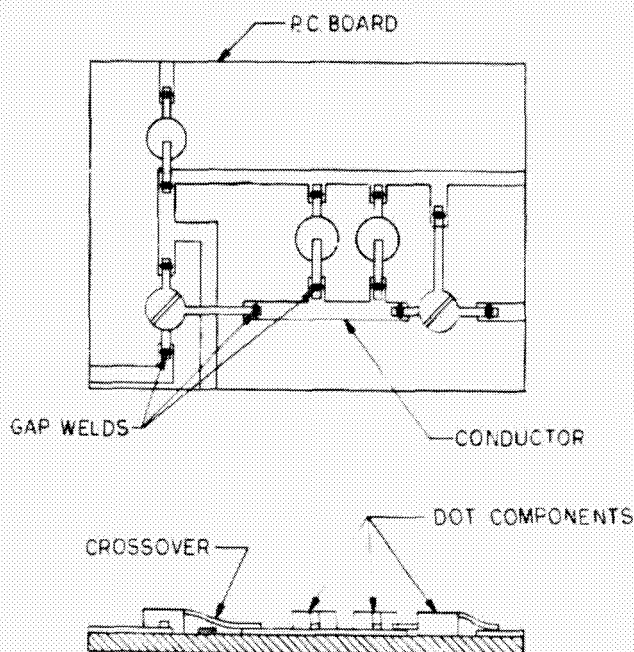


Figure 10-13—Surface mounted dot component.

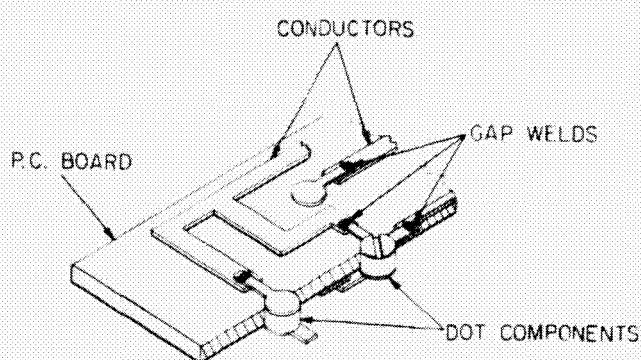


Figure 10-14—Swiss cheese mounting of dot components.

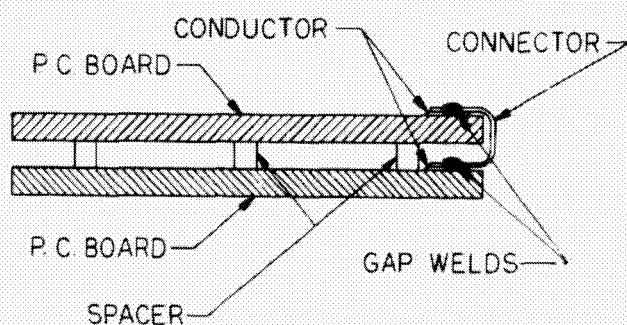


Figure 10-15—Two sides of printed wiring board.

## CONCLUSION

Gap welding, performed under the proper conditions, provides the only metal joint that can be visually inspected for quality. It is a simple and reliable method of interconnecting electronic components and has many other applications which will be developed in the future. Automated microcircuit assembly of welded circuitry by planar gap welding is possible when accurately indexed component packages are available. This process makes assembly a simple two-dimensional problem. The only obstacle in the realization of automated assembly of electronic circuitry by use of this method is the lack of indexing component packages within the needed tolerances to place each lead in position for welding. This has been discussed with a number of manufacturers, and there is some progress in this direction. The flight control computer PW board shown in Figure 10-20 was drilled on a numeric controlled machine to test the feasibility of this approach.

## ACKNOWLEDGMENT

The author wishes to express his appreciation to Mr. L. L. Folsom for his help in making weld tests and establishing welding specifications, and for his helpful suggestions in simplifying the design of the flight control computer.

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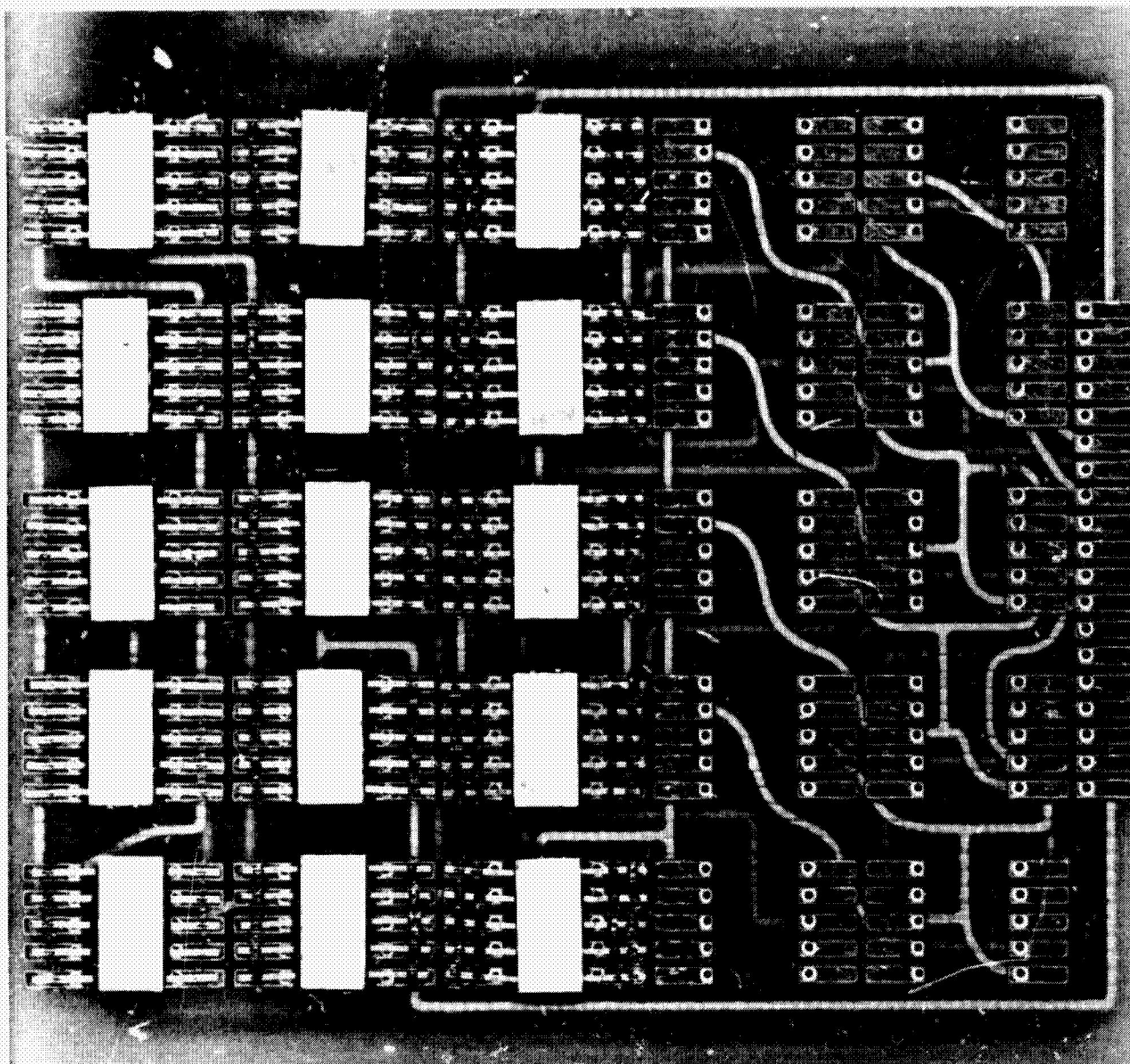


Figure 10-16—Gap welding circuitry.

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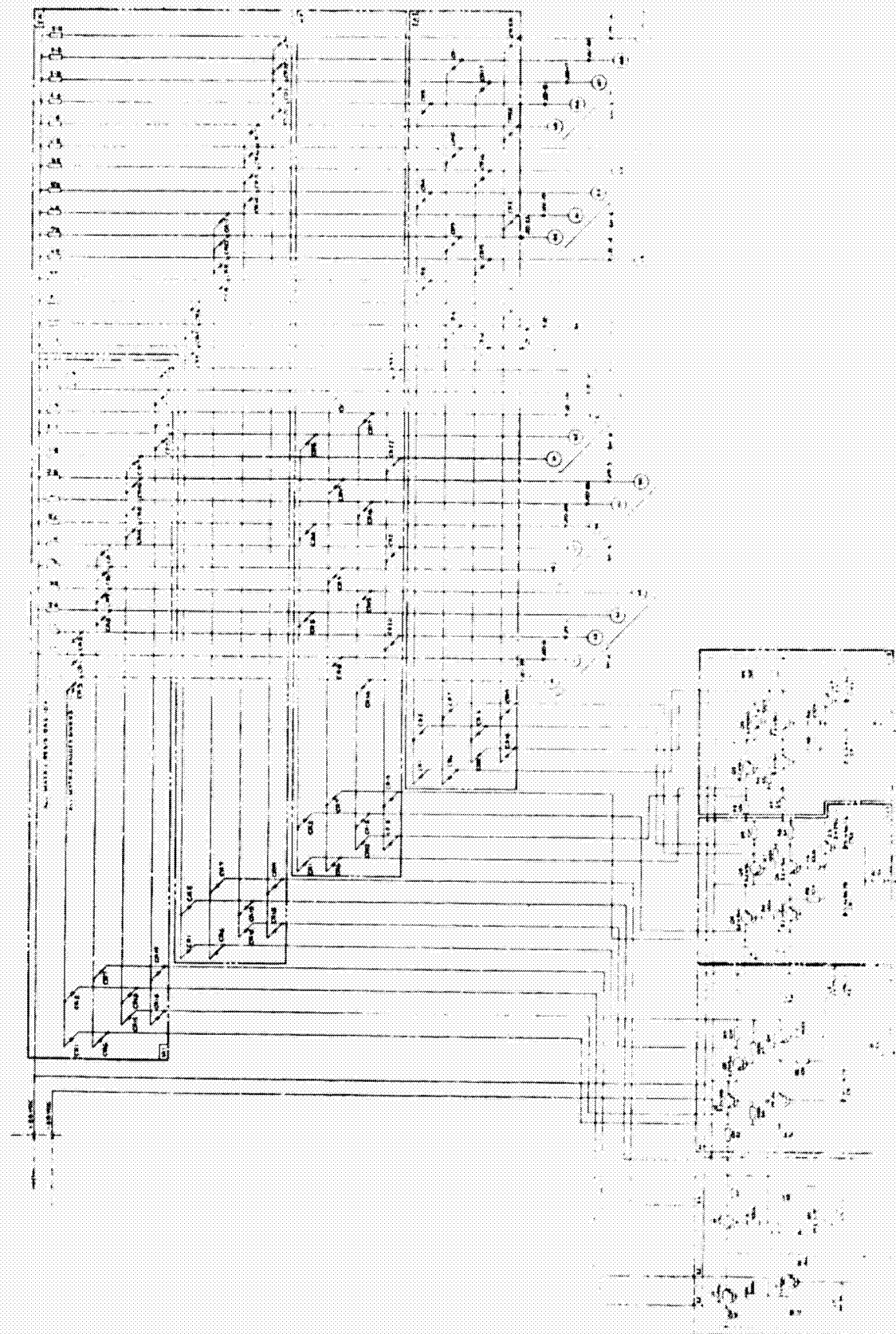


Figure 10-17—Flight control computer, schematic diagram.



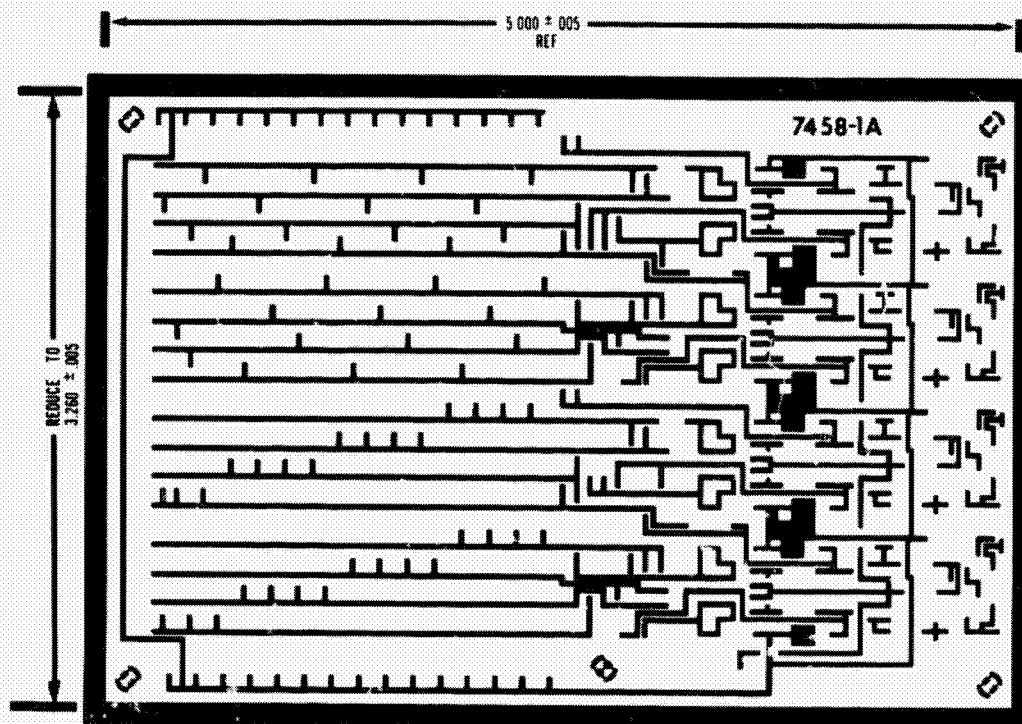


Figure 10-18—Flight control computer P. W. board, sheet 1 of 2.

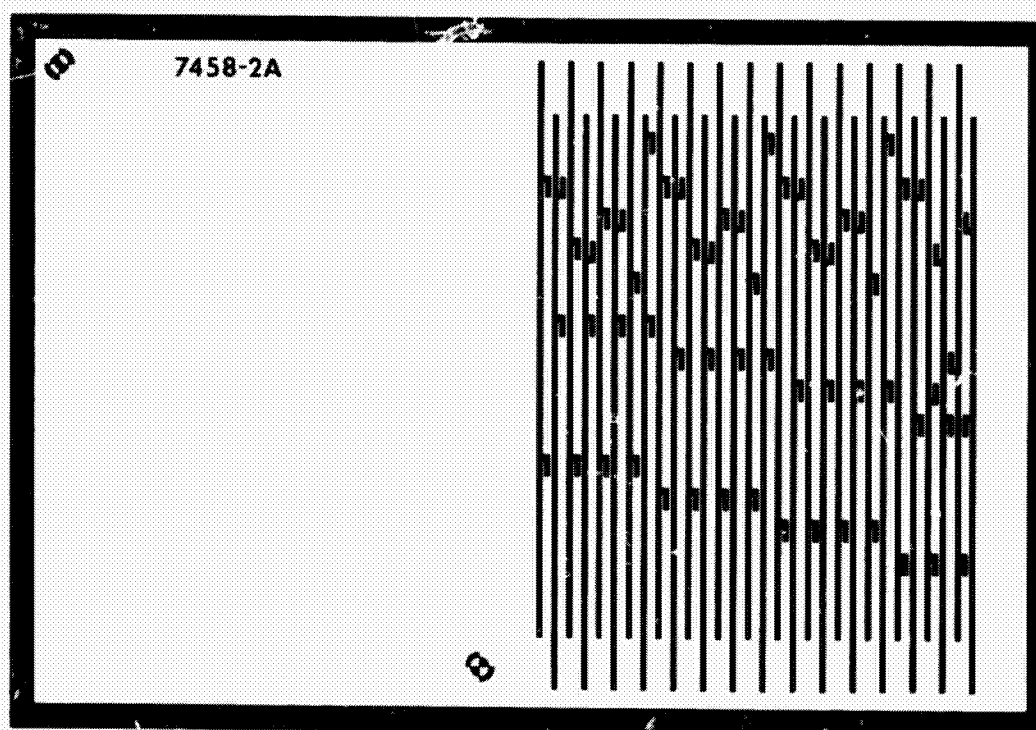


Figure 10-19—Flight control computer P. W. board, sheet 2 of 2.

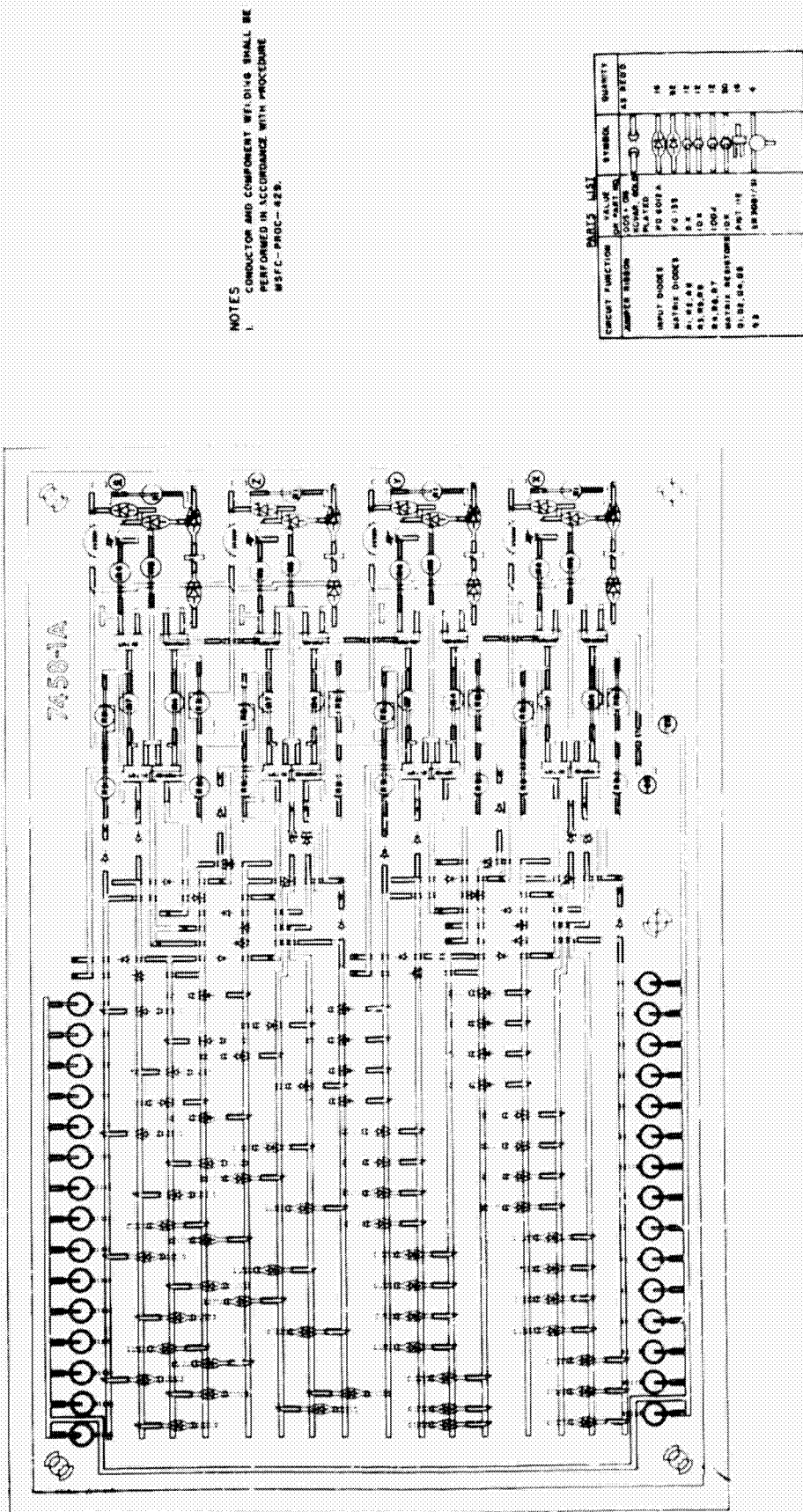


Figure 10-20—Flight control computer circuit assembly drawing, sheet 1 of 2.

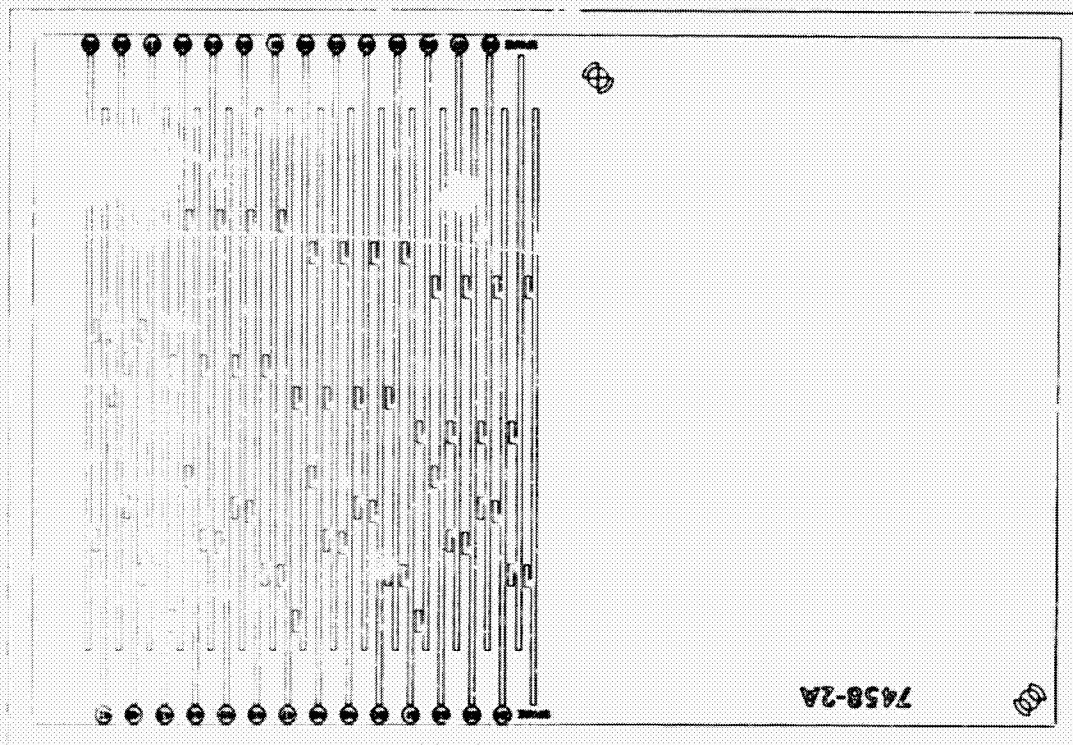


Figure 10-21—Flight control computer circuit assembly, sheet 2 of 2.

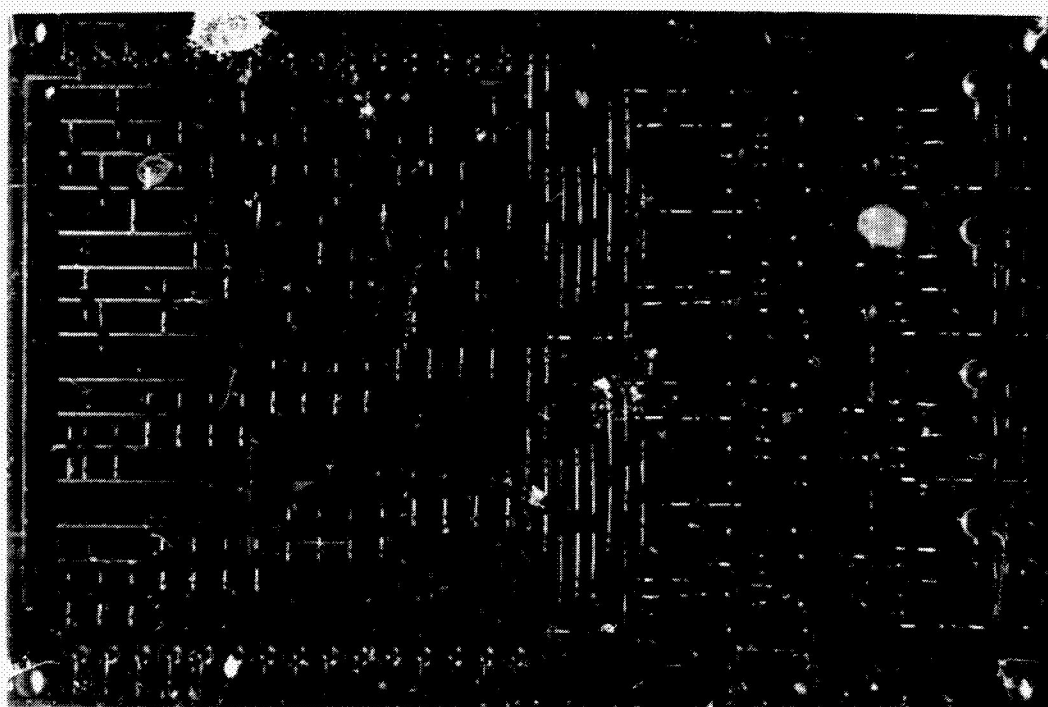


Figure 10-22—Planar gap welded flight control computer.



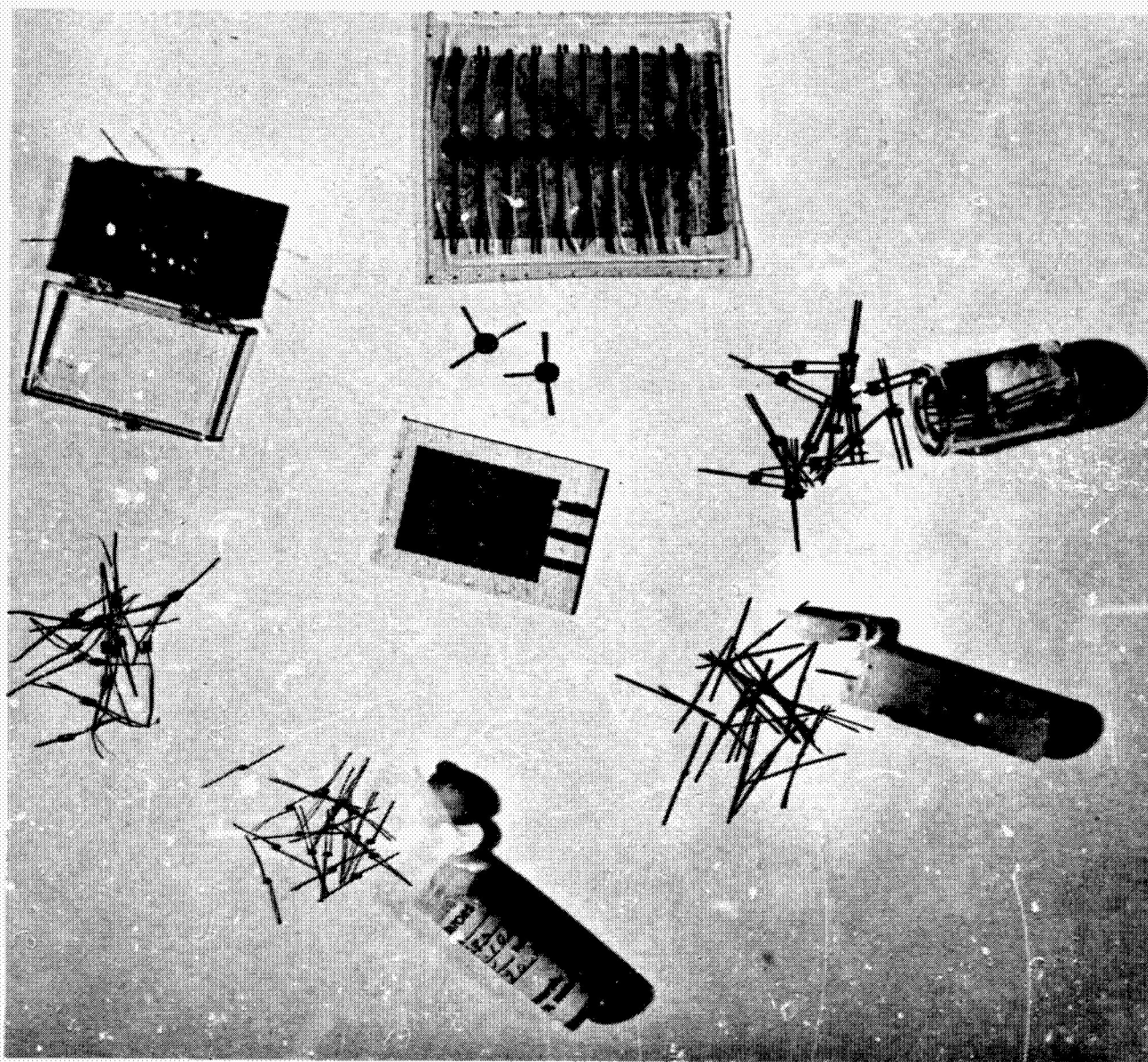


Figure 10-23—Components available for gap welded circuits.

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## 11. PROPERTIES OF VACUUM-DEPOSITED THIN-FILM NICHROME RESISTORS

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Nichrome has certain advantages over other metals and alloys for use in resistors because most others cannot be evaporated from a simple resistance-heated filament. The yield of usable circuits with thin-film nichrome resistors on a production basis is greater than 75 percent. A program which involved producing and testing microminiature circuits using nichrome resistors was carried out to determine the properties of vacuum-deposited nichrome thin-film resistors. This paper describes the methods and procedures used in the fabrication and testing, as well as the resulting characteristics, of these resistors. Test procedures and results are described for both accelerated aging and temperature coefficient of the resistance of the nichrome resistors.

### I. INTRODUCTION

#### General

Currently, a number of techniques and materials can be used for producing resistors in thin-film hybrid microelectronic circuits. The relative merits of the different methods and the selection of materials for fabricating thin-film resistors depend on the properties required of the component—tolerance, power dissipation, available area, resistivity, etc. Although data are available stating the general characteristics of thin-film resistors produced by current methods, details are lacking on individual device performance.

The structure of metal films vacuum-deposited on a substrate has been studied in great detail within the past 10 years. It has been generally agreed that the vaporized metal strikes the condensing surface and tends to form nuclei. Additional vapor condensing on the substrate grows and crystallizes from the nucleation sites into "islands." The "islands" join together as the metal thickness increases. The thinner films have greater voids between nucleation sites. Deposition conditions, residual gas pressure, substrate cleanliness, and surface roughness influence to some extent the growth of thin films. The thickness of the film determines the electrical properties to some degree.

## Property Requirements For Thin-Film Resistors

Certain properties are required for an ideal thin-film resistor. The device must be stable when exposed to elevated temperature, stored for long periods, and operated continuously. Desired requirements are a low temperature coefficient of resistance (TCR), a practical sheet resistivity, good adherence to substrate surface, and the ability to be manufactured by standard vacuum-deposition techniques.

### Nichrome Metal

No single material has been found that meets all the requirements exactly. However, nichrome metal (80 percent nickel, 20 percent chromium) has been used more extensively than any other single material for resistive films. In addition, nichrome possesses the desired properties required for most thin-film circuit applications. A program was carried out in the Microelectronics Unit laboratory to determine the properties of vacuum-deposited nichrome thin-film resistors. Numerous prototype microminiature circuits using nichrome resistors have been produced and tested successfully in this laboratory. Characteristics of the thin-film nichrome resistors used in these circuits are described.

## II. FABRICATING THIN-FILM NICHROME RESISTORS

### Test Pattern

Thin-film nichrome resistors were fabricated for testing by vacuum evaporating the bulk metal from a resistance-heated tungsten filament. The vacuum disposition cycle was conducted at a pressure range of  $10^{-4}$  N/m<sup>2</sup> ( $10^{-6}$  torr). Layout of the resistor pattern is shown in Figure 11-1 and resistor values are listed in Table 11-1. Resistors 1 through 11 were coated with a vapor-deposited layer of silicon monoxide approximately 2000 Å thick. The surfaces of resistors 12 through 22 were left unprotected.

### Resistor Configuration

The order in which material was deposited on the substrate and the resistor configuration

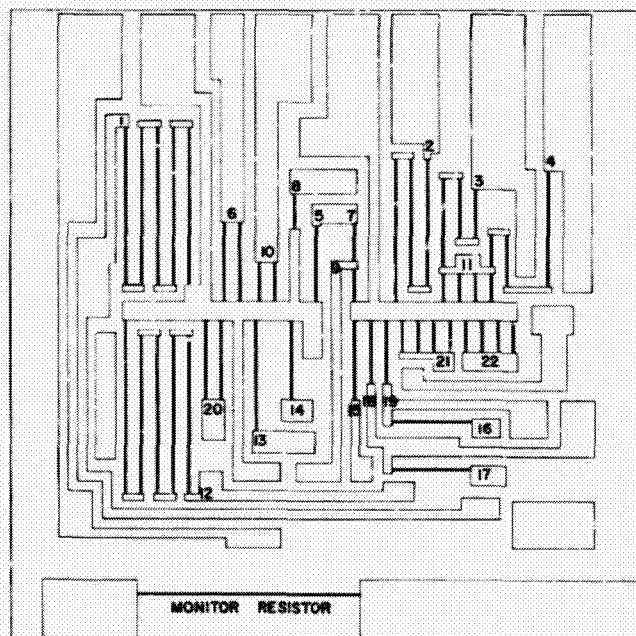


Figure 11-1—Pattern layout of thin-film test resistors.

Table 11-1

## Resistor Values

Resistor no.	Resistor values — k ohms		
	100 ohms/sq	200 ohms/sq	300 ohms/sq
1	50	100	250
2	25	50	25
3	12.5	25	62.5
4	12.5	25	62.5
5	4.76	9.53	23.8
6	2.5	5	12.5
7	2.32	4.64	11.83
8	2.21	4.42	11
9	2.01	4.02	10
10	1.25	2.5	6.25
11	0.43	0.86	2.15
12	50	100	250
13	7	14	35
14	5	10	25
15	5	10	25
16	5	10	25
17	5	10	25
18	4	8	20
19	4	8	20
20	2.5	5	12.5
21	0.5	1	2.5
22	0.5	1	2.5

are depicted in Figure 11-2. The substrate is processed initially by having contact pads applied. The pad pattern is applied by screen printing with Du Pont 7713 silver-conductive paste; the paste is metallized by firing to 610° C for 20 minutes. All resistors are 0.012 cm wide.

## Substrates

Two types of substrate material were used for the thin-film resistors—glass and glazed ceramic. The ceramic substrate, Alsimag 614 manufactured by the American Lava Corporation, is 0.05 cm thick, 0.9 cm square and has a 1-microinch glaze finish on one side. The glass substrate is 0.4 mm thick, 0.9 cm square; designated Corning 7059 electronic grade glass, it is



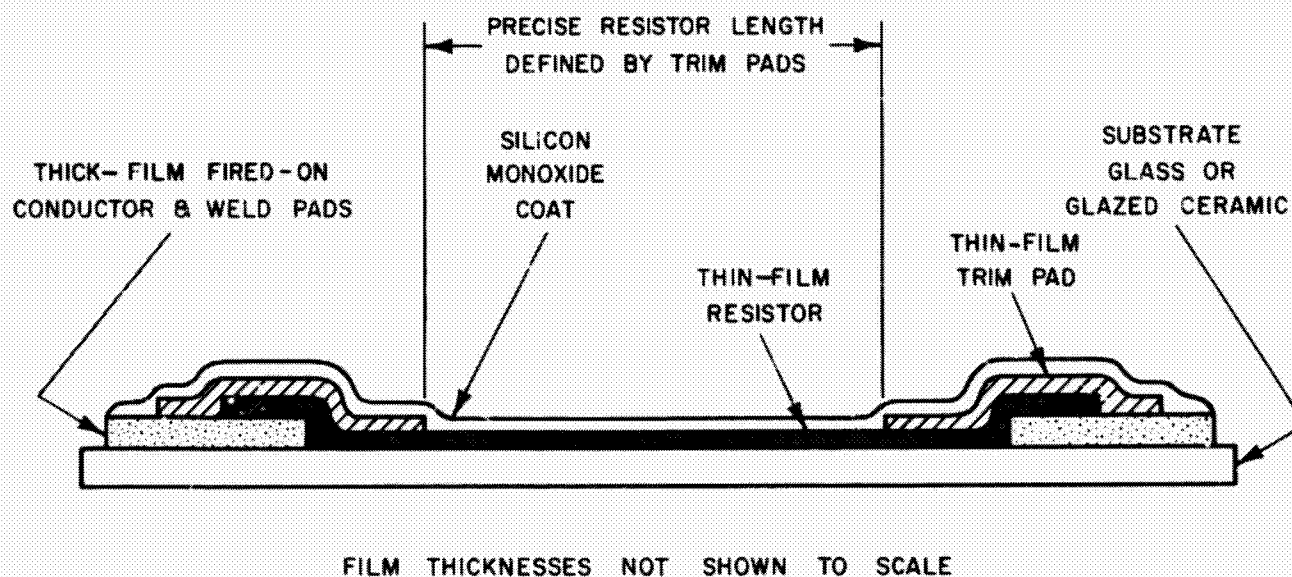


Figure 11-2—Cross section of thin-film resistor configuration.

manufactured by Corning Glass. These two materials are typical of the substrates currently used for hybrid microelectronic circuits.

### Thin-Film Deposition

The thin films were vapor deposited in a vacuum system at a pressure range of  $10^{-4}$  N/m<sup>2</sup>. The substrates were maintained at  $225^{\circ} \pm 5^{\circ}$  C during deposition. The contact method with precision metal masks was used to form the thin-film patterns on the substrate. Gold was used for thin-film conductor lines and resistor trim pads. Silicon monoxide was vapor-deposited over half the resistors on each substrate as a protective coating.

### Sheet Resistivities

The nichrome films were deposited with sheet resistivities of 100, 200, and 500 ohms per square. The resistivity was controlled by measuring the resistance of a monitor film on the substrate during the evaporation process. The thicknesses of the gold and silicon monoxide were monitored during deposition with a crystal oscillator thickness monitor. The monitor resistor is shown in Figure 11-1 in the lower edge of the substrate. The resistivity values represent the range used generally for nichrome thin-film resistors. The 100 and 200 ohms per square values are the most commonly used in circuitry applications. The maximum usable resistivity value for nichrome has been reported at 300 ohms per square. However, 500 ohms per square was chosen for these experiments to determine if the usable range could be extended for higher-than-normal resistor values, when required.

### III. ACCELERATED AGING OF RESISTORS

#### Test Procedure

The aging stability of the thin-film resistors was determined by storing them in a standard laboratory oven with a normal air atmosphere. The temperature range of the oven was 38° to 288° C. The resistors were measured prior to storage in the oven and were removed periodically to have the change in resistance measured. The substrates were allowed to stabilize at room temperature before resistance measurements were made. A group of control resistors were stored at room temperature for comparison with the accelerated-age devices. Measurements were made on a digital volt-ohmmeter which has four significant digits and manual range selection and is capable of measuring 0.0001 to 999 kilohms,  $\pm 1$  count in the last digit. A test apparatus consisting of a holding fixture and switching box was used to mount the substrate while measuring the resistors. The apparatus is shown in Figure 11-3. Wire springs were mounted in an insulated block to form contacts to the termination pads of each resistor on the substrate. Measurements were made by switching to the desired pair of contact points.

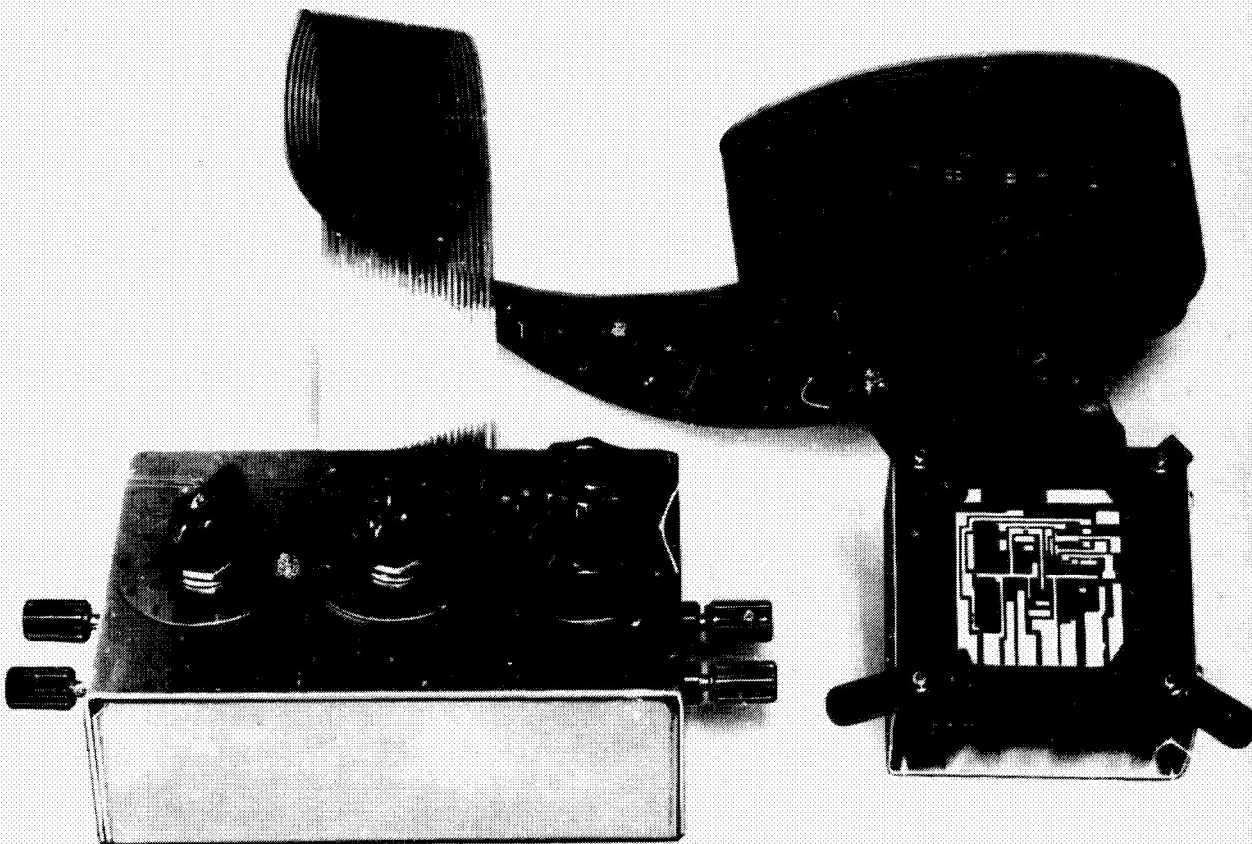


Figure 11-3—Test substrate holding fixture and switch box.

## Test Results

The data derived from the accelerated aging tests are summarized in Tables 11-2 through 11-7. The resistance change represents the average value of the resistors on a single substrate. The average change in resistance as a function of time for the test substrates is shown in Figures 11-4 through 11-33. Each figure contains two curves—one for the resistors protected with silicon monoxide and the other for the unprotected resistors.

1. Resistors Protected with Silicon Monoxide. Evaluation of the elevated temperature aging data shows that all of the resistors protected with silicon monoxide exhibited excellent stability up to the maximum test temperature of 198° C. No significant differences existed in the performance of resistors deposited on either glass or ceramic substrates.
2. Unprotected Resistors. The uncoated resistors oxidized and increased in resistance at a rate dependent on the storage temperature. As the figures show, the resistors changed continually, but the rate of change decreased with storage time. The oxidation layer apparently provided some protection as the thickness increased. However, the oxide layer will not protect the nichrome from continual oxidation. These resistors, as experienced by this laboratory and other investigators (Reference 1), will increase in value until a complete breakdown of the film continuity occurs.

Table 11-2

Accelerated Aging Characteristics of 100-ohms-per-square Nichrome Resistors  
on Glass Substrates

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested	10	11	9	11	10	11	10	11	9	11	10	11
Total aging time, T-hours	4032	4032	137	137	137	137	280	280	115	115	139.5	139.5
Average percent change after T-hours	0.43	0.10	0.47	0.05	-0.02	-0.82	1.70	0.22	1.57	0.30	6.80	0.45
Standard deviation of percent change	0.20	0.11	0.31	0.07	0.77	1.50	0.22	0.08	0.22	0.10	3.40	0.91
Reference number:												
Substrate	1,2,3	1,2,3	7	7	9	9	11	11	13	13	15	15
Figure	4	4	6	6	8	8	10	10	12	12	14	14
Page	26	26	28	28	30	30	32	32	34	34	36	36

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 100-ohms-per-square film 15 Å.



Table 11-3

**Accelerated Aging Characteristics of 100-ohms-per-square Nichrome Resistors  
on Glazed Ceramic Substrates**

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested	10	11	11	11	11	11	11	11	11	11	no sample	
Total aging time, T-hours	300	3672	137	137	137	137	280	280	115	115		
Average percent change after T-hours	2.44	0.14	0.34	0.04	0.84	-0.03	0.0	0.03	1.75	0.19		
Standard deviation of percent change	0.30	0.06	0.05	0.10	0.19	0.30	0.15	0.06	0.26	0.09		
Reference number:												
Substrate	4,5,6	4,5,6	8	8	10	10	12	12	14	14		
Figure	5	5	7	7	9	9	11	11	13	13		
Page	27	27	29	29	31	31	33	33	35	35		

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 100-ohms-per-square film 150 Å.

Table 11-4

**Accelerated Aging Characteristics of 200-ohms-per-square Nichrome Resistors  
on Glass Substrates**

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested	10	11	8	11	9	10	9	11	8	11	6	10
Total aging time, T-hours	4008	4008	137	137	137	137	280	280	115	115	139.5	139.5
Average percent change after T-hours	3.00	0.13	0.79	0.04	1.49	0.27	4.60	0.78	5.50	0.29	18.70	0.89
Standard deviation of percent change	0.37	0.06	0.13	0.05	0.12	0.48	0.62	0.31	0.83	0.23	8.70	1.60
Reference number:												
Substrate	1,2,3	1,2,3	16	16	18	18	20	20	22	22	24	24
Figure	4	4	15	15	17	17	19	19	21	21	23	23
Page	26	26	37	37	39	39	41	41	43	43	45	45

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 200-ohms-per-square film 75 Å.

Table 11-5

**Accelerated Aging Characteristics of 200-ohms-per-square Nichrome Resistors  
on Glazed Ceramic Substrates**

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested			11	11	11	11	11	11	10	10	10	11
Total aging time, T-hours	3768	3768	137	137	137	137	280	280	115	115	139.5	139.5
Average percent change after T-hours	2.90	0.17	0.47	0.04	0.23	-0.02	3.80	0.08	4.10	0.17	15.5	0.57
Standard deviation of percent change	0.34	0.08	0.05	0.07	0.23	0.21	0.20	0.07	0.53	0.10	4.20	0.36
Reference number:												
Substrate	4,5,6	4,5,6	17	17	19	19	21	21	23	23	25	25
Figure	5	5	16	16	18	18	20	20	22	22	24	24
Page	27	27	38	38	40	40	42	42	44	44	46	46

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 200-ohms-per-square film 75 Å.

Table 11-6

**Accelerated Aging Characteristics of 500-ohms-per-square Nichrome Resistors  
on Glass Substrates**

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested	11	10	8	11			7	10	8	11	10	
Total aging time, T-hours	3860	3860	137	137	no sample		280	280	115	115	139.5	139.5
Average percent change after T-hours	5.50	0.47	2.40	0.02			10.10	0.09	9.10	0.08	25.0	-0.06
Standard deviation of percent change	0.26	0.16	0.12	0.01			0.74	0.14	0.70	0.18	10.0	0.28
Reference number:												
Substrate	1,2,3	1,2,3	26	26			29	29	31	31	33	33
Figure	4	4	25	25			28	28	30	30	32	32
Page	26	26	47	47			50	50	52	52	54	54

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 500-ohms-per-square film 30 Å.

Table 11-7

**Accelerated Aging Characteristics of 500-ohms-per-square Nichrome Resistors  
on Glazed Ceramic Substrates**

Aging temperature, °C	RT	RT	50	50	90	90	125	125	152	152	198	198
Protective coating	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO	none	SiO
Number resistors tested			11	11	9	10	11	9	11	11	10	10
Total aging time, T-hours	3744	3744	137	137	137	137	280	280	115	115	139.5	139.5
Average percent change after T-hours	10.5	0.14	1.30	0.01	8.00	0.15	9.10	0.26	9.00	0.04	38.50	-4.50
Standard deviation of percent change	0.87	0.24	0.17	0.03	2.00	0.28	0.10	0.24	0.68	0.20	9.20	2.60
Reference number												
Substrate	4,5,6	4,5,6	27	27	28	28	30	30	32	32	34	34
Figure	5	5	26	26	27	27	29	29	31	31	33	33
Page	27	27	48	48	49	49	51	51	53	53	55	55

Notes: 1. RT: Control resistors stored at ambient room temperature of approximately 25°C.  
2. Approximate thickness of 500-ohms-per-square film 30 Å.

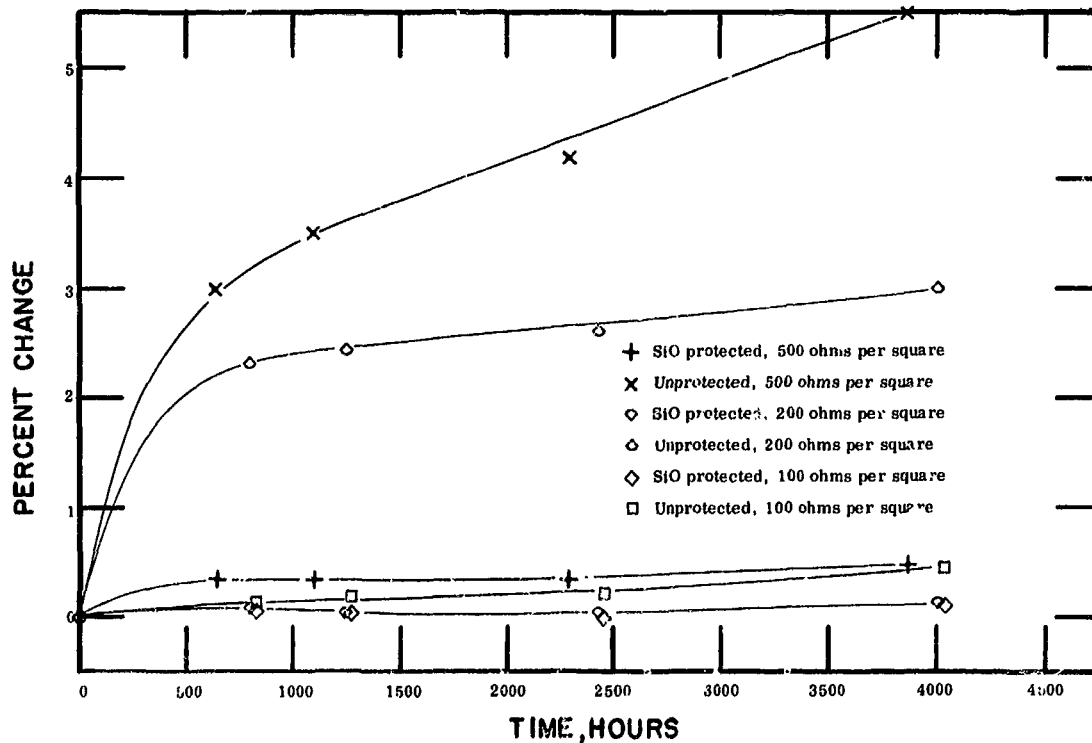


Figure 11-4—Substrates 1, 2, and 3—Average change in resistance of 100, 200, and 500-ohms-per-square control resistors deposited on glass.

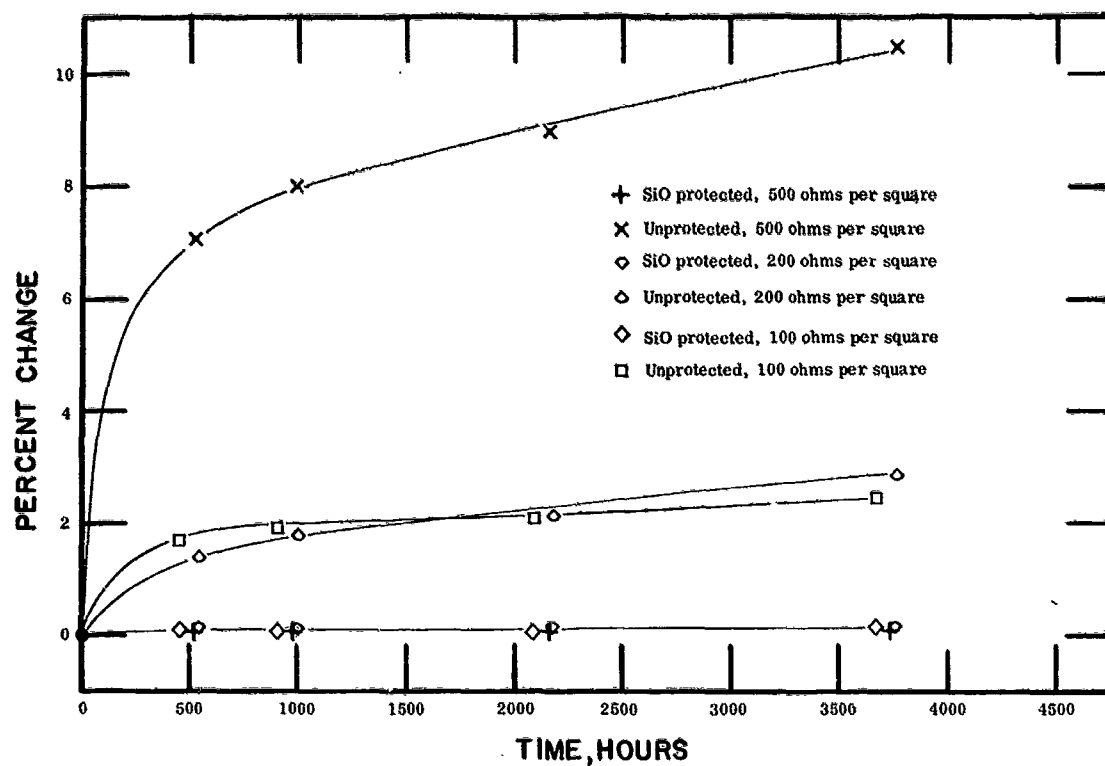


Figure 11-5—Substrates 4, 5, and 6—Average change in resistance of 100, 200, and 500-ohms-per-square control resistors deposited on glazed ceramic.

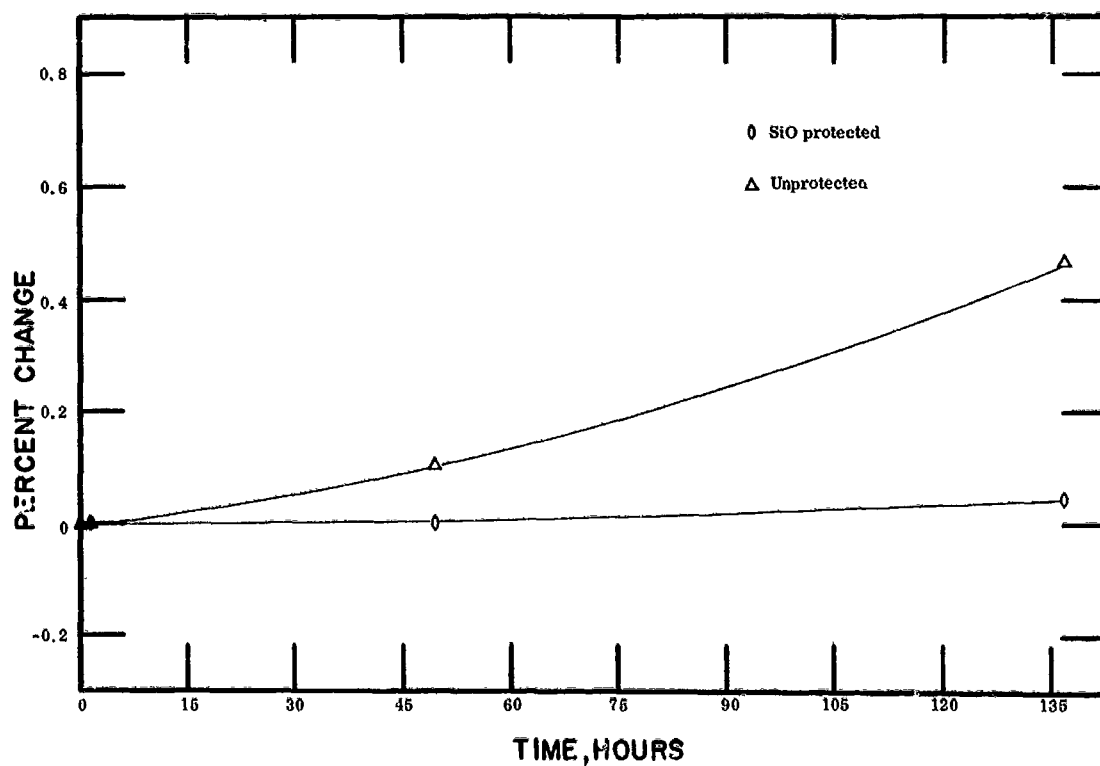


Figure 11-6—Substrate 7—Average change in resistance of 100-ohms-per-square resistors deposited on glass and aged at 50°C.

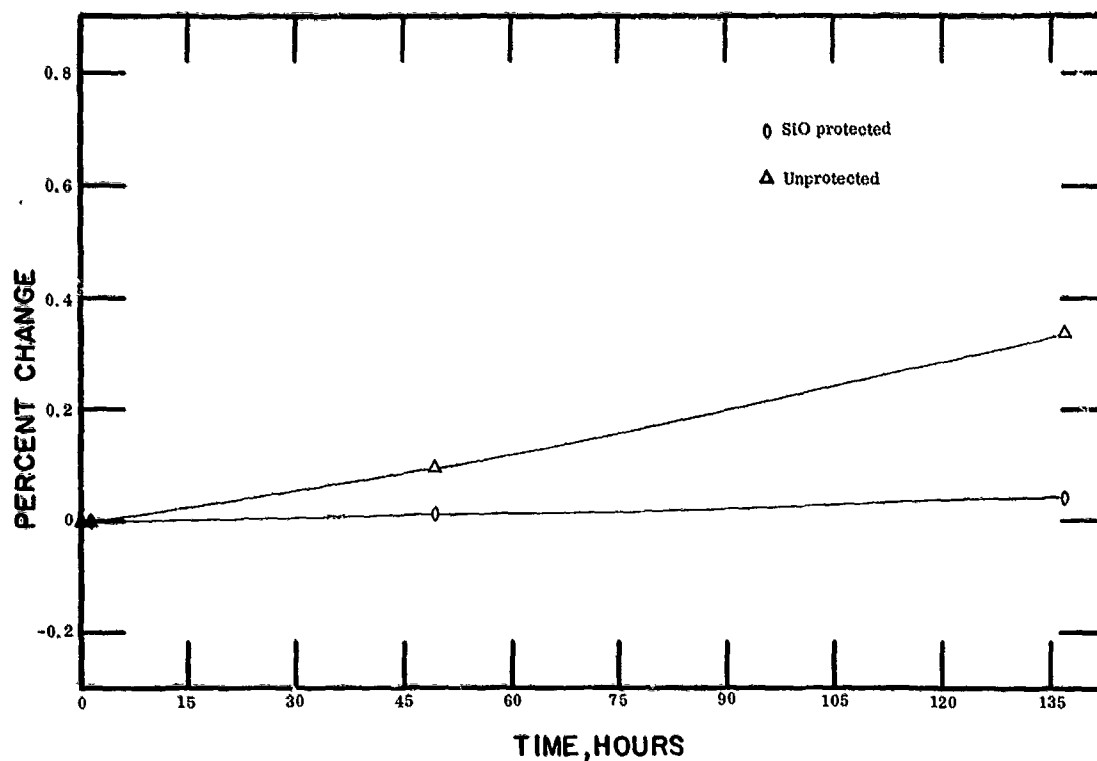


Figure 11-7—Substrate 8—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic and aged at 50°C.

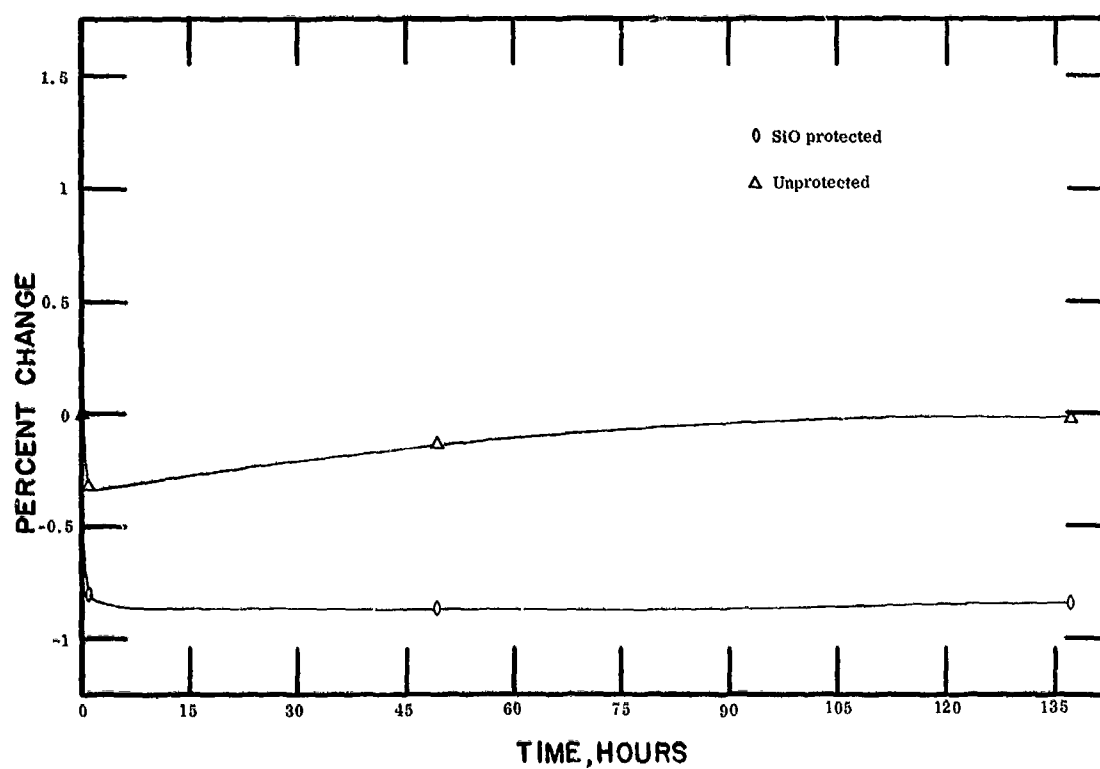


Figure 11-8—Substrate 9—Average change in resistance of 100-ohms-per-square resistors deposited on glass and aged at 90°C.

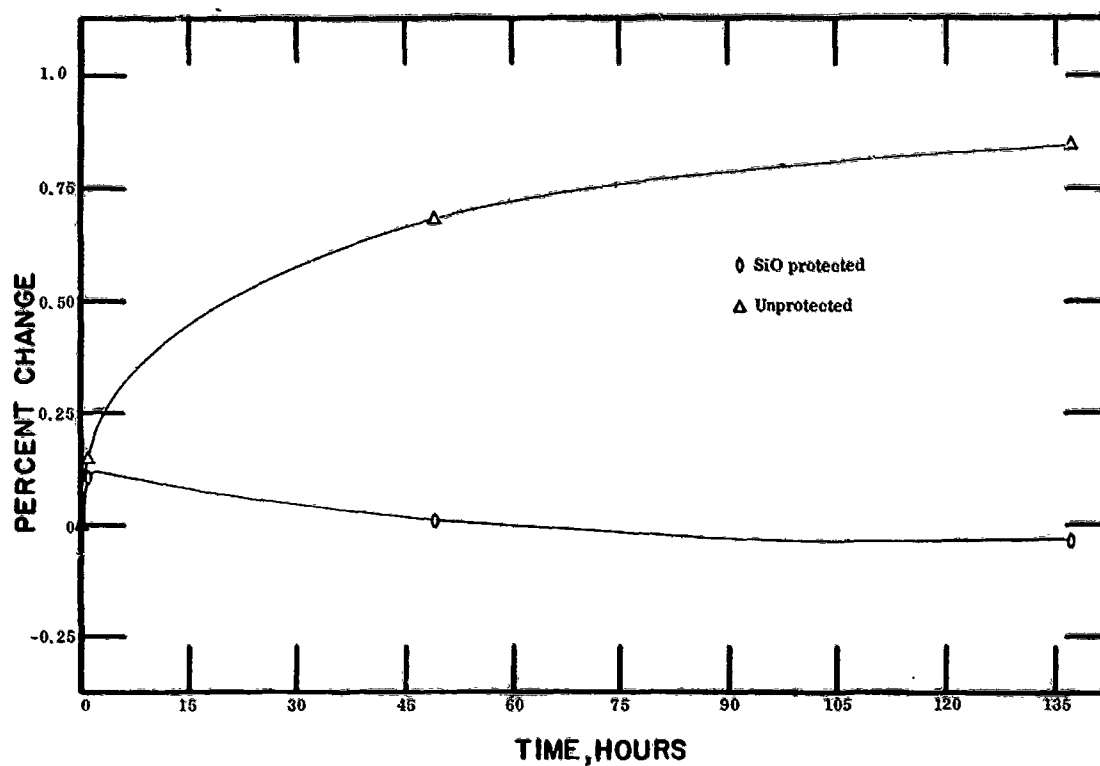


Figure 11-9—Substrate 10—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic and aged at 90°C.

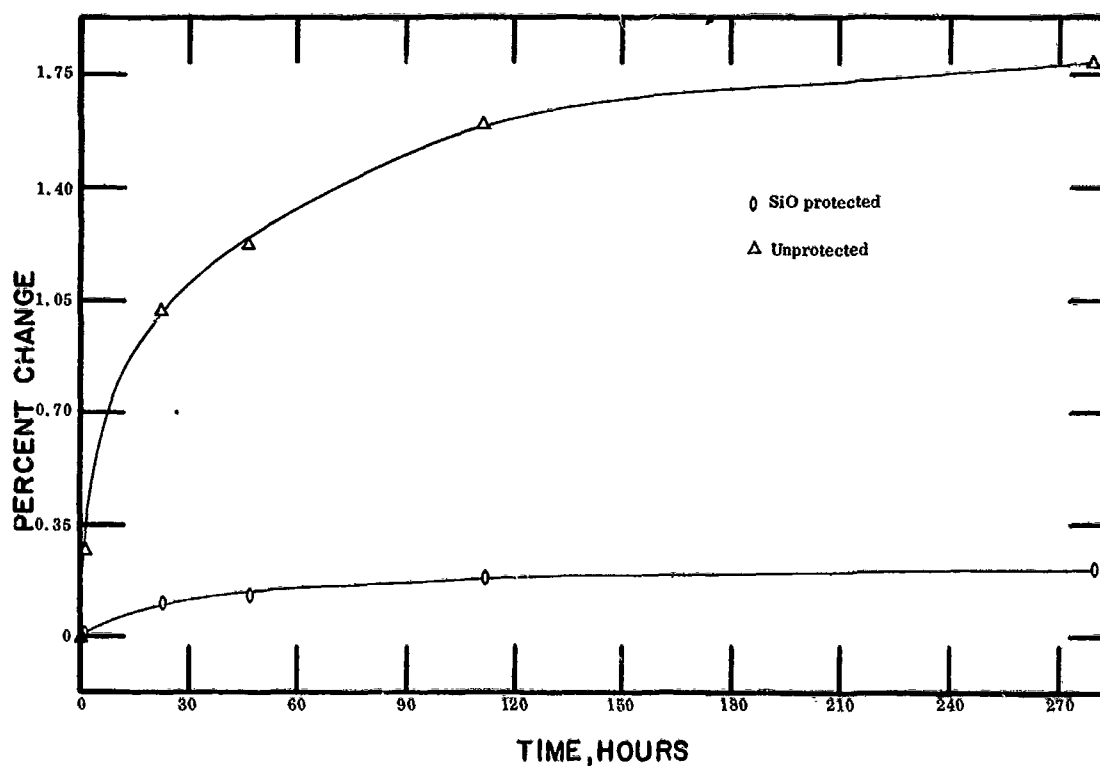


Figure 11-10—Substrate 11—Average change in resistance of 100-ohms-per-square resistors deposited on glass and aged at 125°C.

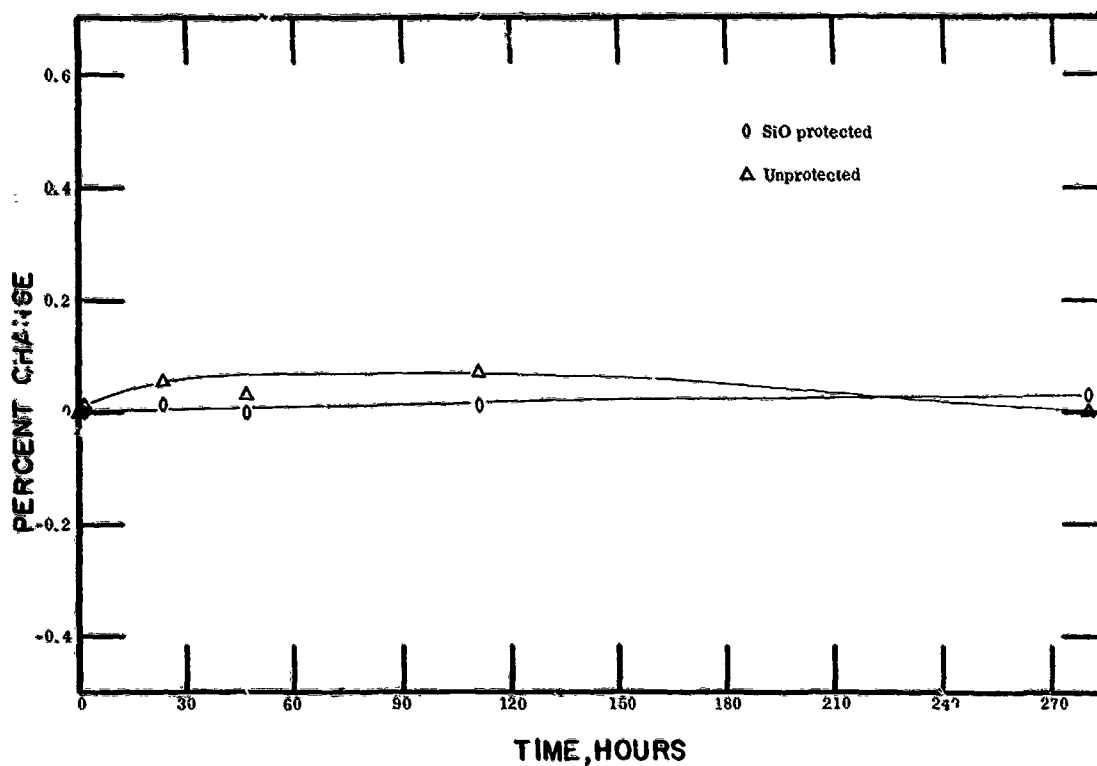


Figure 11-11—Substrate 12—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic and aged at 125°C.

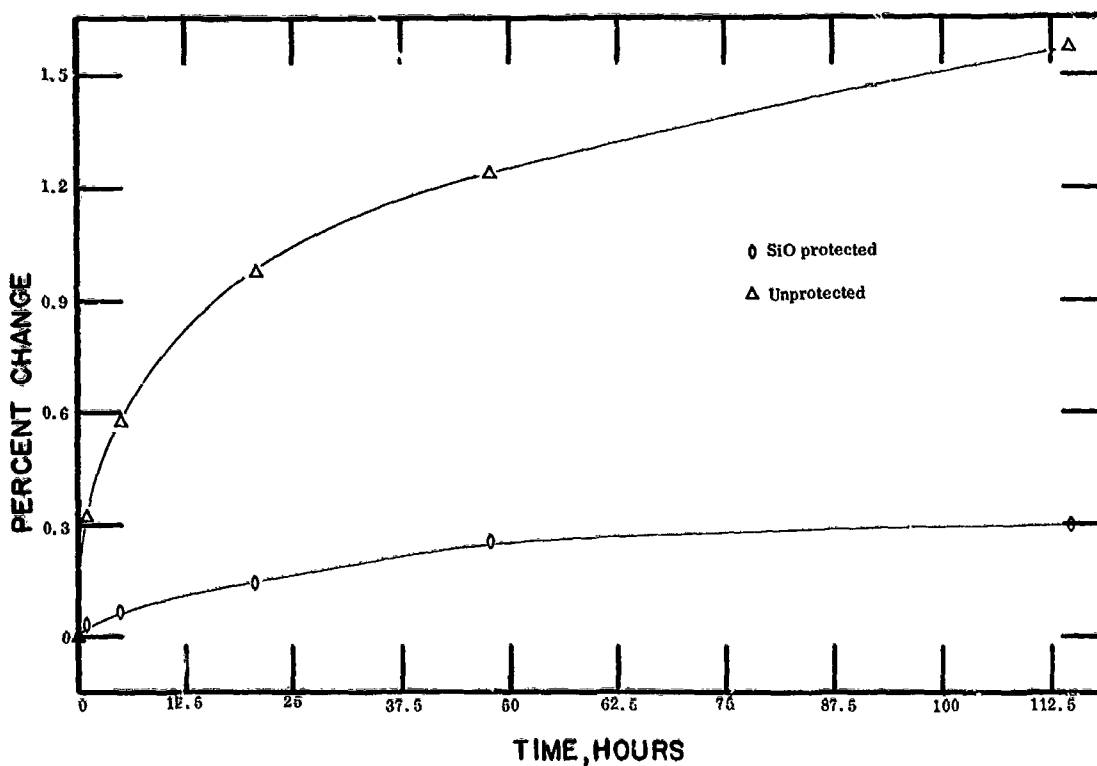


Figure 11-12—Substrate 13—Average change in resistance of 100-ohms-per-square resistors deposited on glass and aged at 152°C.

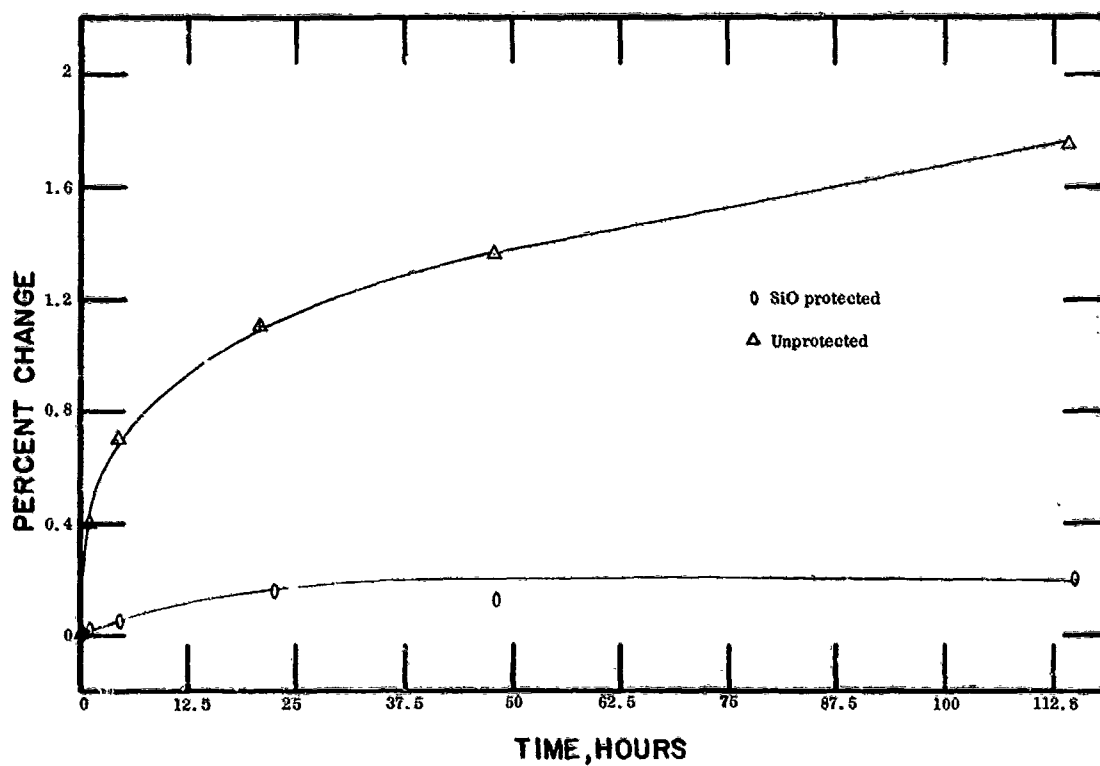


Figure 11-13—Substrate 14—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic and aged at 152°C.

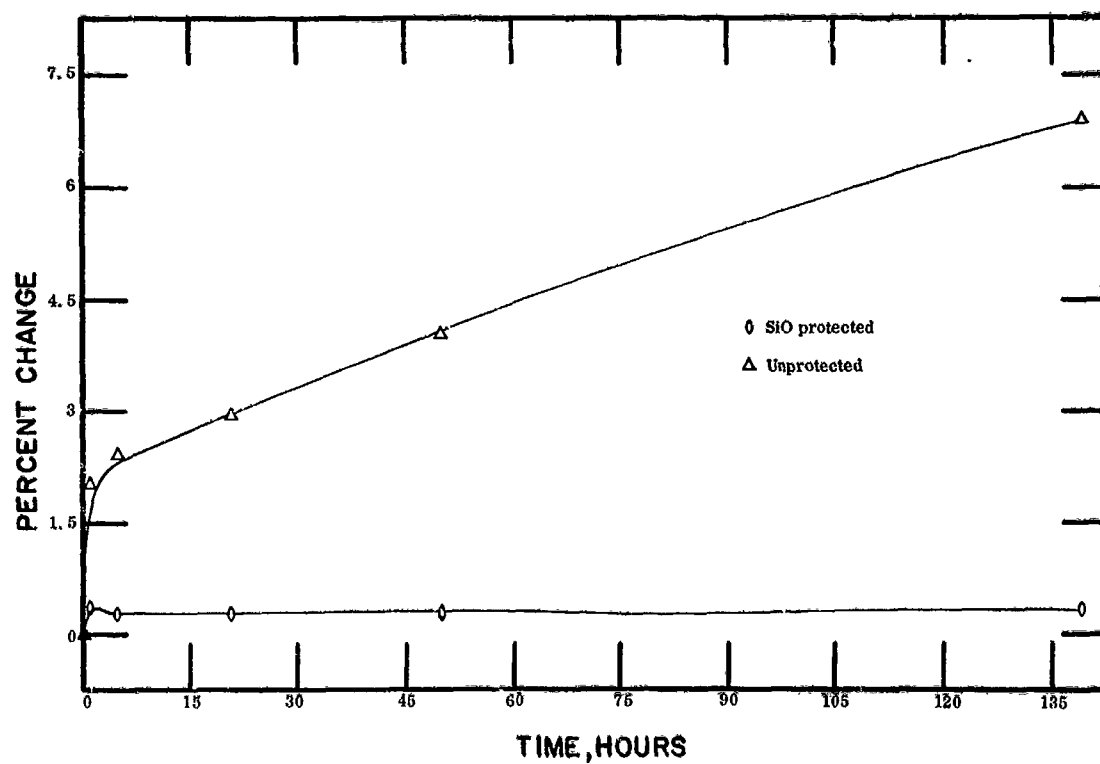


Figure 11-14—Substrate 15—Average change in resistance of 100-ohms-per-square resistors deposited on glass and aged at 198°C.



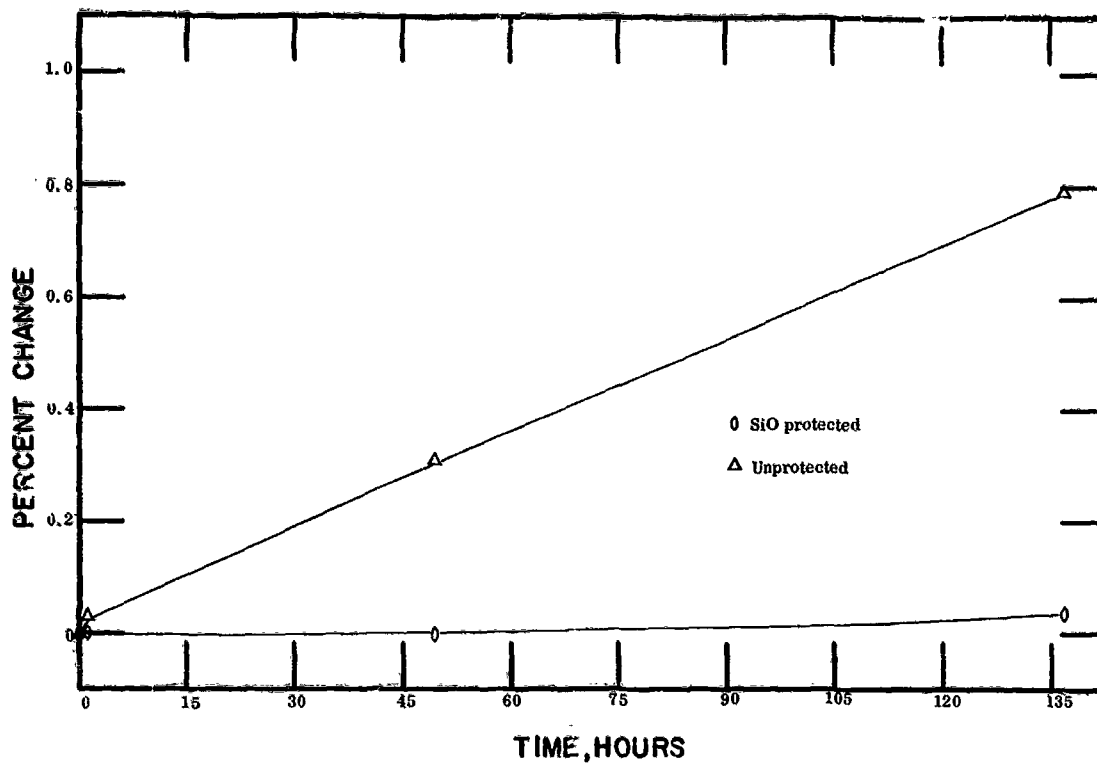


Figure 11-15—Substrate 16—Average change in resistance of 200-ohms-per-square resistors deposited on glass and aged at 50°C.

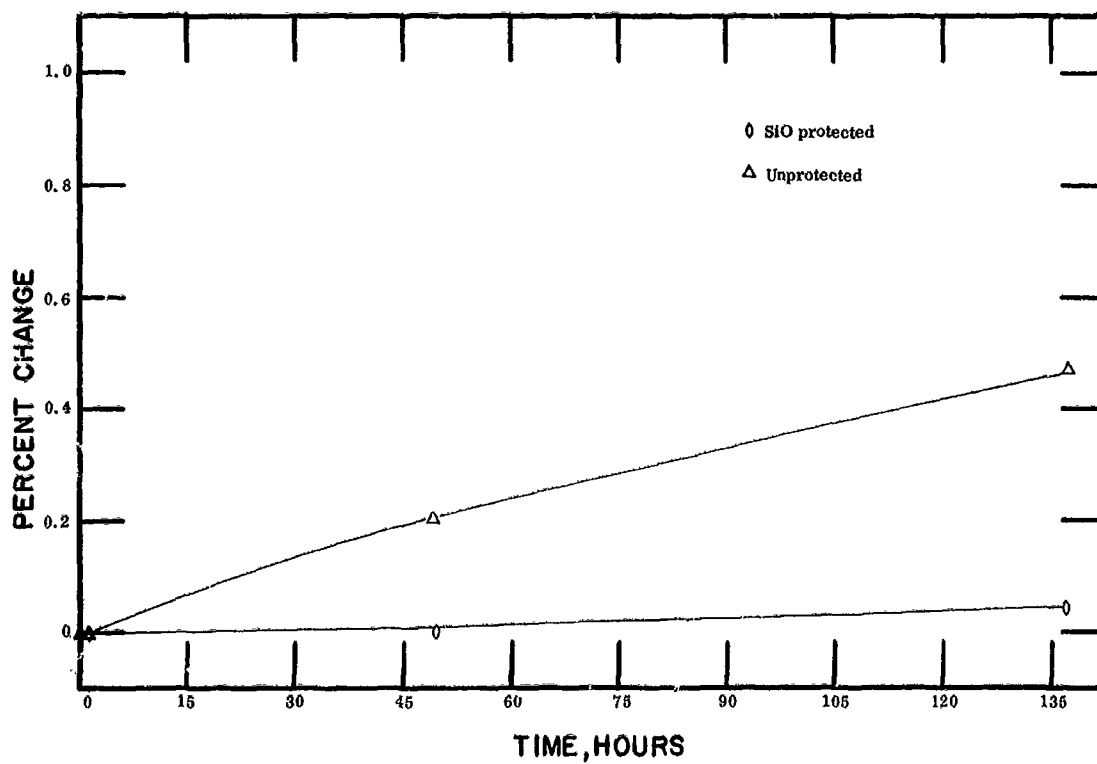


Figure 11-16—Substrate 17—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic and aged at 50° C.

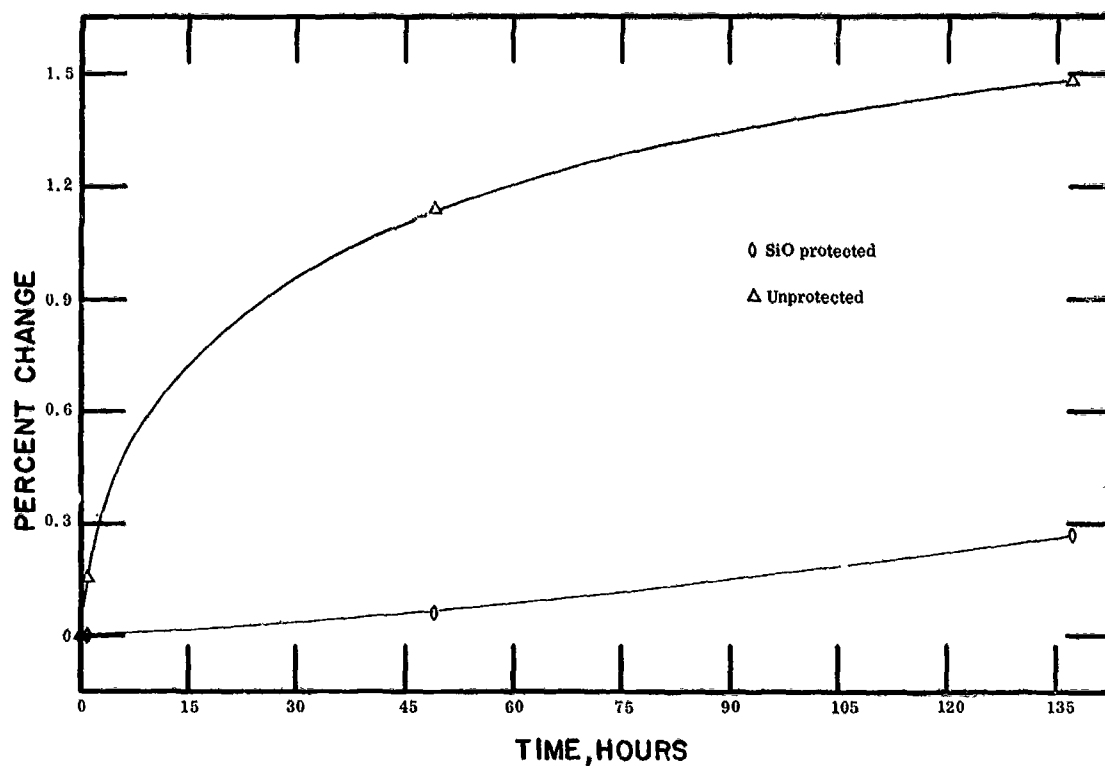


Figure 11-17—Substrate 18—Average change in resistance of 200-ohms-per-square resistors deposited on glass and aged at 90°C.

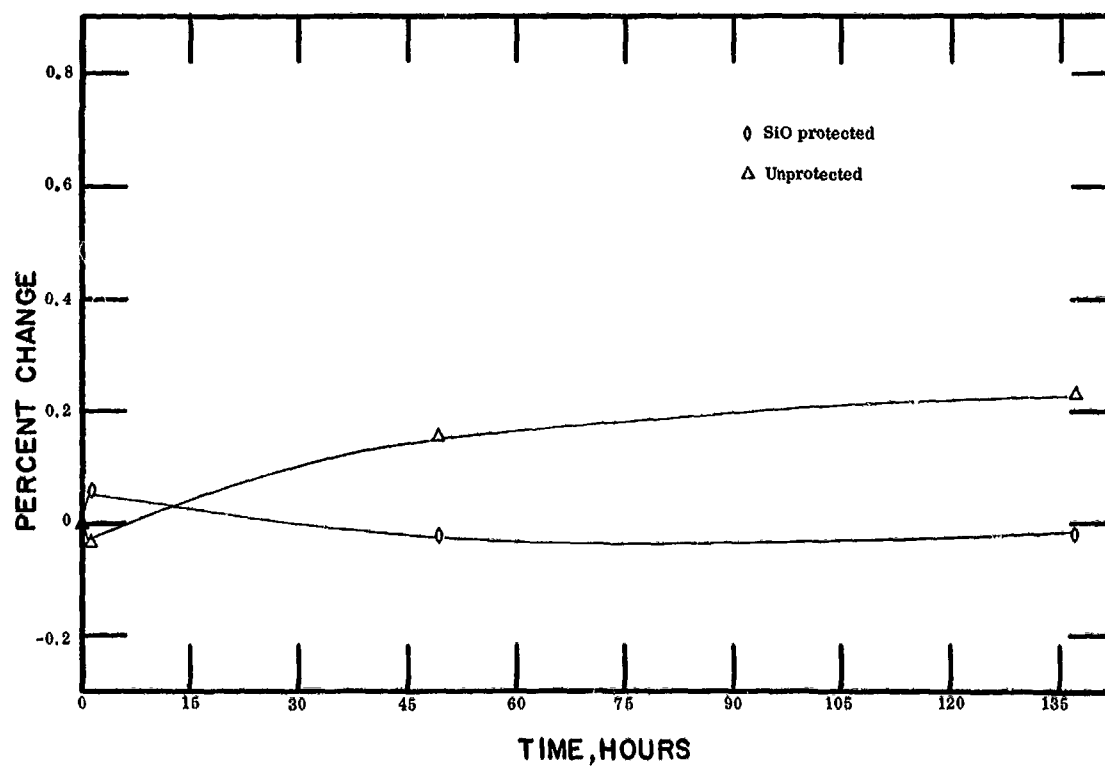


Figure 11-18—Substrate 19—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic and aged at 90°C.

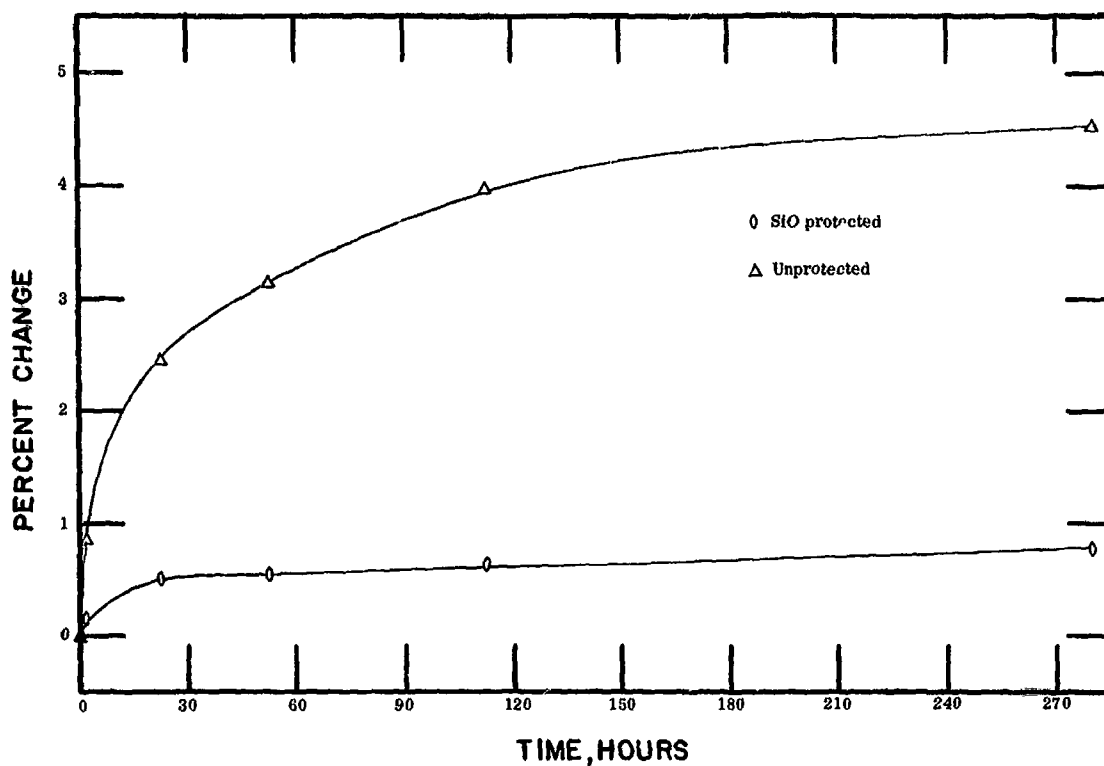


Figure 11-19—Substrate 20—Average change in resistance of 200-ohms-per-square resistors deposited on glass and aged at 125°C.

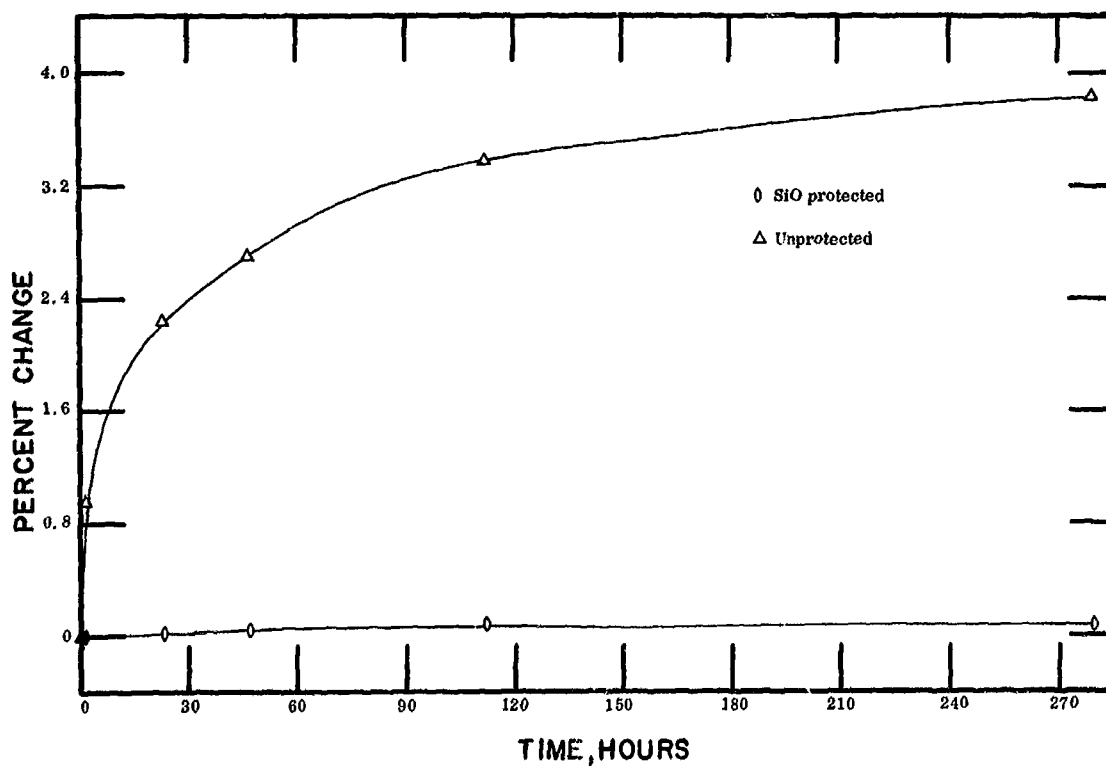


Figure 11-20—Substrate 21—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic and aged at 125°C.

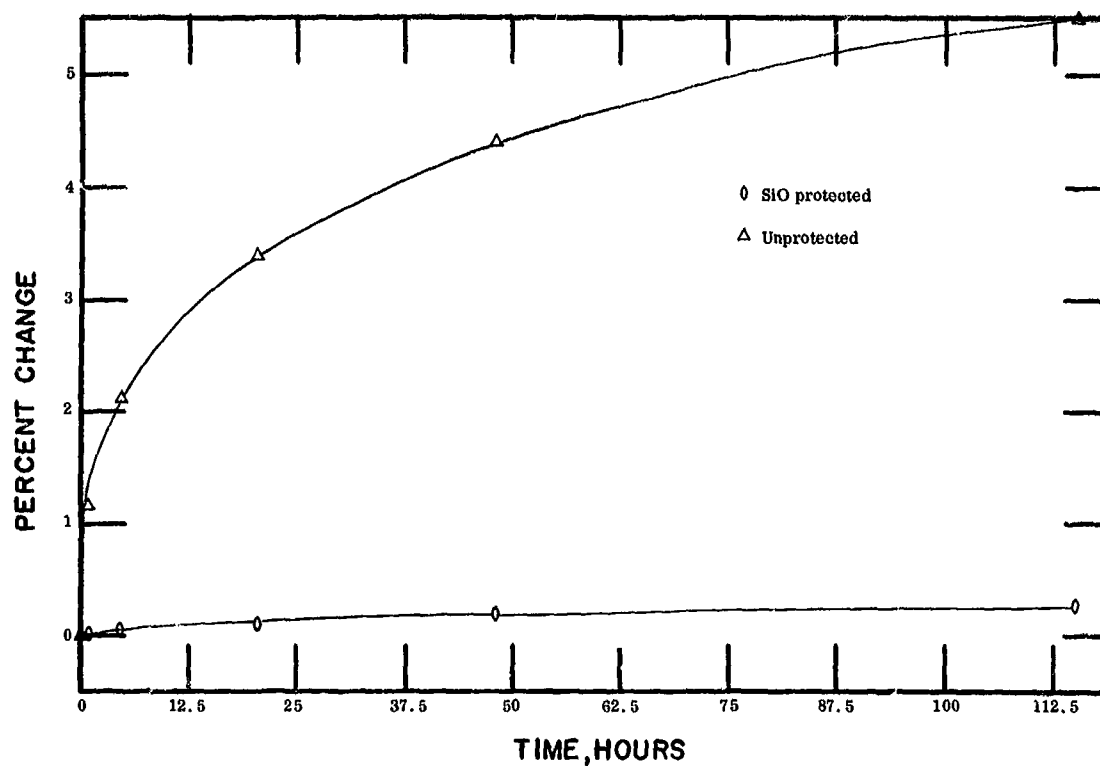


Figure 11-21—Substrate 22—Average change in resistance of 200-ohms-per-square resistors deposited on glass and aged at 152°C.

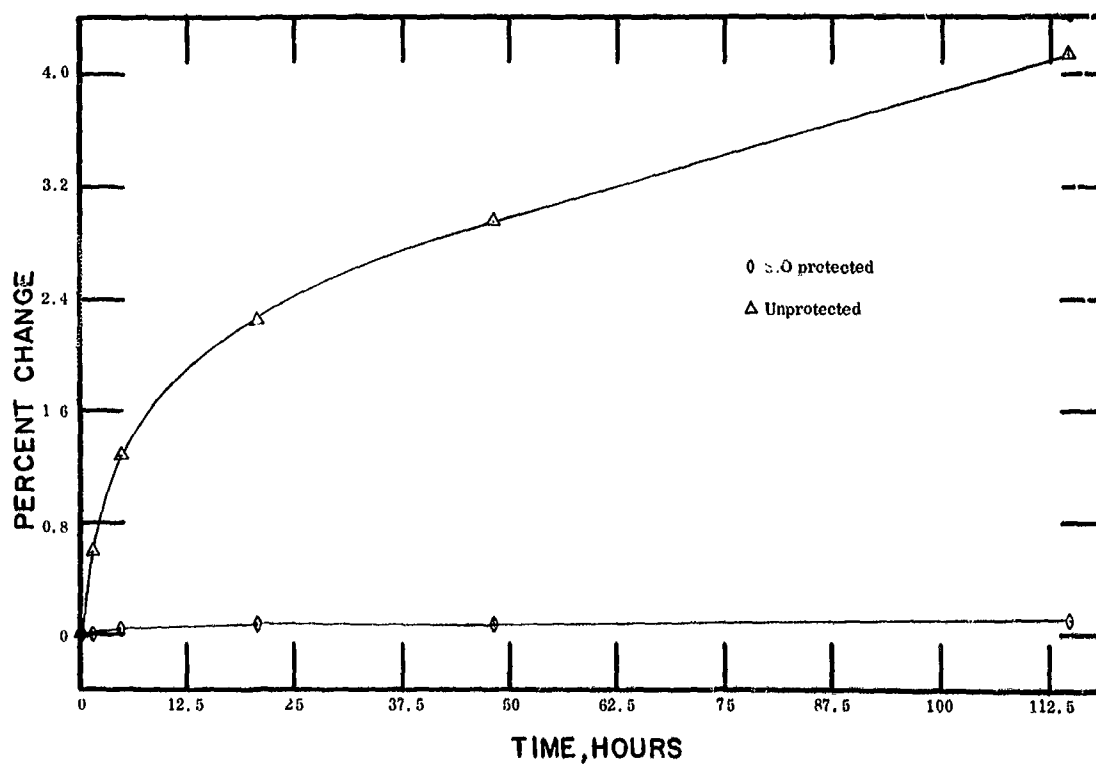


Figure 11-22—Substrate 23—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic and aged at 152°C.

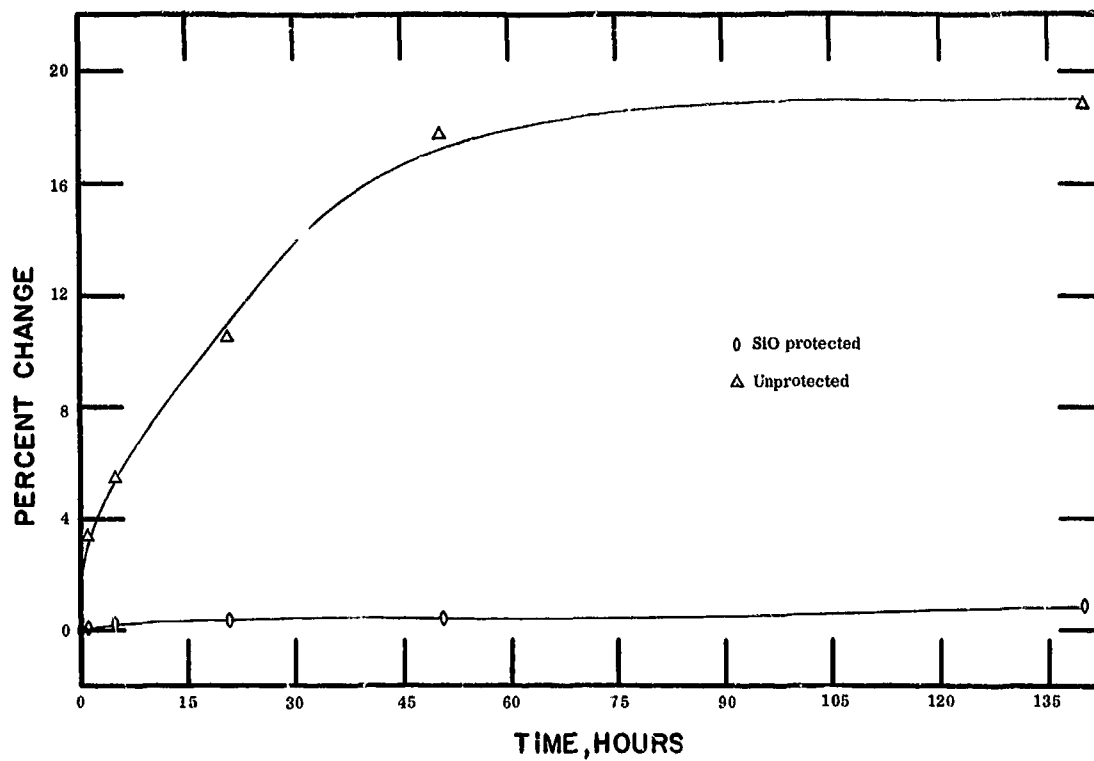


Figure 11-23—Substrate 24—Average change in resistance of 200-ohms-per-square resistors deposited on glass and aged at 198°C.

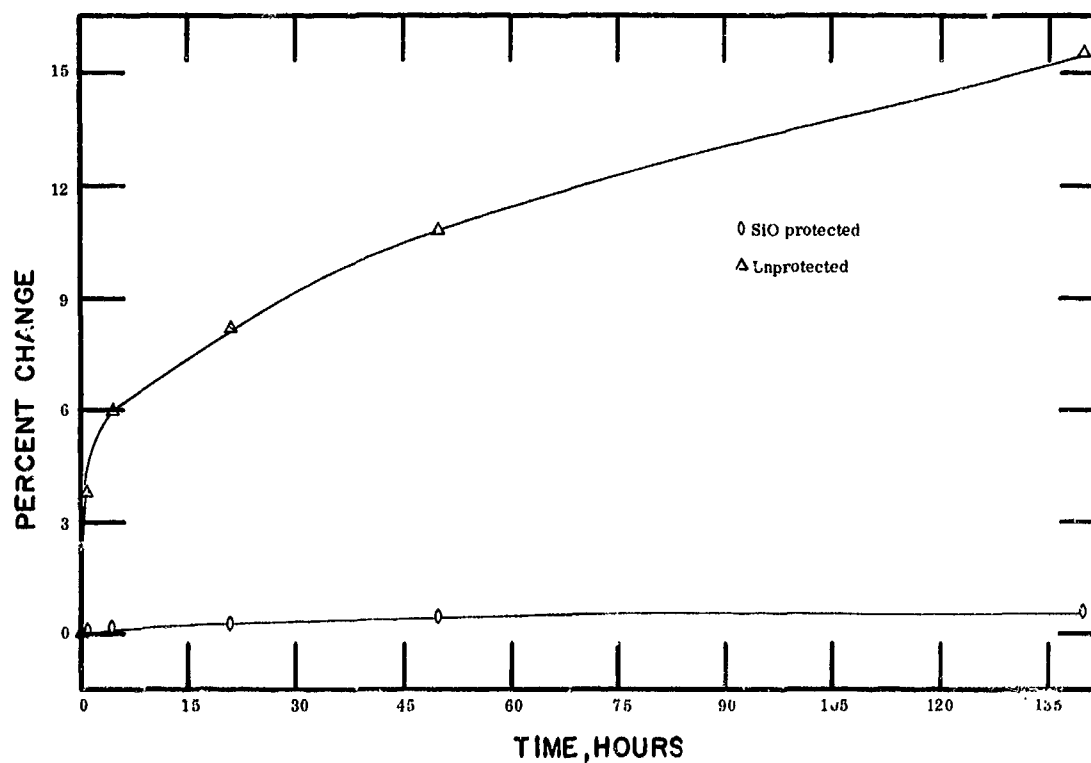


Figure 11-24—Substrate 25—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic and aged at 198°C.

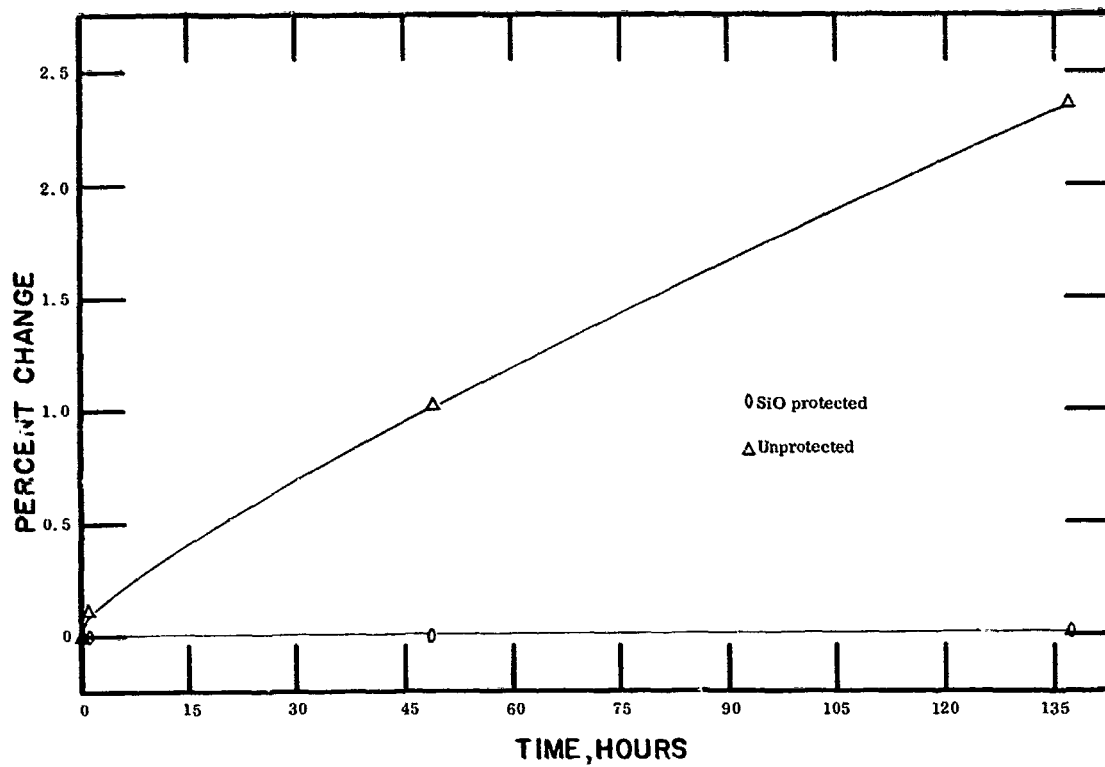


Figure 11-25—Substrate 26—Average change in resistance of 500-ohms-per-square resistors deposited on glass and aged at 50°C.

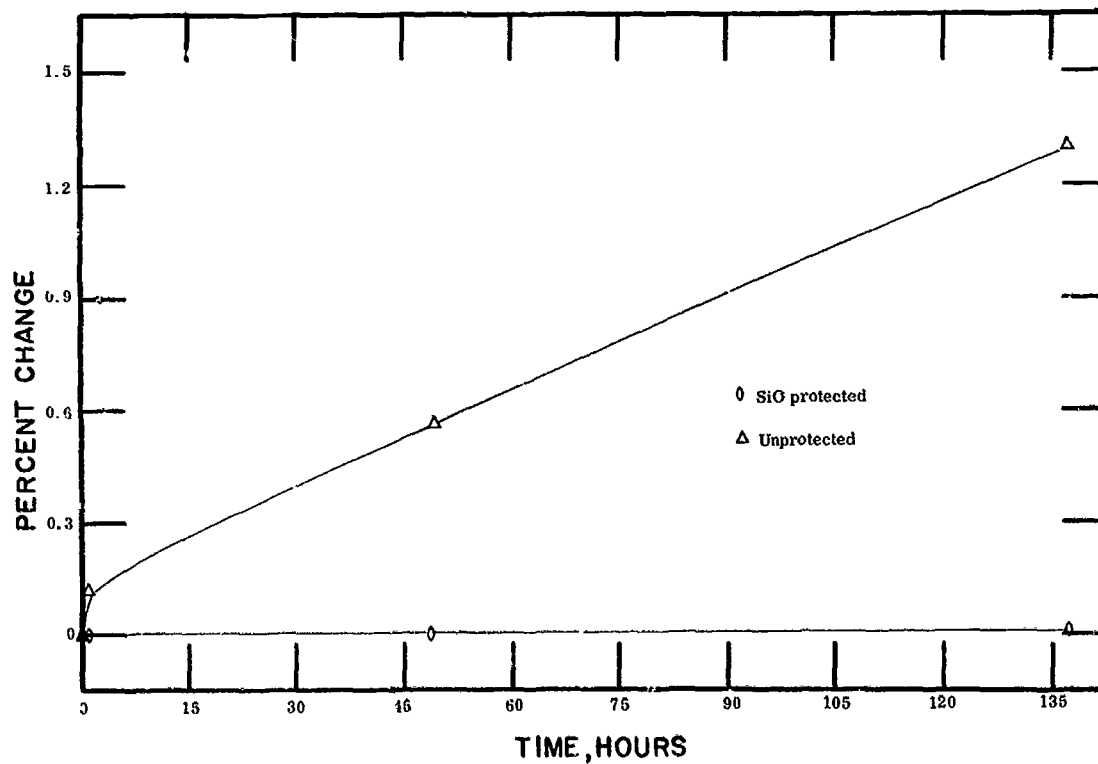


Figure 11-26—Substrate 27—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic and aged at 50°C.

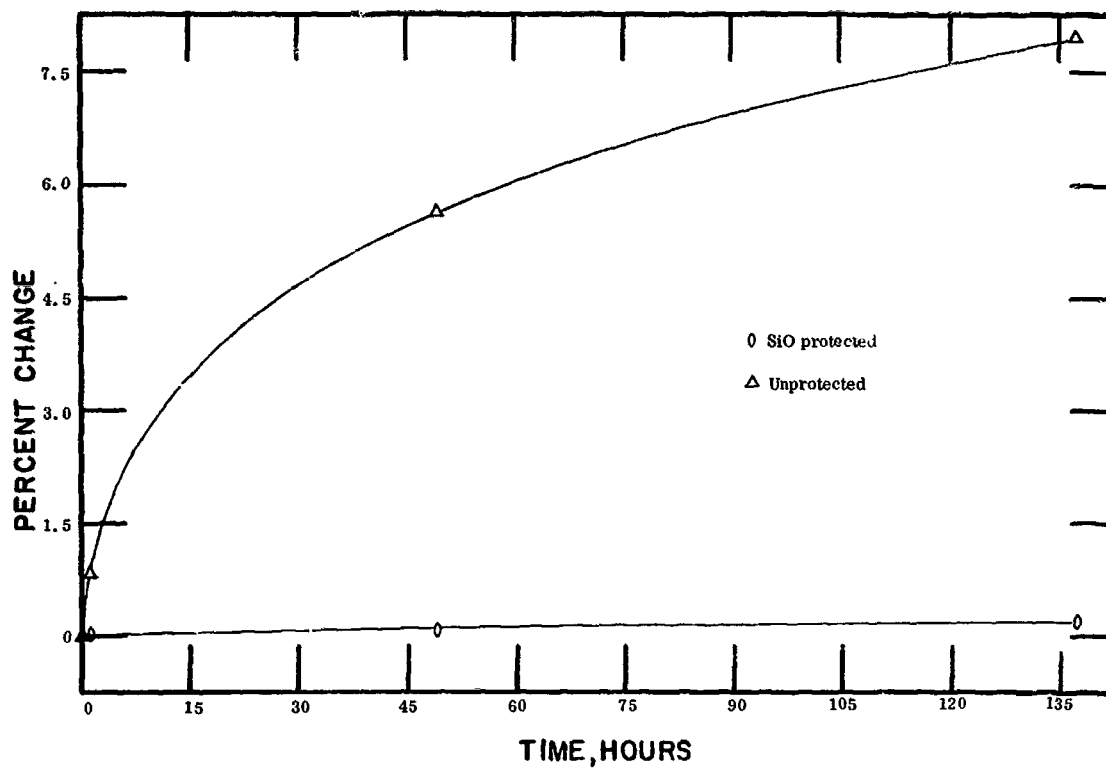


Figure 11-27—Substrate 28—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic and aged at 90°C.

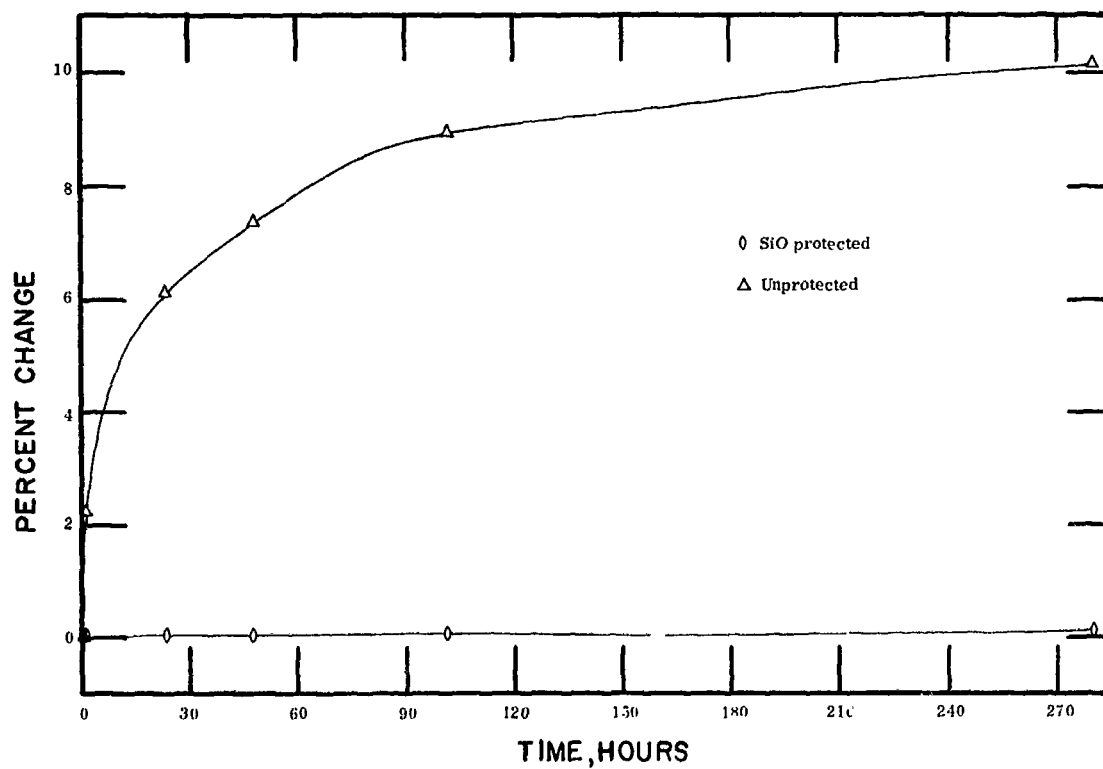


Figure 11-28—Substrate 29—Average change in resistance of 500-ohms-per-square resistors deposited on glass and aged at 125°C.

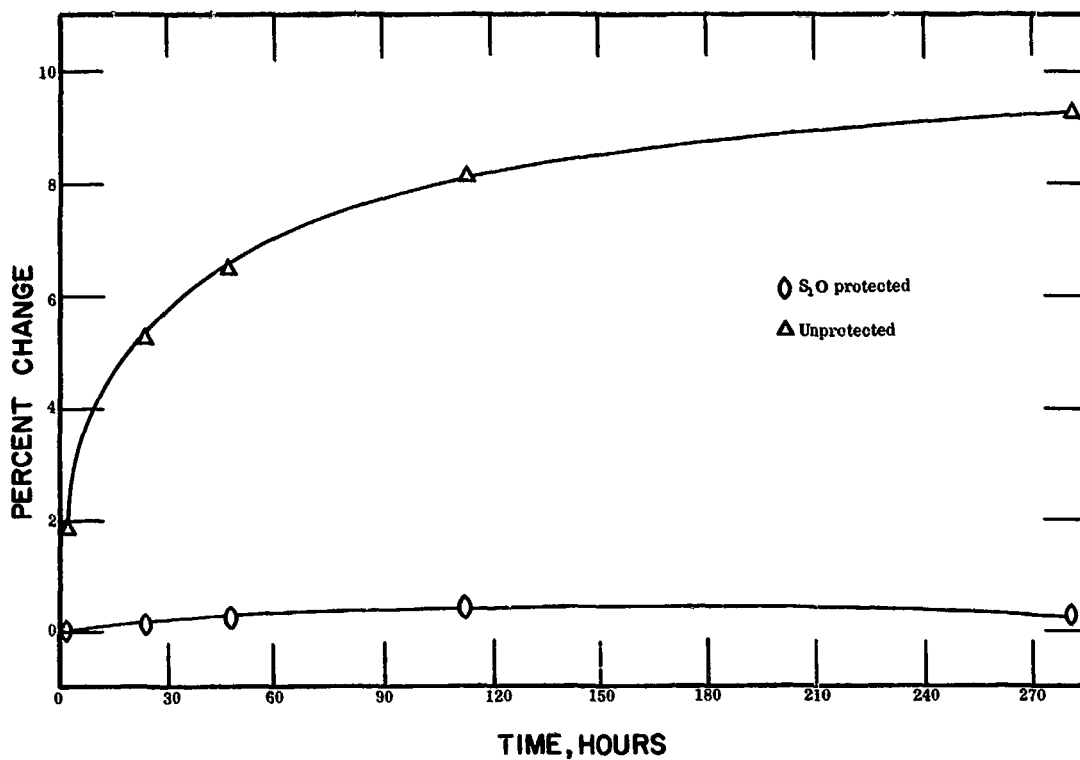


Figure 11-29—Substrate 30—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic and aged at 125°C.

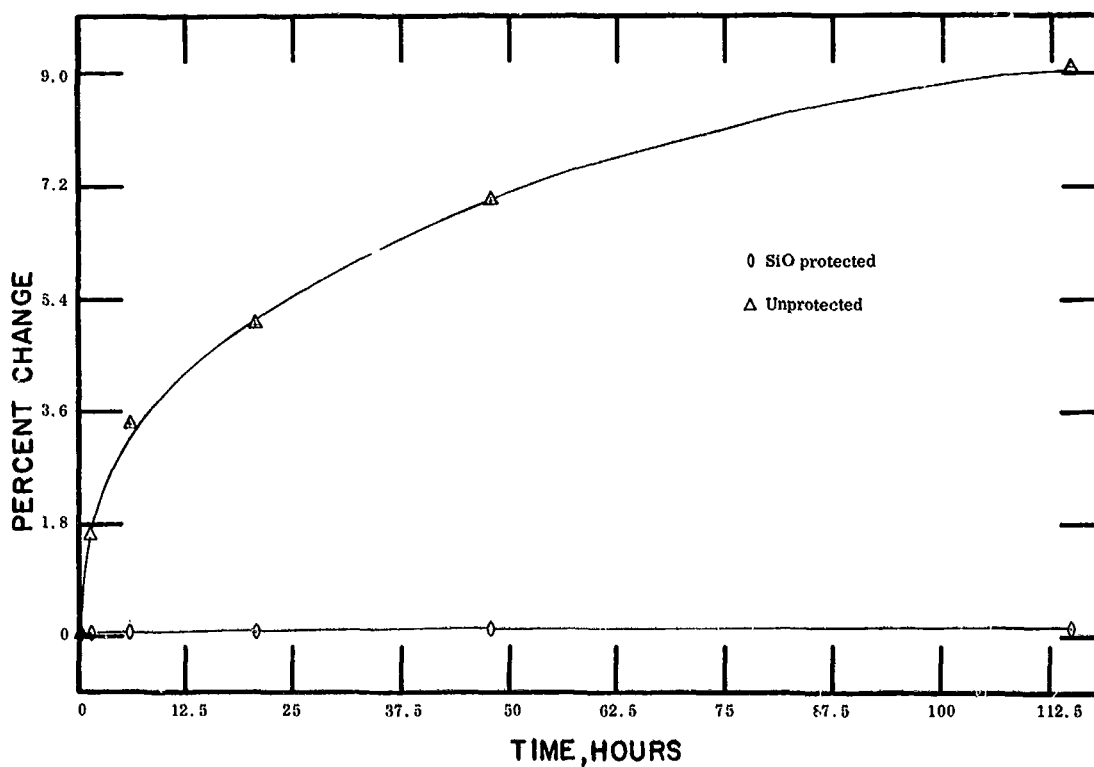


Figure 11-30—Substrate 31—Average change in resistance of 500-ohms-per-square resistors deposited on glass and aged at 152°C.



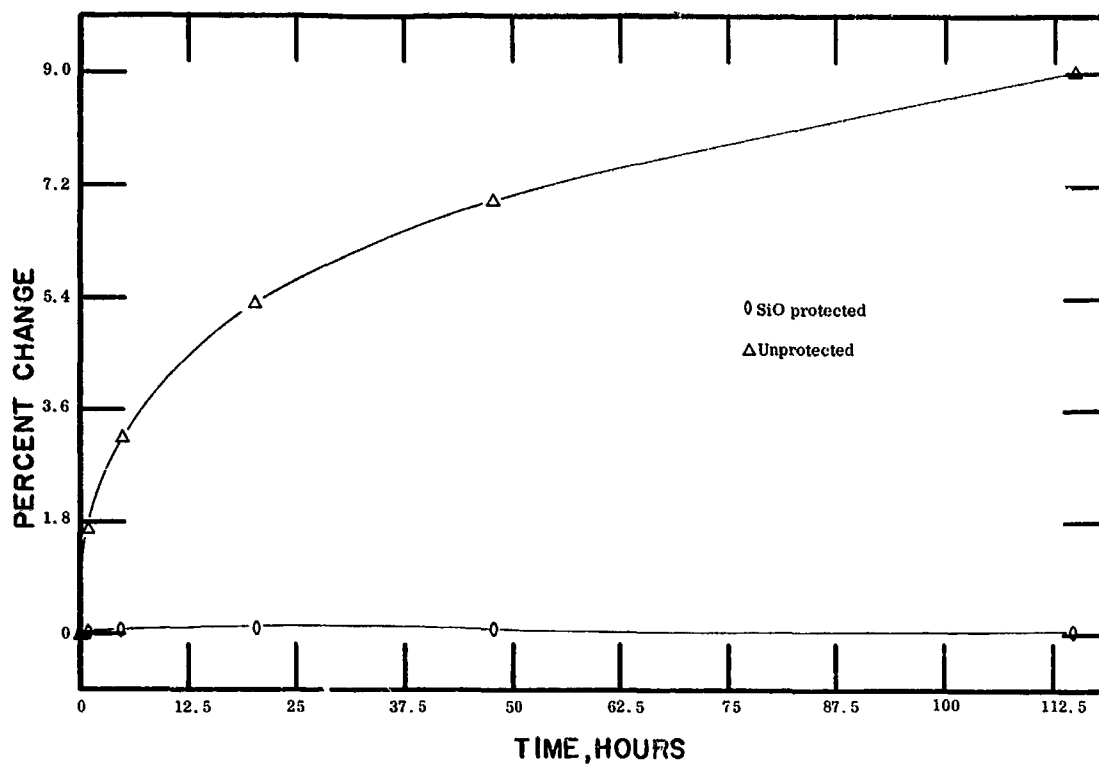


Figure 11-31—Substrate 32—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic and aged at 152°C.

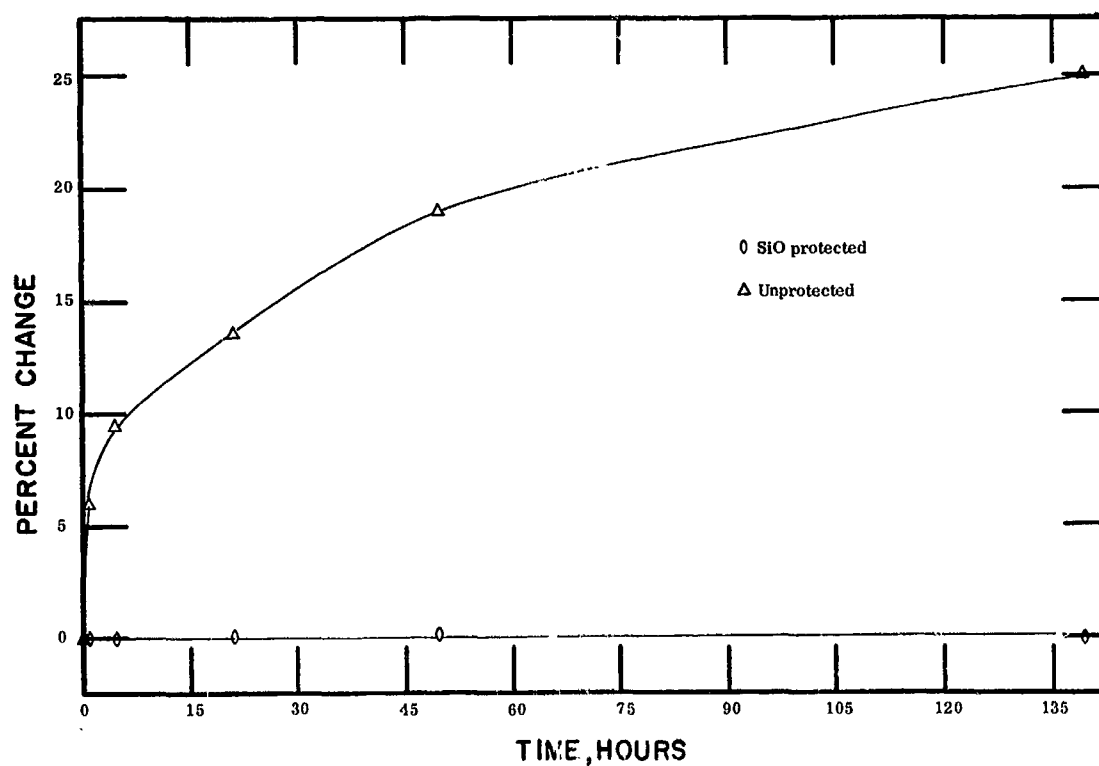


Figure 11-32—Substrate 33—Average change in resistance of 500-ohms-per-square resistors deposited on glass and aged at 198°C.

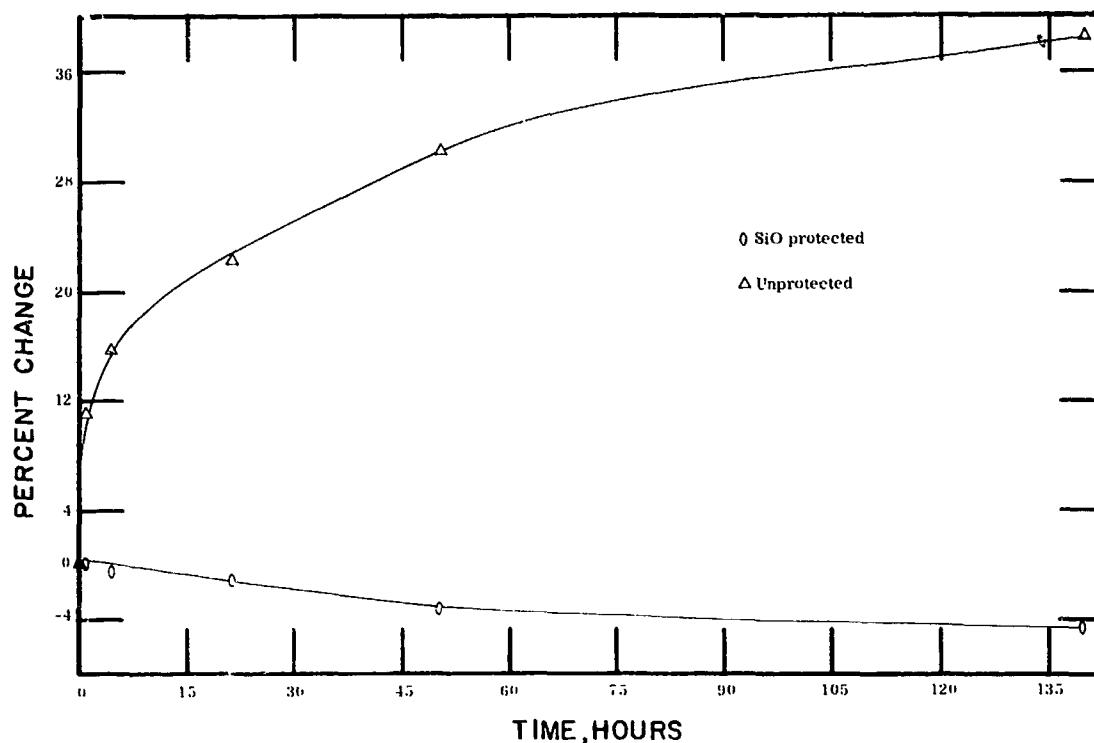


Figure 11-33—Substrate 34—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic and aged at 198°C.

3. 100-Ohms-Per-Square Films. The 100-ohms-per-square films were more stable than the thinner 200 and 500 ohms-per-square films. However, the 100-ohms-per-square film exhibited properties similar to bulk metal; that is, elevated temperature caused these films to anneal and hence decrease in resistance in some cases. The silicon-monoxide-protected, 100-ohms-per-square films are more evidence of this effect because a significant permanent change was not superimposed with the annealing factor.
4. 200-and 500-Ohms-Per-Square Films. The 200-and 500-ohms-per-square resistors behaved characteristically as would be expected of thin films. These 200- and 500-ohms-per-square films did not anneal or tend to crystallize noticeably as did the 100-ohms-per-square film. A comparison of the 100-, 200-, and 500-ohms-per-square film resistors at 150° C, both protected and unprotected, is illustrated in Figure 11-34.

#### IV. TEMPERATURE COEFFICIENT OF RESISTANCE

##### General

The temperature coefficient of resistance (TCR) was determined for nichrome resistors at film resistivities of 100, 200, and 500 ohms per square. The resistors were vacuum-deposited, as described previously, on both glazed ceramic and glass substrates.

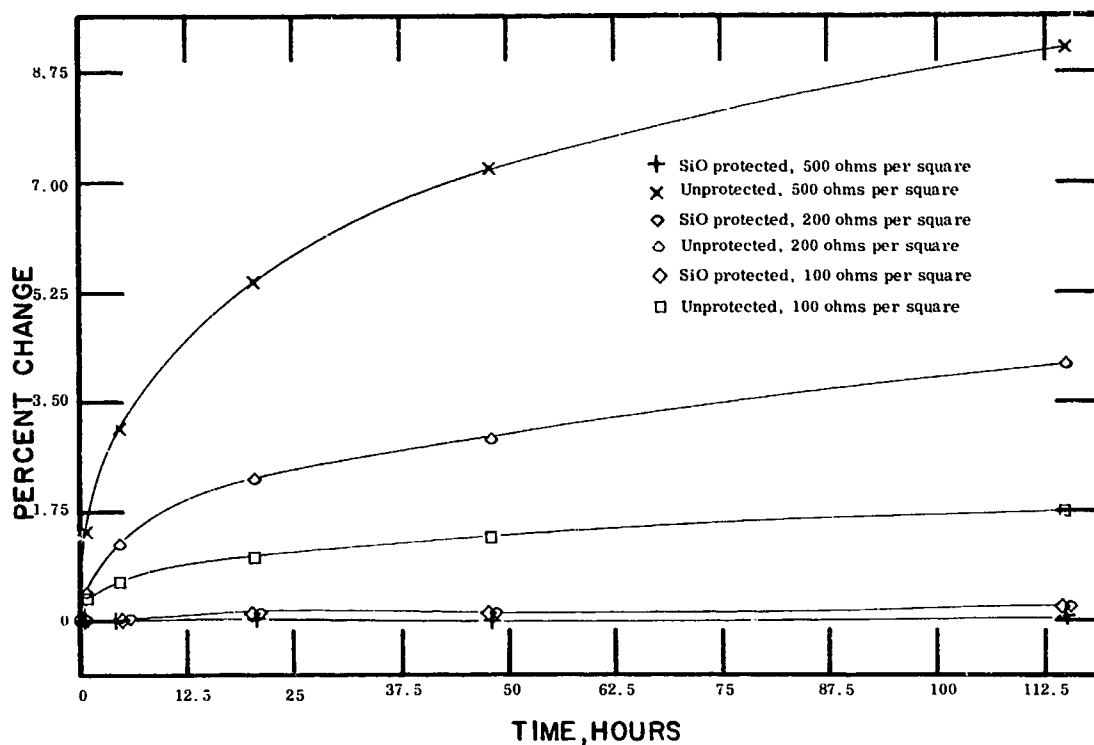


Figure 11-34—Substrates 14, 23, and 32—Average change in resistance of 100, 200, and 500-ohms-per-square resistors deposited on glazed ceramic and aged at 152°C.

### Test Procedure

The TCR was determined on both unprotected and silicon-monoxide-protected nichrome thin-film resistors. The measurements were made at several temperatures over a range of approximately -197° C (liquid nitrogen) to +150° C. At +25° C above, the unprotected resistors were heated, and resistance measurements were taken while the substrates were in a vacuum chamber at a pressure range of  $10^{-4}$  N/m<sup>2</sup>. This procedure prevented oxidation of the metal, which causes permanent changes in resistance. Silicon-monoxide-protected resistor tests were conducted in normal atmosphere.

Resistance measurements were made as a function of temperature, and the resultant data were plotted. The TCR was calculated from the R versus T curves by the standard formula

$$\text{TCR} = \frac{R_2 - R_1}{R_1(T_2 - T_1)} \times 10^6 = \text{parts per million per degree centigrade,}$$

where  $R_1$  = resistance at reference temperature in ohms,

$R_2$  = resistance at test temperature in ohms,

$T_1$  = reference temperature in °C, and

$T_2$  = test temperature in °C.

## Electrical Measurements

Resistance measurements were taken with a precision impedance bridge. Bridge accuracy is 0.05 percent with a precision of 0.01 percent. A type J thermocouple was placed in surface contact with the substrates for temperature measurements. The holding fixture described previously was used to retain the substrate during electrical measurement of each resistor. In the vacuum experiments, wire leads were soldered to individual resistor termination pads. A standard vacuum seal feed-through was used for the leads from the system.

## Low-Temperature Measurements

Low-temperature measurements were made with a type J thermocouple and a millivolt potentiometer using liquid nitrogen as the coolant. The thermocouple reference junction was measured with a thermometer. The substrate and holding fixture (Figure 11-2) were placed on a platform above the liquid level inside a Dewar flask containing liquid nitrogen. The liquid nitrogen level was adjusted to provide the desired temperature. The resistors were measured when the substrate temperature became constant. The  $-197^{\circ}\text{C}$  tests were made with the entire holding fixture and substrate immersed in the liquid nitrogen.

## Test Results

The percent change versus temperature data were plotted for each substrate and are shown in Figures 11-35 through 11-46. The complete TCR data are compiled in Table 11-8. The curves shown in the figures represent an average of the individual resistor values on a single substrate. The TCR values given in Table 11-8 were calculated from the plotted curves in the temperature range of  $-55^{\circ}$  to  $+125^{\circ}\text{C}$ . This temperature range represents the operating range normally specified for electronic circuits.

The 100- and 200-ohms-per-square film resistors had negative TCR values of 37 or less. One exception was found in the silicon monoxide protected films on glazed ceramic substrate number 39. The resistor deposited on this particular substrate gave positive TCR data which were inconsistent with the other resistor films tested. In addition to the positive TCR values shown in Figure 11-39, the aging characteristics at  $+125^{\circ}\text{C}$  shown in Figure 11-11 did not follow the pattern exhibited by the other nichrome films. Therefore, continual thermal anneal of the 100-ohms-per-square film affected the properties of this film in contrast to the thinner 200- to 500-ohms-per-square films. However, the usefulness of the thicker film (100 ohms per square) for electrical passive devices would not be hampered.

Generally, TCR data (Reference 2) have been reported for nichrome in both positive and negative values. It has been postulated that the thickness of the film and the solidarity of the aggregate growth determine the direction in which the resistance changes with change in temperature

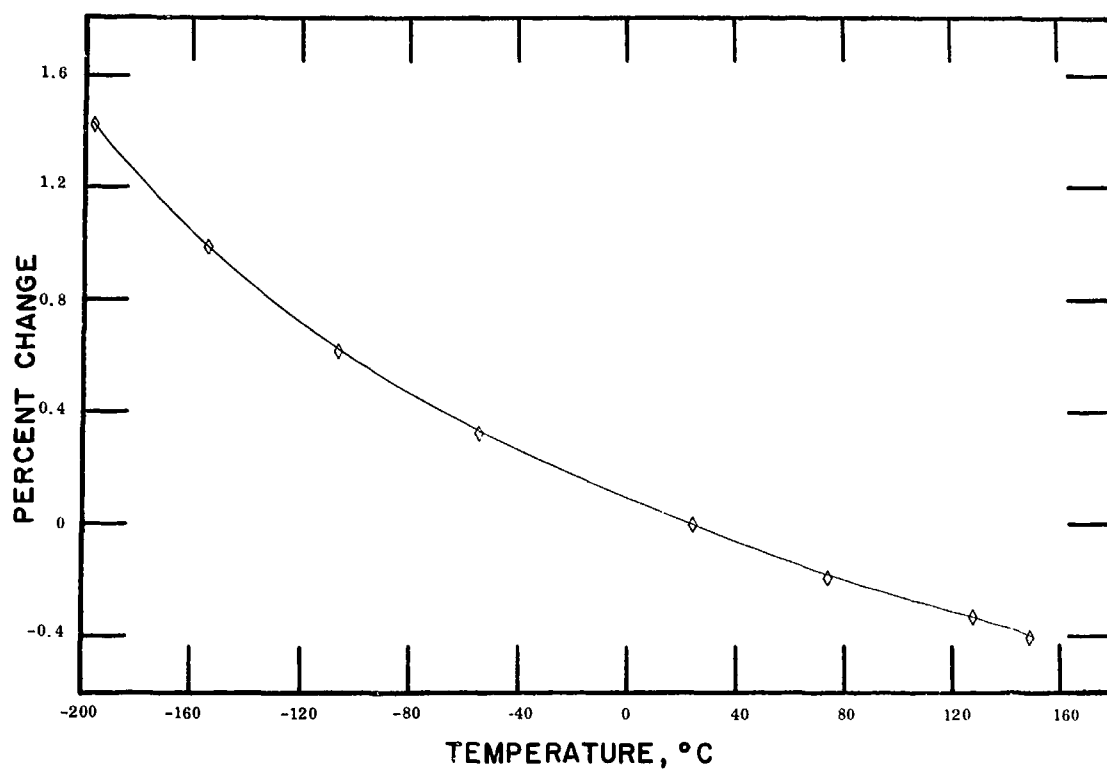


Figure 11-35—Substrate 35—Average change in resistance of 200-ohms-per-square resistors deposited on glass.

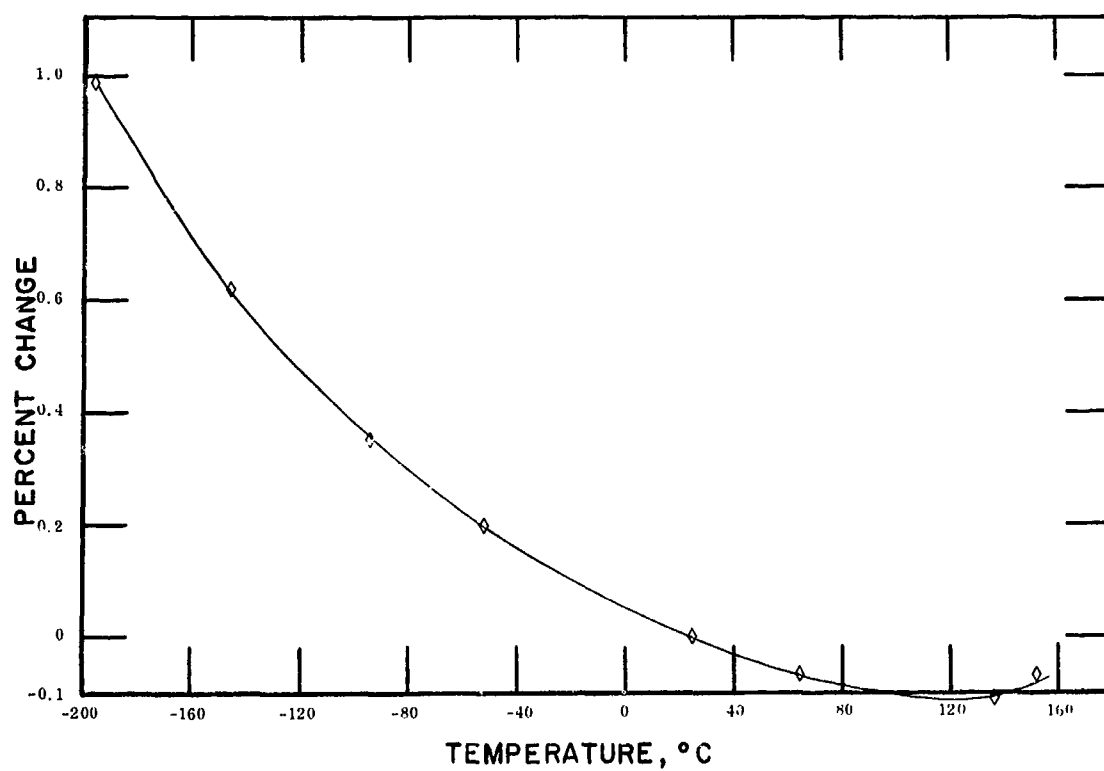


Figure 11-36—Substrate 36—Average change in resistance of 200-ohms-per-square resistors deposited on glass.

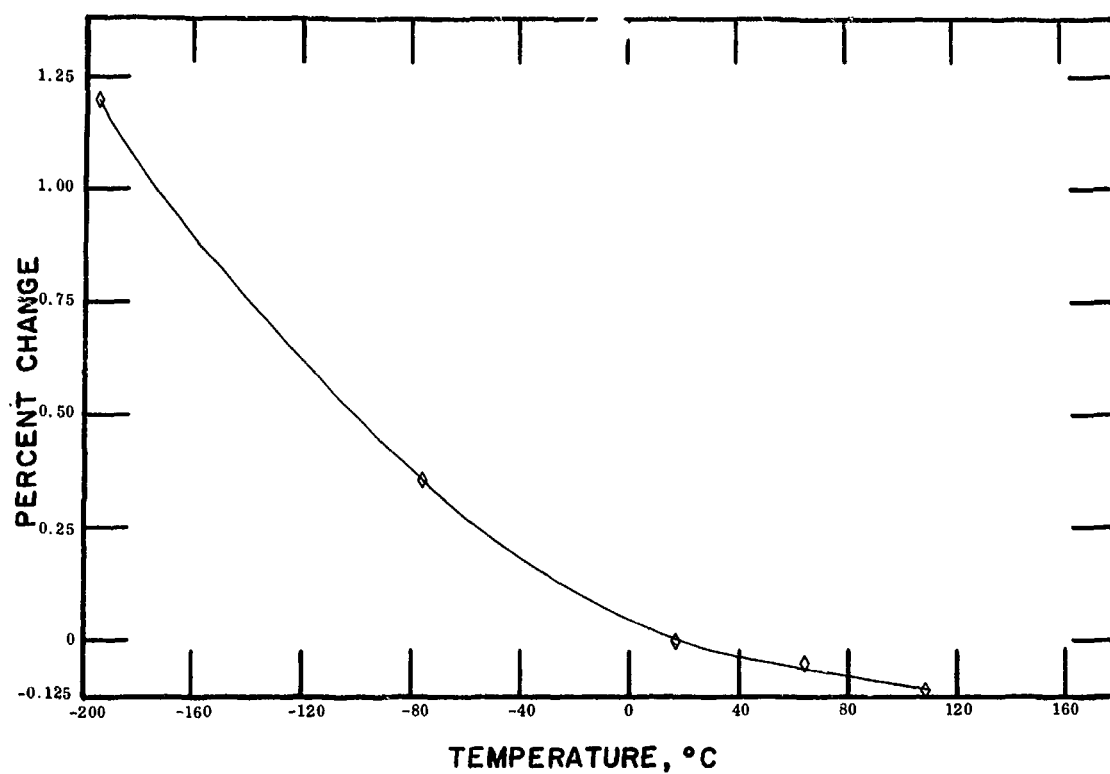


Figure 11-37—Substrate 37—Average change in resistance of 200-ohms-per-square resistors deposited on glass.

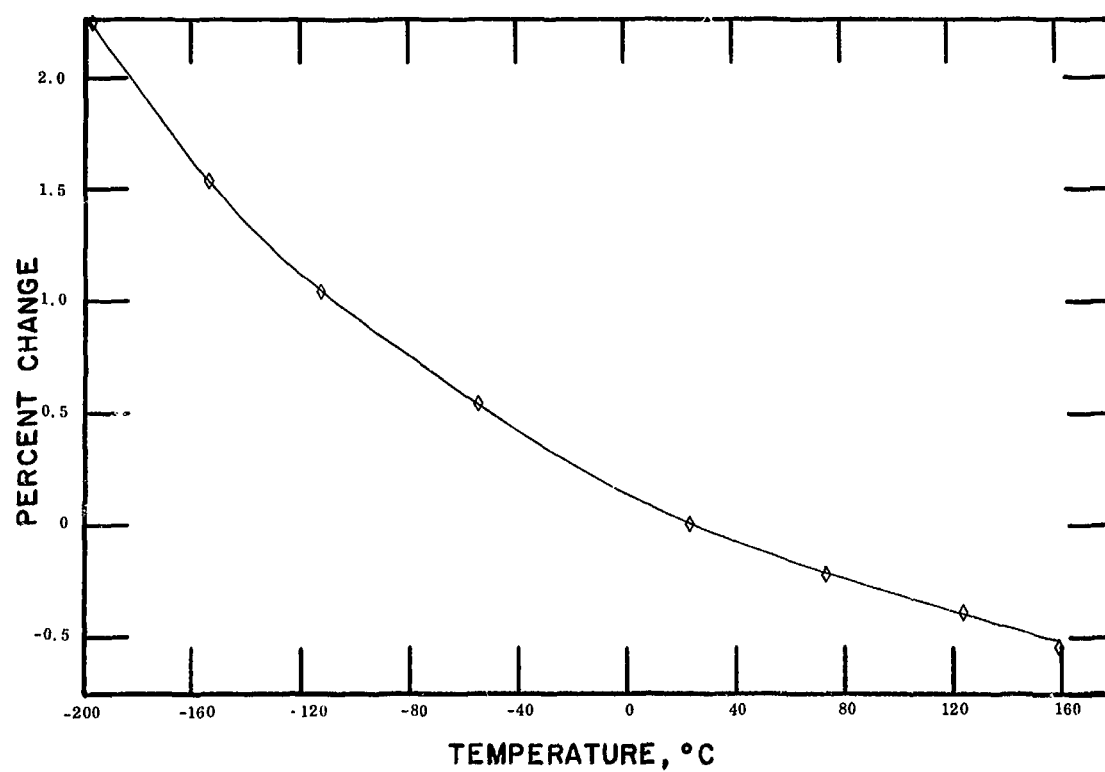


Figure 11-38—Substrate 38—Average change in resistance of 500-ohms-per-square resistors deposited on glass.

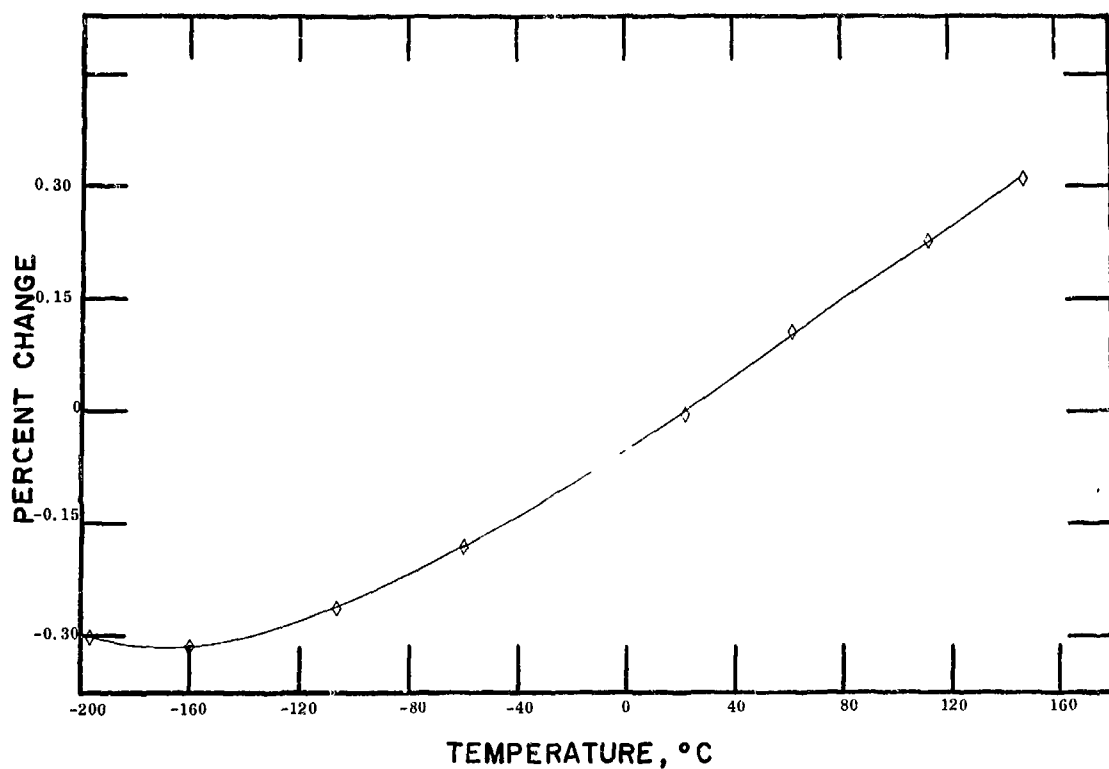


Figure 11-39—Substrate 39—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic.

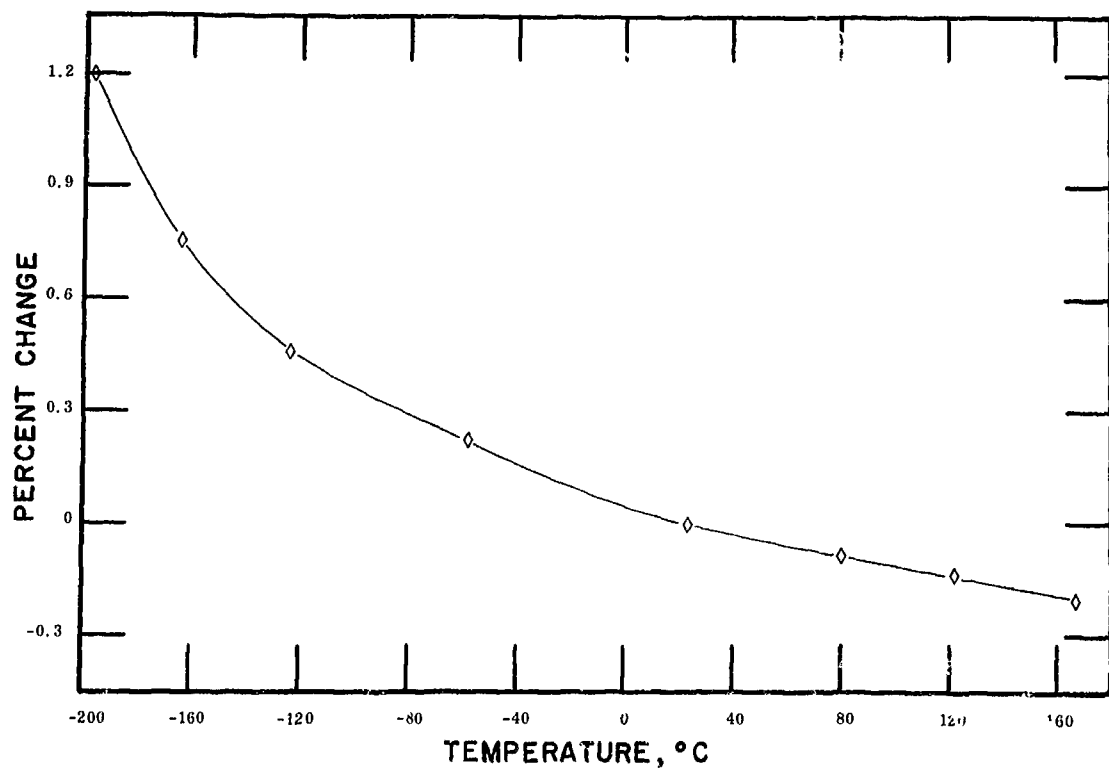


Figure 11-40—Substrate 40—Average change in resistance of 100-ohms-per-square resistors deposited on glazed ceramic.

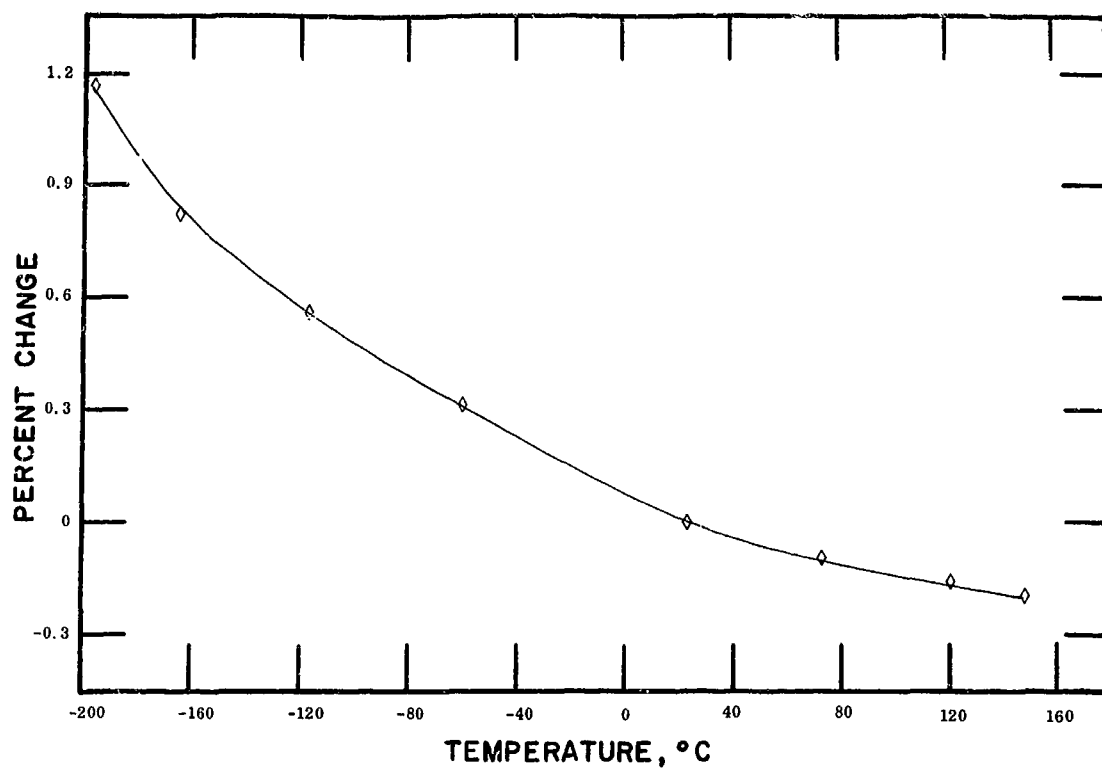


Figure 11-41—Substrate 41—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic.

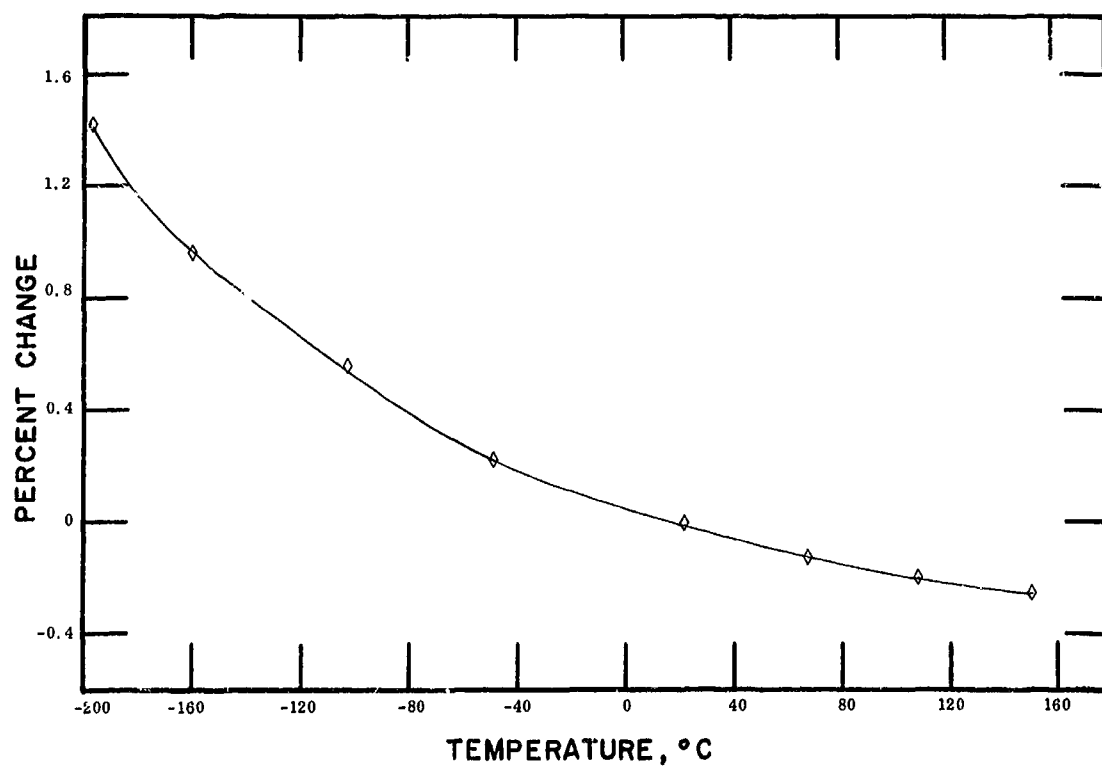


Figure 11-42—Substrate 42—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic.



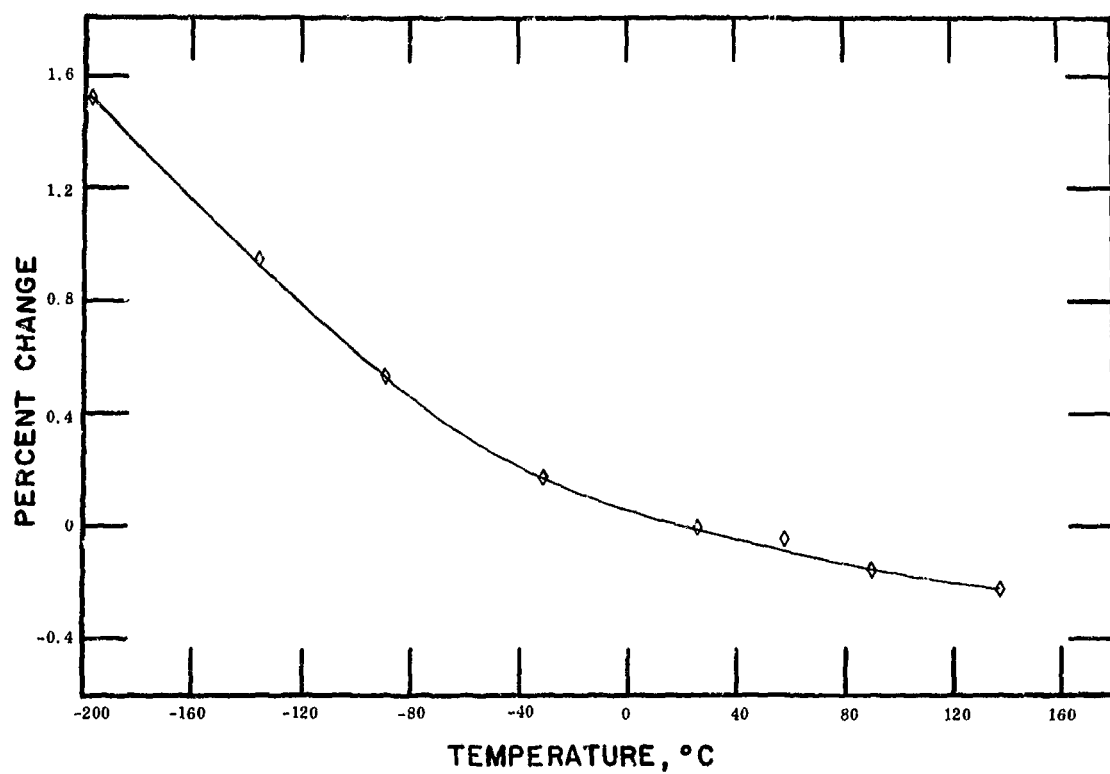


Figure 11-43—Substrate 43—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic.

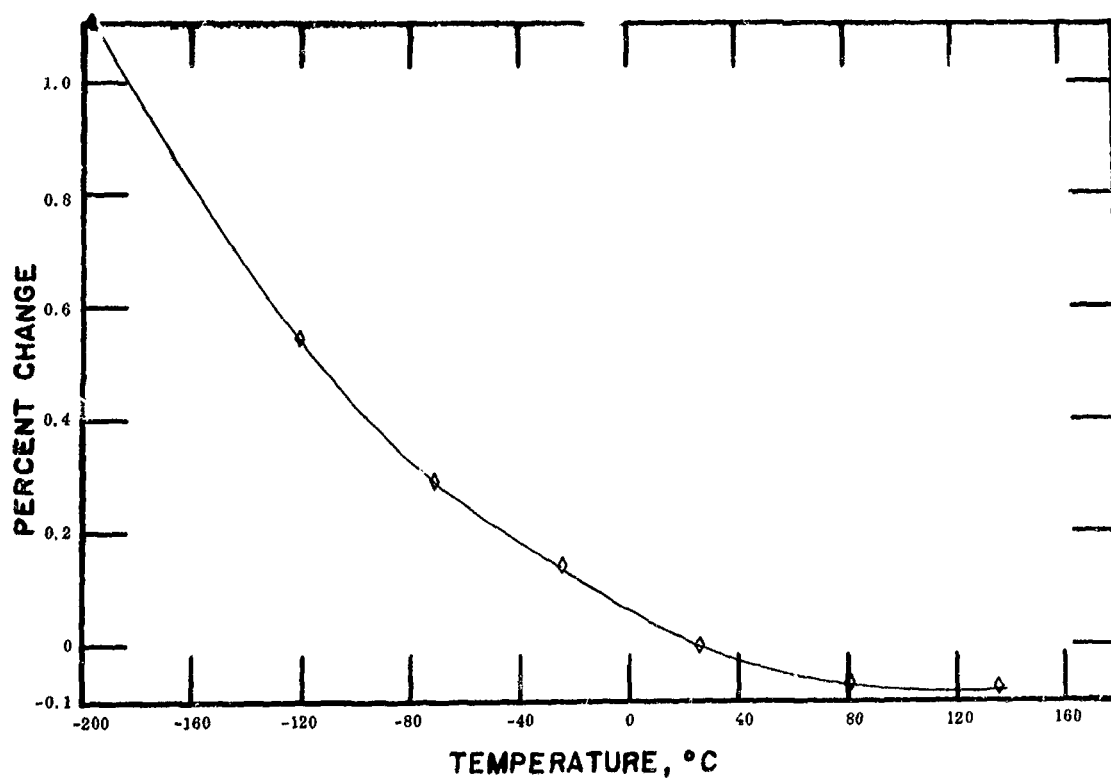


Figure 11-44—Substrate 44—Average change in resistance of 200-ohms-per-square resistors deposited on glazed ceramic.

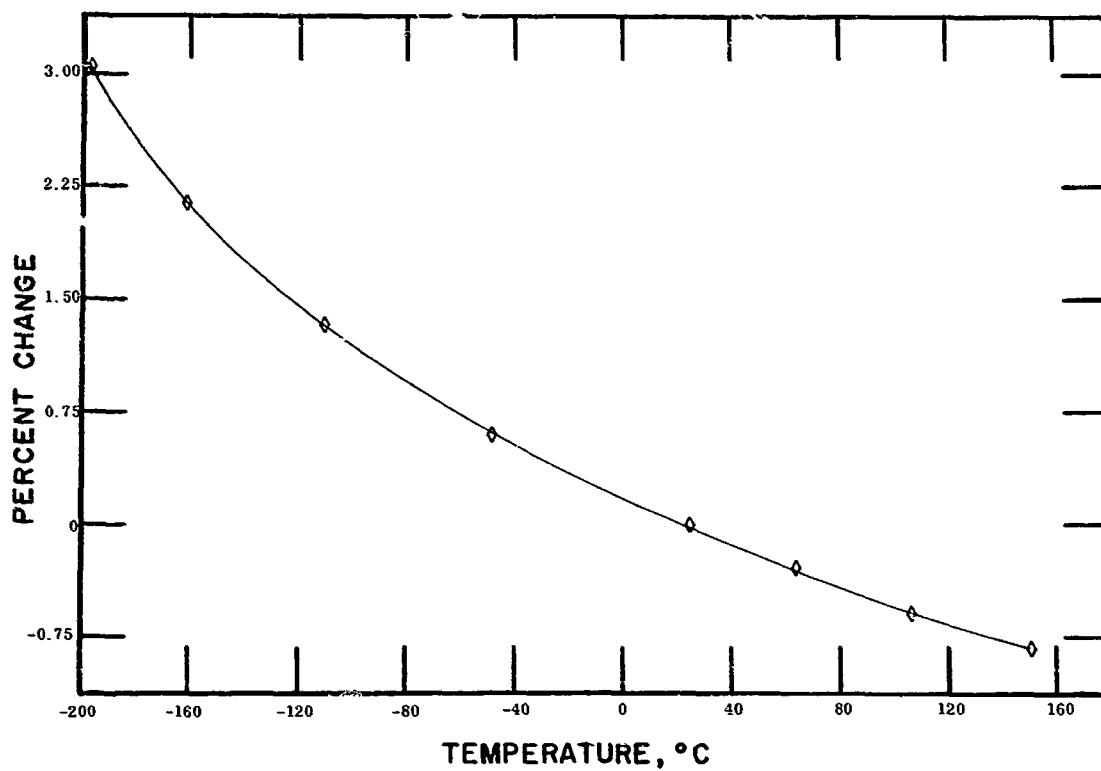


Figure 11-45—Substrate 45—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic.

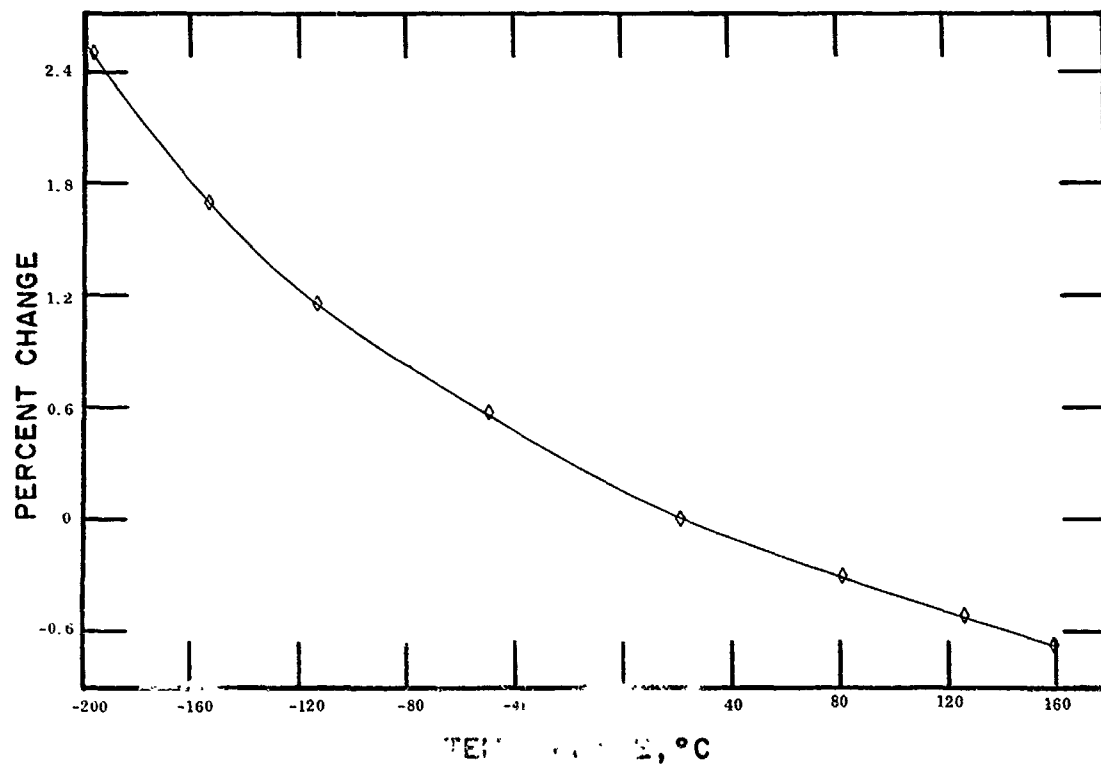


Figure 11-46—Substrate 46—Average change in resistance of 500-ohms-per-square resistors deposited on glazed ceramic.

Table 11-8

**Temperature Coefficient of Resistance of Nichrome Resistors on  
Glass and Glazed Ceramic Substrates**

Parameter	Glass				Ceramic							
Film resistivity, ohms/sq	200	200	200	500	100	100	200	200	200	200	500	500
Protective coat	SiO	none	none	SiO	SiO	SiO	SiO	SiO	none	none	SiO	SiO
Number resistors tested	7	5	5	7	7	3	7	7	5	5	6	7
Test range, °C	-197 to +149	-197 to +152	-197 to +113	-197 to +159	-197 to +147	-197 to +167	-197 to +150	-197 to +149	-197 to +137	-197 to +135	-197 to +159	-197 to +150
Resistance change:												
Total, percent	1.83	1.00	1.31	2.80	0.6	2.2	1.67	1.37	1.64	1.20	3.15	3.84
-55 to +125°C, percent	0.67	0.31	0.34	0.90	0.39	0.33	0.48	0.51	0.51	0.29	1.08	1.42
Average TCR, PPM/°C												
-55 to +125°C	-37	-18	-20	-51	+22	-19	-24	-25	-29	-17	-62	-73
-55 to +25°C	-43	-24	-31	-70	+19	-27	-32	-41	-43	-25	-80	-87
+25 to +125°C	-33	-8	-12	-37	+25	-13	-19	-16	-19	-5	-48	-64
Reference number:												
Substrate	35	36	37	38	39	40	41	42	43	44	45	46
Figure	35	36	37	38	39	40	41	42	43	44	45	46
Page	57	58	59	60	61	62	63	64	65	66	67	68

(Reference 3). Ultrathin films, where small islands formed around nuclei growth patterns, exhibit high resistivity and negative TCR. Thin films, in contrast to ultrathin films, show positive TCR characteristics. The resistivity values have not been clearly defined as to thin and ultrathin films. The data derived from the resistor experiments described in this report would tend to classify the films in the ultrathin category. Additional studies are currently being made to determine the exact mechanism causing these thin-film resistors generally to have negative TCR values.

## V. CONCLUSION

### Advantages of Nichrome

The nickel-chromium thin-film resistors tested in the laboratory showed properties consistent with published reports using similar material and procedures. Most known metals, both pure and alloy, have been investigated as possible resistor material for microelectronic passive elements. The major drawback of nichrome alloy in thin-film form is the limited ohms-per-square range from 50 to 500. Materials such as chromium, nickel, tantalum, chromsilicon, titanium, rhenium, and

others have been deposited successfully in planar array but have shortcomings more undesirable than nichrome. Most metals and alloys cannot be evaporated from a simple resistance-heated filament and therefore require DC sputtering, electron bombardment, flash evaporation, or chemical vapor deposition. Stability in most cases is improved but results in much higher TCR values.

### Significant Conclusions From Nichrome Data

The nichrome data presented in the figures and tables show several significant conclusions:

1. Film Protection. Films must be protected with a passive layer, such as vapor-deposited silicon monoxide, to prevent atmospheric oxidation that results in permanent resistance change.
2. 500-Ohms-Per-Square Films. Nichrome films are usable to 500 ohms per square when passivated (Figures 11-25 through 11-32).
3. Thermal Anneal. Film thicknesses of 100 ohms per square are thermally stable, but they anneal and change properties when heated. The 200- to 500-ohms-per-square films appear not to change because of further thermal anneal. All the films produced for these tests were annealed initially at 225° C in a vacuum.
4. TCR Variance. The average temperature coefficient of resistance varied from +22 to approximately -87 ppm/° C. One substrate yielded resistors with a TCR averaging +22 ppm/° C (Figure 11-39). This inconsistency was probably caused by the thickness of the 100-ohms-per-square film, which continued to anneal during aging tests.
5. Substrate for Thin-Film Components. Glass or glazed ceramic makes a suitable base for thin-film components. No significant difference was found in resistor properties deposited on either type of substrate.

### Practical Aspects

In performing tests as discussed in this report, foremost consideration is given to the practical aspects of producing electrical circuits in the form of microelectronics. The laboratory has been successful in producing numerous working circuits using nichrome metal. The method used (Reference 4) for optimum efficiency requires that all the thin-film passive elements and interconnection network be deposited on a substrate in a single vacuum cycle. Although other material will work as thin-film resistors, nichrome is the most convenient and reliable to use in a simple resistance-heating source.

The nichrome resistors produced on hybrid microelectronic circuits in this laboratory have been deposited through precision metal masks with a routine tolerance of  $\pm 5$  percent. Circuits

containing resistors with  $\pm 3$  percent or better tolerances are possible by selection. Matching between resistors on a single substrate is normally  $\pm 3$  percent or better. Yield of usable circuits with thin-film nichrome resistors on a production basis is greater than 75 percent. Statistical data for microcircuit production are being prepared in a separate report.

#### REFERENCES

1. Holland, Thin-Film Microelectronics, Chapman and Hall, October 1965.
2. I. A. Lesk, Thin-Films in Integrated Circuits, Motorola Instruction Course.
3. E. R. Dean, Aging Mechanisms in Thin-Film Resistors, Transactions of the Metallurgical Society of AIME, Volume 236, 1966.
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## 12. MICROCIRCUIT MASKING TECHNIQUES

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This paper discusses microcircuit masking, from the artwork preparation stage to the final circuit pattern. Emphasis is given to the importance of edge resolution and the physical limitations inherent in the various masking techniques. Fabrication methods of each type are discussed, and detailed process data is included in the appendix for some of the types. Special masking techniques such as those used in thin-film transistor fabrication are also included.

### INTRODUCTION

Microcircuit masks are generally associated with vacuum-deposited thin-films and are assumed to be a thin foil having apertures corresponding to some desired circuit pattern. To a great extent, this assumption is true, but it is not complete since it describes only one type of mask. Microcircuit masking techniques are many and varied, but they are all based on a photographic and etching process known as photoengraving.<sup>1</sup>

In photoengraving, a photographic image and a light-sensitive, etch resistant medium known as photoresist is used to produce a circuit pattern on some desired material. This pattern is transferred permanently onto the material with an etchant. In some cases the etched material may become an integral part of a circuit itself, but more commonly it becomes a mask for additional processing operations.

This paper will describe the types of masks used in microcircuitry, the methods used to fabricate them, and their advantages and disadvantages. Particular attention is given to the importance of edge resolution since it is the factor which governs tolerance as circuit geometries become smaller. Processing details for some of the masking techniques are given in the appendix.

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<sup>1</sup>This technology is often referred to as "photolithography" however, since etching is involved rather than lithography, "photoengraving" or more generally, "photomasking" is preferred.

## THE PHOTOGRAPHIC IMAGE

The photographic image used in photoengraving is itself a mask, a photomask, and it must be perfect in every detail since any defects in it will be transferred to all subsequent processing steps. The photomask should be dimensionally stable, capable of high resolution, and possess a high contrast ratio. All of these requirements are satisfied by high-resolution glass photographic plates.<sup>2</sup> The plates are preferred not only for their resolution capabilities, which are considerable, but for their flatness and ease of mounting. The theoretical resolution obtainable from the emulsions on these plates is 2000 lines-per-millimeter, and this far exceeds that obtainable from any available lens system (see Reference 1).

## THE ART WORK MASTER

The quality of the photographic image can be no better than the artwork and camera which produced it. Since the artwork is many times larger than the photographic image, errors in it are reduced in proportion to the amount of reduction. The artwork masters are most often prepared on a precision x-y coordinatograph<sup>3</sup> using "cut 'n' strip"<sup>4</sup> laminated drafting films. When the opaque upper layer is cut and peeled away from the supporting transparent mylar base, the film is capable of contrast ratios of 1000:1 with rear illumination. The best ratio obtainable with front illuminated ink drawings is 50:1 (see Reference 2). The most important feature of the laminated drafting films is that a clean edge is obtained when the films are cut; this minimizes light scattering and produces an improved image edge on the photographic plate.

## THE MICROCIRCUIT CAMERA

The camera system used in microcircuit mask making can be very simple if fixed reductions are used with fixed artwork sizes (see Reference 1). This will save time in both the photographic and artwork preparation stages, although it will limit the flexibility of the installation. The lens is the most important part of the camera system, and special microcircuit reduction types are available.<sup>5,6</sup> They are usually selected to be free from spherical aberrations rather than chromatic aberrations. For this reason, rear-illuminated copy boards should produce a monochromatic light, especially in a band that has a peaked response in the color spectra of the high resolution emulsion (see Reference 3). This is about 540 m $\mu$  (blue-green) (Figure 12-1).

<sup>2</sup>Eastman Kodak Co., Apparatus and Optical Division, 400 Plymouth Avenue N, Rochester, N. Y. 14605.

<sup>3</sup>Aero Service Corp., 210 East Courtland St., Philadelphia, Penn. 19120.

<sup>4</sup>Keuffel & Esser Co., New York, 300 Adams Street, Hoboken, New Jersey 07030.

<sup>5</sup>C. P. Goerz American Optical Co., 461 Doughty Blvd., Inwood, Long Island, N. Y. 11696.

<sup>6</sup>Eastman Kodak Co., Special Prod. Sales Dept., Apparatus and Optical Div., Rochester, New York 14650.



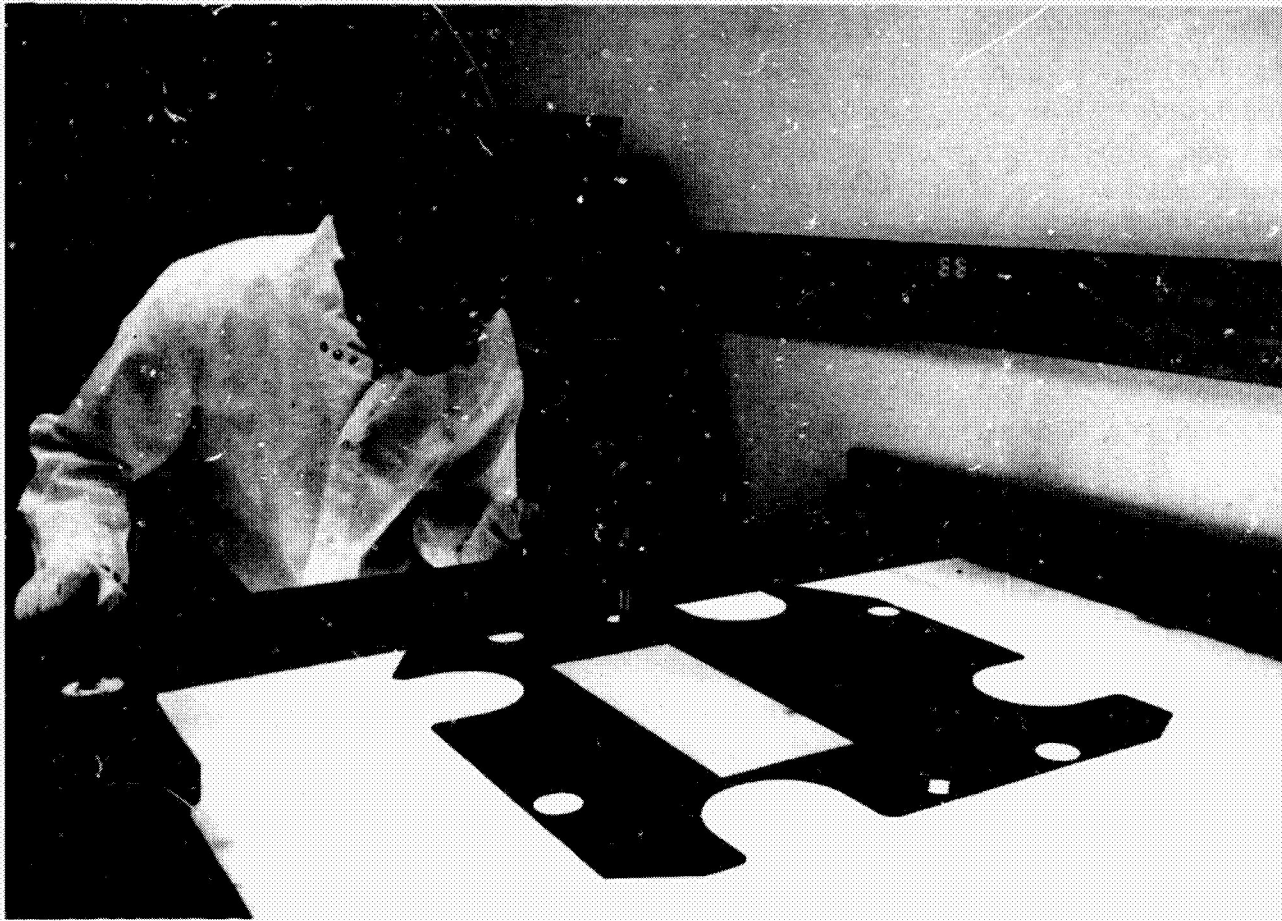


Figure 12-1—Artwork preparation on the X-Y coordinate.

A sharp image can only be obtained when the lens and all other lighted surfaces, especially the plate holder, are perfectly parallel to each other. The depth of focus is limited to about 2 mils, consequently very little out-of-plane error can be tolerated; otherwise a fuzzy image edge will be formed. A fuzzy edge can also be produced by vibration either through the floor or from a shutter on the lens mount. To avoid the latter problem, the copy board lights are usually switched on and off to make an exposure. Floor vibration coupled with long exposure times can cause distorted images and cause dimensions to increase or create soft image edges.

Precise focusing of the reduced image is best accomplished with a microscope mounted behind the plate holder and through the use of a slightly fogged plate. Ground glass image plates are not useful because the coarseness of the surface prevents precise examination of the image edges. If the microscope is a traveling type (i.e., traverses across the entire image) dimensional checks to within 0.1 mil are possible (Figure 12-2).

## PHOTORESISTS

Although seemingly a simple process, the application and processing of photoresists is subject

to more difficulties than any other operation. The difficulty is in no small part due to the manufacturer whose product varies from batch to batch. This is further complicated by the resist sensitivity to humidity, viscosity, and surface preparation. The microcircuit industry, in its quest for finer resolution, has been content with in-house processing of commercial resists to satisfy their needs. A comprehensive discussion of this type of processing will be available as a NASA report (see Reference 4).

Photosensitive resists are organic solutions which, when exposed to light of the proper wave length, change their solubility in an appropriate developer solution. There are two types: positive acting<sup>7</sup> and negative acting.<sup>8</sup> The positive acting resist is initially a polymer which is insoluble in the developing solution. During exposure to ultraviolet light the polymer becomes soluble. For negative acting resists the action is reversed. Of the two, the negative acting type is used most commonly and is resistant to most etch solutions.

It is of course desirable, in ultra high resolution work (0.1 mil widths), that the resist print be as sharp and clear as possible to accurately reproduce the original artwork (Figure 12-3). Even assuming perfect film processing and a resulting perfect image edge, some deterioration will occur during the contact printing operation. Light diffraction within the resist layer can become a significant factor particularly when the resist is thick (see Reference 5). Light scattering within the resist also occurs because of its solid globular content and the reflectivity of the surface to which the resist is applied. The net result of these factors is to expose the resist in an undesirable fashion and create an effect known as "coving" (see Reference 2). Figure 12-4 shows this effect on both positive and negative acting resists. Positive acting resists suffer less from this effect and are therefore potentially capable of improved resolution. Thinner resist layers minimize the coving effect but are sensitive to pinhole problems.

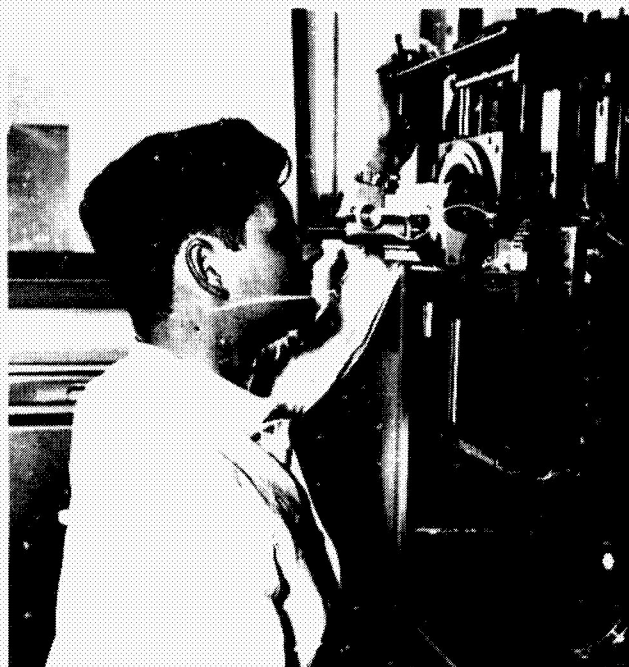


Figure 12-2—Focusing with the aid of a traveling microscope.

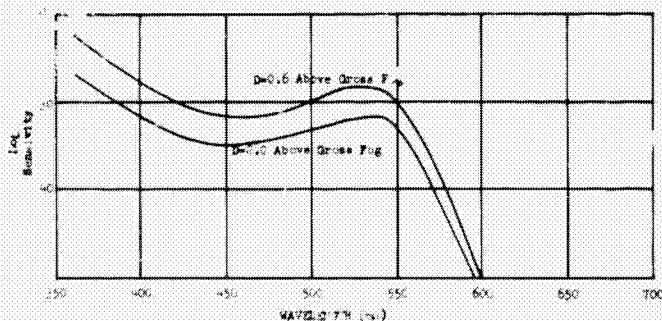


Figure 12-3—High resolution emulsion spectral response.

<sup>7</sup>AZ (Positop) Trademark of Shipley Co., Walnutpark, Wellesley, Mass. 02181.

<sup>8</sup>Kodak Photoresist, Kodak Metal Etch Resist Kodak Thin Film Resist, Trademark, Eastman Kodak Co., Rochester, New York.

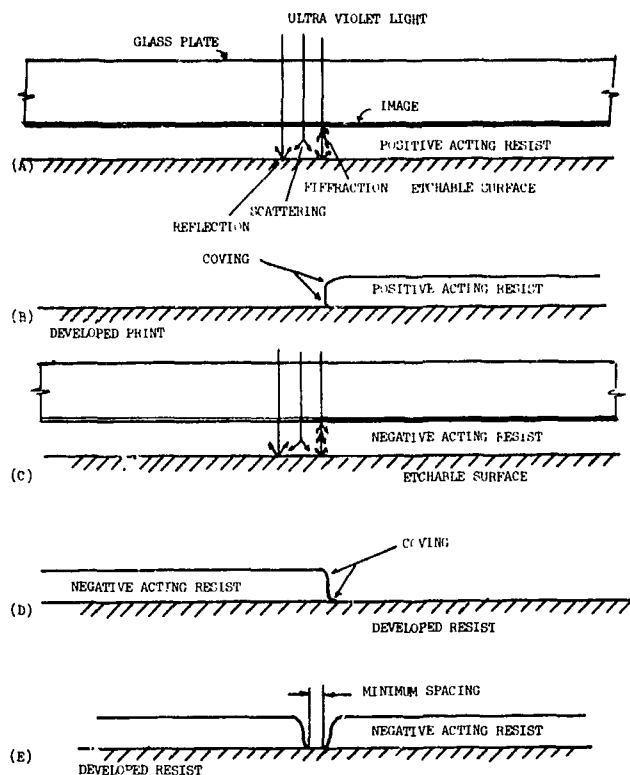


Figure 12-4—Coving effect in resists.

or series of them, becomes part of the finished circuit and, because of the elevated processing temperatures do a job that cannot be done easily, by any other means (Figure 12-5).

#### CONTACT OR SUBSTRUCTIVE MASKING (See Reference 7)

The metallization of silicon wafers by vacuum deposition and the subsequent etching to form a conductor pattern is also well known. However, less familiar is the use of this metallization as a deposition mask that is discarded after use. Diffused silicon resistors are limited in application by their high-temperature coefficient of resistance; but in their place, high-stability nickel-chrome resistors can be deposited by using the etched metallized film as

It is clear from the foregoing discussion that the resist industry, on which microminiaturization is based, has not kept pace with the developments in microcircuits. To satisfy the need for ultrasmall device geometries, new and better resists are required; and NASA should sponsor research in this area since it would benefit their programs as well as the entire semiconductor field.

#### MASKING TECHNIQUES ON SILICON WAFERS

Enough has been written concerning the fabrication of monolithic circuits to make most workers aware of the need to generate an oxide on the surface of a silicon wafer as a necessary step in the development of a circuit (see Reference 6). This oxide when etched to a desired pattern is used as a mask to delineate emitter, base, and collector regions as well as those of resistors, capacitors, and diodes. The mask,

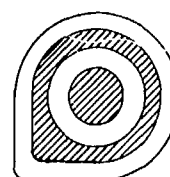
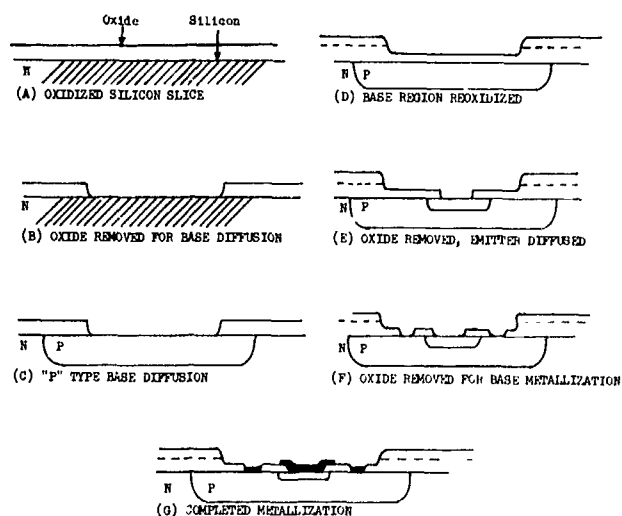


Figure 12-5—Silicon oxide masking technique.

a mask. After deposition, the metallized film is removed with an etch which does not attack the resistance film nor the silicon wafer. The wafer is then remetalized and a conductor pattern is etched to complete the circuit (Figure 12-6).<sup>9</sup> The in-situ mask technique is particularly useful for producing precision resistors, especially those less than one mil wide. At this narrow width the edge resolution exerts an ever-increasing influence on the resistor tolerance and photomasking is the only way this tolerance can be maintained.

The in-situ masking technique and variations of it are useful in optical and thin-film work as well. For example, a photomask which is durable and scratch resistant can be fabricated in this manner.<sup>10</sup> The same method is useful in producing reticles and other patterns on optical flats.<sup>11</sup> Its greatest use, however, is in thin-film circuits where it serves to eliminate the need for mechanical masks when only a small number of a circuit type are desired. The same artwork can always be used to make a set of mechanical masks if it is required. A variation of this technique permits the two deposition steps to be combined in one pumpdown. The resistance material is first deposited to the desired resistance and is immediately followed with the conductor material (copper or aluminum). A resist circuit pattern of conductors and resistors is applied, and an appropriate etch is used to remove all excess material. A new resist pattern consisting of only the conductor patterns is now applied, and the circuit is subjected to a selective etch which attacks the unprotected conductor metal above the resistors but nothing else (Figure 12-7). Thus, a circuit can be produced with prepared substrates using only the photomask to determine its design (see Reference 7).

Another variation of the in-situ mask technique is to anodize the undesired circuit areas into a nonconducting oxide rather than etch it away. As before, photomasking is used to delineate the circuit pattern (see Reference 8). If a resistant material such as tantalum is used, the anodization can be used to trim a resistor pattern to close tolerances. Capacitors are also possible when the oxide is limited to some portion of the thickness, and a vacuum-deposited upper plate is added

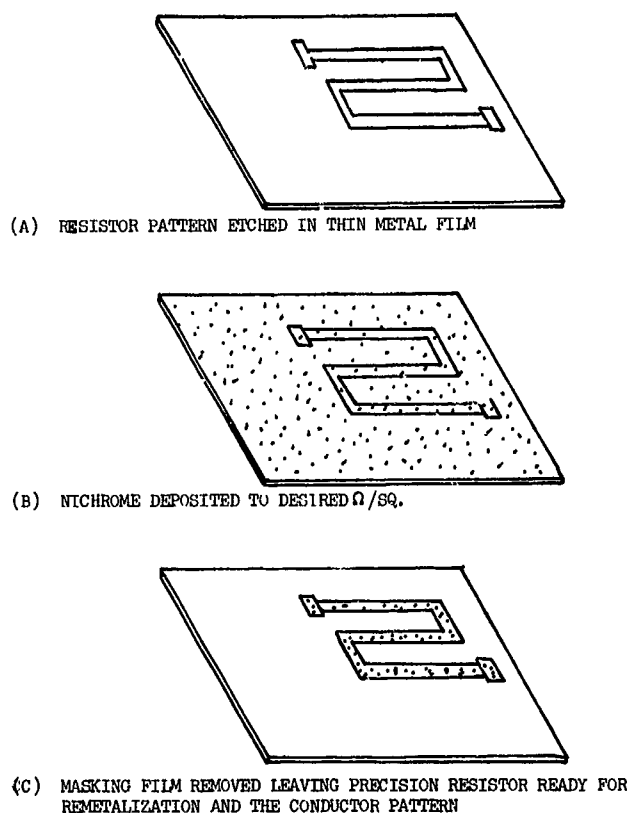


Figure 12-6—Precision Nichrome resistors on silicon wafers.

<sup>9</sup>The process details of this technique are included in the appendix.

<sup>10</sup>Vishay Instruments, Inc., 63 Lincoln Highway, Malvern, Pennsylvania 19355.

<sup>11</sup>Buckbee Meers Co., 245 E. Sixth St., St. Paul, Minn.

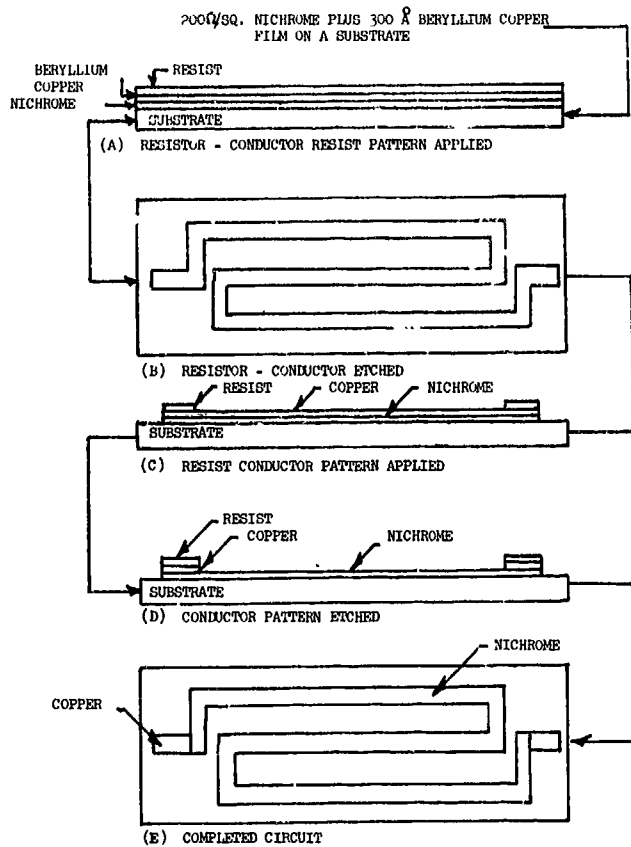


Figure 12-7—Resistor-conductor contact masks.

rectangular form with a constant thickness and vertical sides. Several things combine to prevent this from occurring with mechanical masks, and the geometrical form actually approximates a trapezoid. Hot molecules evaporated from a source arrive at the substrate and release some of their thermal energy. When enough energy is released, the molecules change from a vapor to a solid and serve as a nucleation site for later arriving molecules of the same material (see Reference 9). When enough of such sites are present and interconnected, the film is continuous and opaque. Since not all of the molecules condense when they first strike the substrate, their movement tends to feather the edge of a deposit, especially if the mask is not in good contact with the substrate (Figure 12-10). Also, atoms arriving at the substrate are not all arriving in straight lines from the

(Figure 12-8). The capacitors will be polarized unless they are connected in series. However, owing to the higher dielectric constant of tantalum oxide, the net capacity-per-unit-of-area will not be reduced. The primary advantage of in-situ masking is its excellent resolution—approaching an ideal mask. Its greatest disadvantages are its near limitation to resistive circuit elements only and the requirement for multiple wet-chemical operations.

## DEPOSITION EFFECTS OF MASKS

A perfect mask is one which has intimate contact with the substrate and whose thickness approximates the desired deposit thickness (Figure 12-9). If the deposit is applied in an even manner, the resulting film can approach a

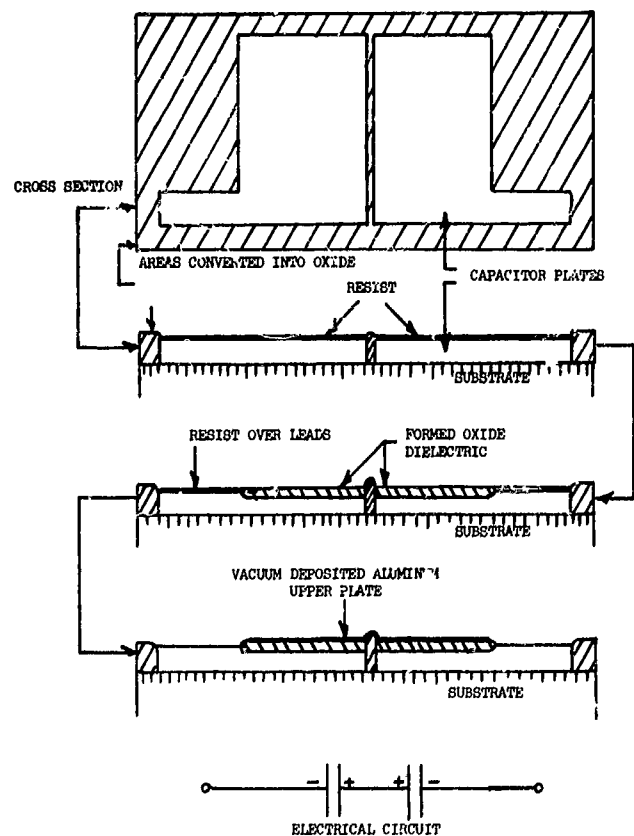


Figure 12-8—Anodized film capacitor.

source. Midway collisions with residual gas atoms or with each other cause this phenomenon. Rotating the substrate has been the best method used to even out the deposit, but this is difficult to do with a sequential masking operation.

## MECHANICAL MASKS

Mechanical masks are separate assemblies that must be positioned against the substrate for good resolution. A different one is required for each circuit pattern, but when loaded into a sequential deposition jig, they enable an entire circuit (resistors, capacitors, transistors, and diodes) to be fabricated in vacuum and in one pumpdown (Figure 12-11). The advantages of this technique are obvious in that the time lost through various resistng operations is eliminated. Extra time is required to produce the masks, but they can be made almost simultaneously and are durable and long lasting.

Mechanical masks are divided into two types: those which are etched, and those which are electroformed. Etched masks are simply thin foils which are masked with resist and subjected to an appropriate acid. The foil materials are varied from easily etched metals like beryllium copper to alloys such as stainless steel and Invar (see Reference 10) to refractory metals such as molybdenum. Pure copper is too soft to be of practical value as a mask, but an alloy of copper and beryllium produce a stiff material which is very suitable. The advantage of this material is that it is easily etched, and masks can be made very quickly and inexpensively. If a spray etcher is used with ferric chloride, the center etched edge is all but eliminated. The action of the spray continually removed the material at an even rate and produces an aperture with nearly vertical walls.<sup>12</sup> Alloys of stainless steel are also popular although etches for this group tend to be preferential according to the alloys and produce a jagged edge (see Reference 11).

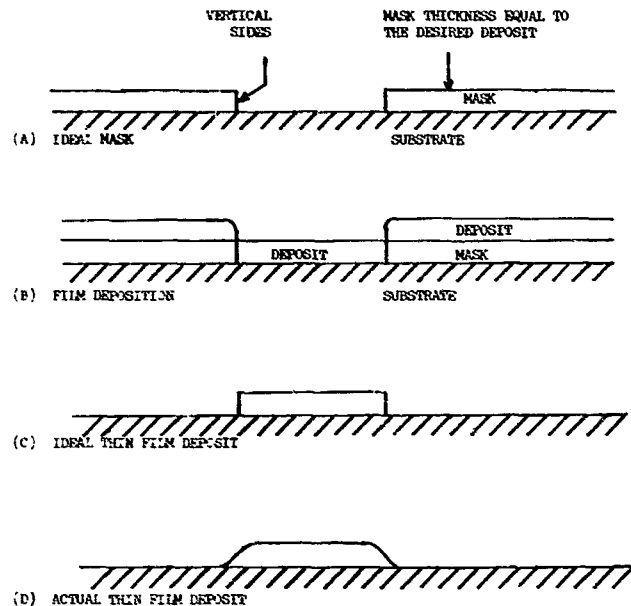


Figure 12-9—The ideal mask.

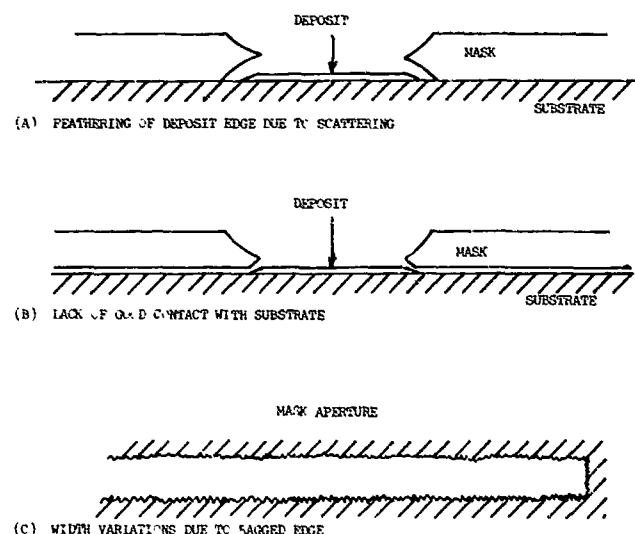


Figure 12-10—Mechanical masking problems.

<sup>12</sup>The process details for this technique are included in the appendix.



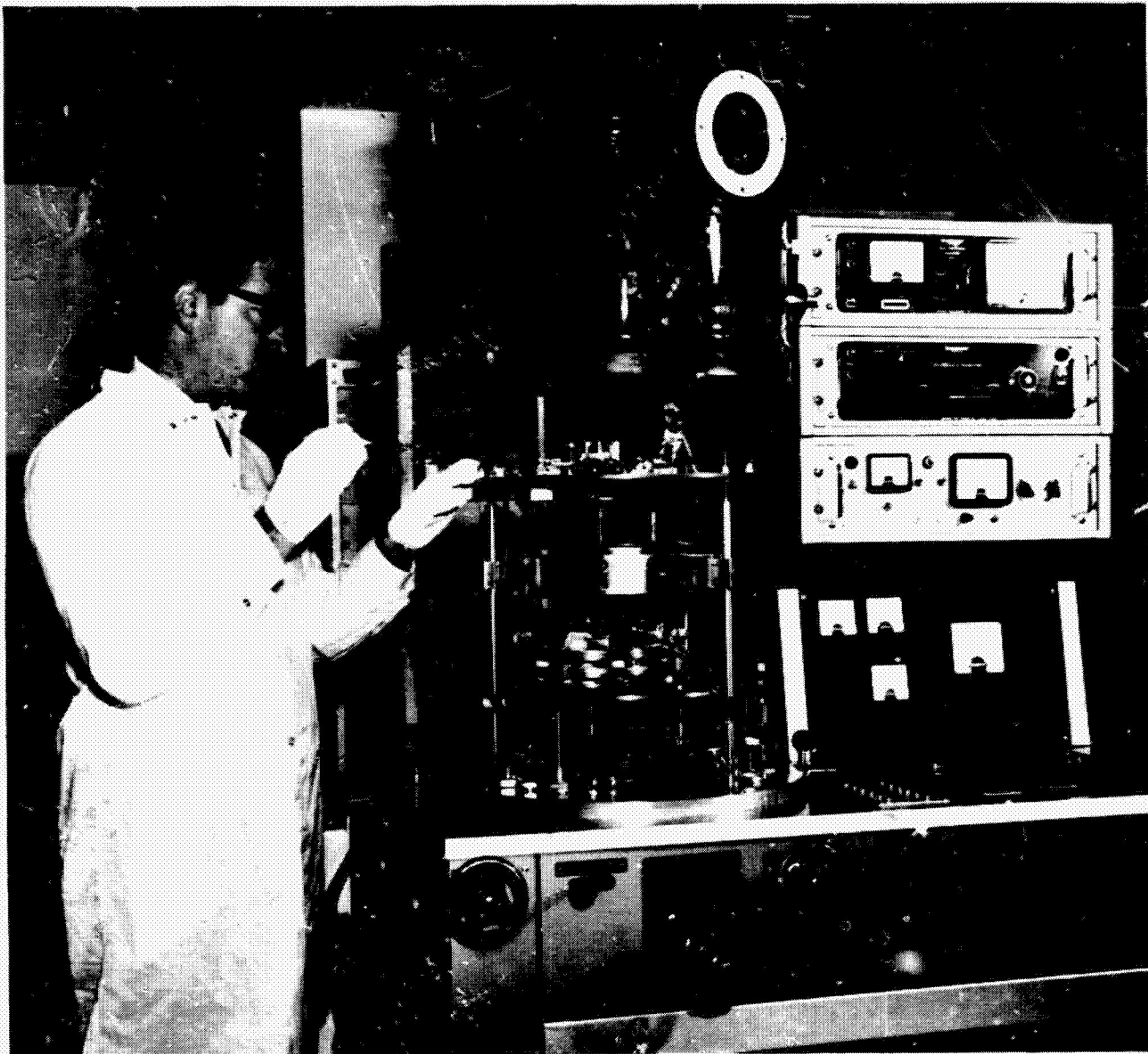


Figure 12-11—The sequential vacuum deposition jig.

The latest group of metals which have been used as masks are the refractories such as molybdenum. Molybdenum has the advantage of stiffness even as a thin foil (e.g., 2 mils) and a low temperature coefficient of expansion, therefore it is best for high-temperature work. Its primary disadvantage is high cost and the violent etches required to make the masks. The resulting resolution, caused by the acid attack on the metal and the resist, is poor. Masks, when etched in a beaker, tend to produce a feather edge in the middle of an aperture<sup>13</sup> (Figure 12-12). This presents a raggedness which diffuses the edge of the pattern. The problem can be reduced somewhat by spraying the etch and by etching one side separately from the other. With spray etching, the metal

<sup>13</sup> The process details for this technique are included in the appendix.

is attacked vertically more so than horizontally, and the jaggedness is not as prevalent. With violent etches, however, spraying is not practical for safety reasons. Commercial mask suppliers<sup>14</sup> have proprietary techniques which apparently overcome the edge problem in molybdenum masks.

Electroetching has been used to assist in etching refractory metals, although this technique is not widely used and is thought to cause deterioration of the resist edge (see Reference 11).

The thickness of a mask determines its resolution. To improve resolution, a thinner foil is required, but as foils become thinner they are no longer self-supporting and will not position tightly against a substrate. The use of foils with harder compositions is the solution, but they are more difficult to etch and are more costly. One answer to supporting the thin foils is to use a separate mask support of a thicker metal with enlarged apertures corresponding to those in a mask. This is at best a compromise since it involves far more expense and time. The mask support, however, does guarantee intimate contact with the substrate, especially if the substrate is weighted. Maintaining intimate contact with a substrate is possible if the masks have a slight bow in the direction of the substrate.

The composite mask overcomes the disadvantage of support problems with thin etched foils, but it retains the inherent improvement in resolution. A thin foil still defines the pattern, but it is now supported with a heavier backing material which is an integral part of the mask. Also, the foil edge is plated—rather than etched—which produces a smoother finish. The masks are made by preparing a piece of beryllium copper 0.005 to 0.010 inch thick and plating 0.0005 to 0.001 inch of nickel on one side. Photoresist is used to define the desired aperture pattern and, being non-conductive, prevents nickel from adhering where it is present (Figure 12-13). The masks are usually made two at a time and taped back-to-back, to prevent nickel from being plated on the back sides. The process details for this technique are included in the Appendix. Upon completion of the plating phase, the masks are resisted on the opposite side in all areas except behind the aperture enclosed by the nickel-plating on the front side. Accurate registration is required as well as a complementary set of negatives (light and dark field). When etched, the copper will be removed from the aperture and because of undercutting, will relieve the nickel foil evenly around the edge (Figure 12-14).

An electroformed mask requires more time to prepare, but it overcomes the disadvantages of very thin etched foils. The coefficient of expansion of the nickel is close to that of the beryllium

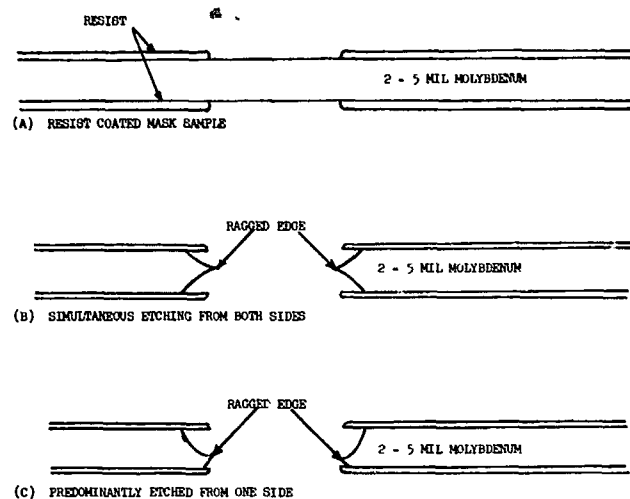


Figure 12-12—Aperture edges of molybdenum masks.

<sup>14</sup>Buckbee Mears Co., 245 E. Sixth St., St. Paul, Minn.



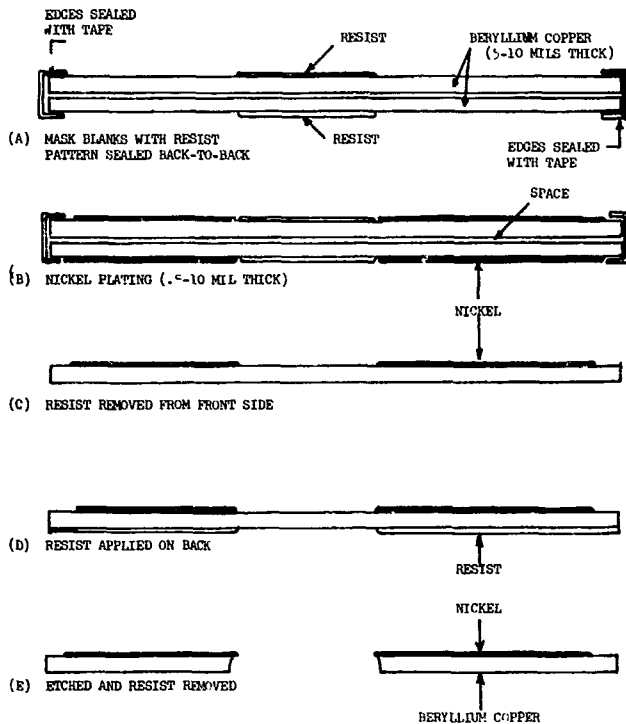


Figure 12-13—Electroformed nickel mask fabrication.

## CONCLUDING REMARKS

Precision microcircuit masking will continue to be one of the most important factors in microcircuit development. Sophisticated

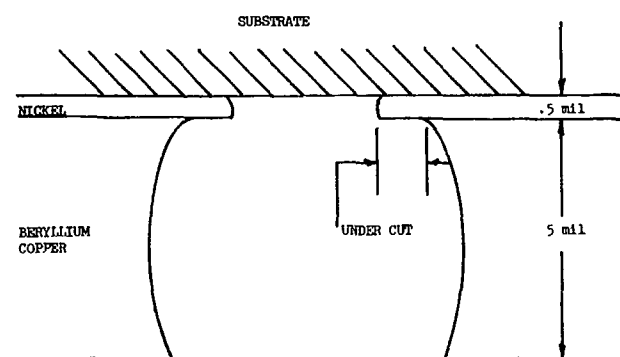


Figure 12-14—Cross-section of an electroformed mask,

copper, and minimum buckling occurs. The masks have been used successfully in temperatures up to 250° C with good results.

## SHADOW MASKING

Shadow masking is a technique which has come into much use lately with the development of thin-field effect transistors. It is a variation of mechanical masking in that it uses an aperture to define a general pattern and a fine obstruction, usually a wire, for a mask. The pattern most commonly made with this mask is the spacing between the source and drain electrodes. The wires are useful for making other elements, however; and as many as 1080 components have been fabricated with a complex mask (see Reference 12). Figure 12-15 shows this mask concept and a typical deposition performed through it.

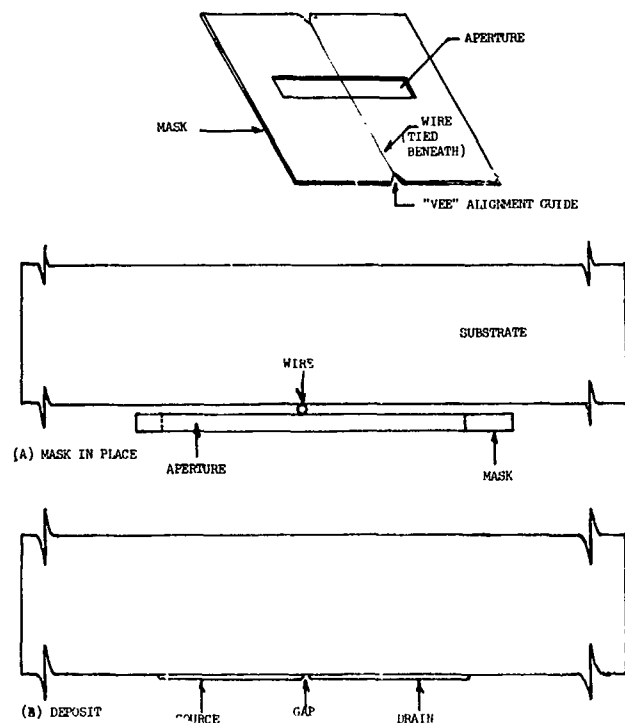


Figure 12-15—Shadow masking.

techniques involving the use of programmed electron beams to expose resist patterns too small for conventional optics are already being considered by designers. Contact and mechanical masks will not be made obsolete by this advance but will instead be enhanced by it as thin-film substrates become interconnect boards for silicon chips.

It is hoped this paper has been of interest to those familiar with masking and of value to those not familiar but interested in duplicating the techniques.

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3. Eastman Kodak Company, "Techniques of Microphotography," Industrial Data Book, p 52, 1963.
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5. Lathrop, J. W., "Semiconductor-Network Technology," Proc. IEEE, Vol. 52, No. 12, pp 1430-1444.
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12. Weimer, P. K., et al, "Integrated Thin Film Scan Generator," Proc. IEEE, Vol. 54, p 345, March 1966.

## APPENDIX Microcircuit Fabrication Laboratory Procedure Process

### Contact Masks

1. Vacuum deposit 300 Å of beryllium copper on a cleaned substrate at room temperature.
2. Immediately, upon removal from the vacuum evaporator, mount the coated substrate on the high-speed whirl coater. Apply 15 drops of refined photoresist and whirl the substrate at 300 rpm for 15 seconds until the interference colors stop changing.
3. Dry for 2 minutes in a dust-free oven at 100°C.
4. Expose for 2 minutes in a vacuum frame through a photomaster.
5. Develop with a spray until all unexposed resist has been removed.
6. Rinse well with filtered methanol and bake at 100°C for 5 to 10 minutes.
7. Etch over a light table holding the substrate flat with tweezers in the following solution:
  - 60 percent by wt. ethyl alcohol
  - 30 percent by wt. ethylene glycol
  - 10 percent by wt. ferric chloride (42° BE)
13. Rinse with methanol and blow dry with filtered gaseous nitrogen.
14. Soak in "stripper 99" (see Reference 1) for 2 minutes, and then swab gently to remove all exposed resist.
15. Rinse with filtered acetone with running deionized water.
16. Dry for 5 minutes at 100°C in a dust-free oven.
17. Deposit nichrome to the desired resistance with substrate temperature of 200°C.
18. Dip in concentrated nitric acid solution until the copper disappears.
19. Rinse in deionized water and blow dry with filtered gaseous nitrogen.

(NOTE: Aluminum may be used, in which case the etch would be a weak solution of sodium hydroxide.)

Reference:

1. Formula "99" Stripper "K", Arnold Laboratories  
7103 Laurel Canyon Blvd.  
North Hollywood, Calif.

Beryllium Copper Masks

1. With DiAcro shear, cut beryllium copper foil (0.005 inch) to roughly one-fourth inch larger than finished mask. (Do not use scissors because they leave a rough edge.)
2. Wash with acetone to remove mill lubricant.
3. Clean both sides with "scrub cleaner 70" (see Reference 1) until the surfaces are wet all over. Use gloves and a sponge to avoid contamination with finger oils.
4. Wash in filtered deionized running water, making sure all abrasive powder is removed.
5. Blow dry with filtered gaseous nitrogen.
6. Vapor degrease with trichloroethylene and dry in a dust-proof area at room temperature.
7. Coat both sides with metal etch resist (see Reference 2) applied through a 10-micron filter and whirl at 75 rpm for 30 minutes.
8. Remove sample from the whirl coater and bake in a dust-free oven at 100°C for 4 minutes to dry the resist.
9. Expose the sample through the required photomasters for 3 minutes using the vacuum contact printer.
10. Repeat the print operation, maintaining registration, to expose the opposite side.
11. Develop the image for 2 minutes at room temperature in metal etch resist developer (see Reference 3). Complete development with a gentle spray of fresh developer solution. All visible unexposed resist must be removed.
12. Bake processed image at 100°C for 20 minutes.
13. Spray etch with 42° Baume ferric chloride solution or "high speed etch" (see Reference 4) until the pattern is just cut through.
14. Wash with filtered deionized running water and dry.

15. Remove resist with "stripper 99" (see Reference 5) by soaking for 30 minutes, and brushing gently with a cotton swab at the end of this time.
16. Wash with acetone and then deionized water until the sample is clean.
17. Cut sample to size with DiAcro shear.
18. Dry sample and immerse for 5 to 10 minutes in "cuposit EL-221" (see Reference 6) gold-plating solution.

#### References:

- |                                  |  |
|----------------------------------|--|
| 1. Scrub cleaner 70              | Shipley Company, Inc.<br>2300 Washington Street<br>Newton, Massachusetts 02162                             |
| 6. Cuposit EL-221                |  |
| 2. Metal etch resist             | Eastman Kodak Co.<br>Apparatus and Optical Division<br>400 Plymouth Avenue N.<br>Rochester, New York 14605 |
| 3. Metal etch resistor developer |  |
| 4. High-speed etch solution      | Philip A. Hunt Chemical Co.<br>Palisades Park, New Jersey  |
| 5. Formula "99" Stripper "K"     | Arnold Laboratories<br>7103 Laurel Canyon Blvd.<br>North Hollywood, California                             |

#### Molybdenum Masks

1. With DiAcro shear, cut sheet molybdenum foil 0.002 to 0.005 inch to roughly one-fourth inch larger than finished mask. (Do not use scissors because they leave a rough edge.)
2. through 12. Repeat these steps as they were performed in the beryllium copper mask procedure.
13. Etch mask in the following solution:
  - 3 parts water, deionized.
  - 1 part sulfuric acid.
  - 1 part nitric acid.

(NOTE: A reaction occurs upon complete mixing of this solution and reaches 180°F. Use a face mask, rubber gloves, and a rubber apron for safety. Always mix the solution in large openmouth beakers under a vented fume hood. Allow the solution to cool to 100°F before etching.)

14. Use plastic or rubber-protected tongs to hold the mask in the etch solution. The etching is violent and rapid; therefore, caution should be exercised to avoid over-etching. Rinse with running deionized water.
15. Remove resist with "stripper 99" (see Reference 1) by soaking for 30 minutes; at the end of this time, brush gently with a cotton swab.
16. Wash with acetone and deionized water until clean.
17. Cut to size with DiAcro shear.

Reference:

1. Formula "99" Stripper "K"      Arnold Laboratories  
7103 Laurel Canyon Blvd.  
North Hollywood, California

Electroformed Masks

1. through 6. Repeat the first 6 steps of the beryllium copper mask procedure for the electroformed masks.
7. Clean plate in electrocleaner solution (see Reference 1) for 60 seconds with the stainless steel tank as the anode at 4 to 5 volts dc. Solution temperature should be 70°C. Rinse thoroughly with deionized water.
8. Dip plate deoxidizer for 10 to 15 seconds, rinse with running deionized water, and blow dry with filtered gaseous nitrogen.
9. Bake at 50°C for 5 minutes.
10. through 16. Repeat steps 7 through 12 of the beryllium copper mask procedure.
17. Tape two plates back-to-back around the edges being careful to avoid scratching the inner resist coating. The plating solution must not penetrate the space between the two masks nor should finger oils contaminate the surface to be plated.
18. Dip in deoxidizer solution for 5 to 10 seconds, rinse with running deionized water, and transfer to the electroforming solution (see Reference 2).
19. Adjust plating current to 10 amperes per square foot and plate for 2 hours (1 mil nickel). The plating solution must be stirred constantly and maintained at 45°C.

20. Remove masks, rinse thoroughly, blow dry, and inspect for plating nodules. Pick off any with a sharp instrument using care to avoid scratching the electroformed areas.
21. Using rubber-coated tongs, immerse the masks in Ethone #36 (see Reference 3) etch until the apertures appear, and then rinse instantly in running deionized water.
22. Inspect mask to determine if the etching is complete. Approximately 5 mils of relief in the copper should appear around each aperture.
23. Repeat step 22, if required.
24. through 29. Repeat steps 14 through 18 of the beryllium copper mask procedure.

#### References:

- |   |  |
|---|--|
| <ol style="list-style-type: none"> <li>1. Ethone #160<br/>(37-1/2 to 52-1/2 G/L)</li> </ol>   | Udyllite Corp.<br>3628 E. Olympic Blvd.<br>Los Angeles, California 90023 |
| <ol style="list-style-type: none"> <li>3. Ethone #36<br/>(340 to 380 G/L)</li> </ol>  |  |
| <ol style="list-style-type: none"> <li>2. Sulfamate Nickel Sol.<br/>(450 to 517 G/L nickel sulfamate +30 G/L boric acid<br/>+38 G/L min. NaLauryl sulfonate)<br/>Ph 3.5 to 4.5</li> </ol> | Udyllite Corp.   |

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**N67-32575**

### **13. SURFACE EFFECTS IN SEMICONDUCTORS DUE TO EVAPORATION TECHNIQUES**

**J. C. Lyons and D. R. Dargo  
Goddard Space Flight Center  
Greenbelt, Maryland**

In the course of semiconductor device fabrication a number of phenomena have been encountered and observed which have a direct bearing on the operating characteristics of the device being fabricated.

Two of these phenomena are:

- (1) Gain increase in a planar transistor after the silicon dioxide passivated surface has been coated with lead oxide and annealed and
- (2) Differences in gain and stability of transistors which have had aluminum interconnections evaporated from an electron beam and from a tungsten filament.

Among the problems encountered in the fabrication of silicon planar transistors, the formation of inversion layers in the P base of an NPN device is one of the most troublesome. This channeling effect, which creates leakage between the emitter and the collector, results in relatively low transistor gain. It is usually caused by one of several sources:

- (1) Inherent contamination in the silicon dioxide over the base region may cause charges to be present in the oxide which create an artificial N channel between the emitter and the collector.
- (2) Aluminum interconnections which run on the oxide across a lightly doped region may induce channels in the same way that MOS devices have induced channels.
- (3) When oxidizing a P-type silicon surface, an oxide system containing silicon dioxide and silicon monoxide is formed which is believed to have a deficiency of oxygen vacancies producing positive charges in the oxide. These charges in turn attract to the surface any free electrons which might be in the P material, causing a shallow N-inversion layer.

To eliminate the positive charge phenomena, oxygen must be added to the system. One method of doing this is by means of evaporating approximately 1,000 angstroms of lead oxide onto the silicon dioxide surface and annealing the wafer at 600°C. This process is performed immediately after the contact windows have been photoengraved and before aluminum has been deposited on the

wafer. The contact windows must be reopened after annealing by removing the lead oxide which has been evaporated onto them. The normal aluminum evaporation can then be performed. It has been found that this process has increased the gains of low-signal transistors tenfold, from 20 to 200, with a base current of one microampere. Several transistors with narrow base regions have been fabricated with gains in excess of 1000 at that current level, with the emitter-to-collector leakage in the order of 1 nano-ampere.

In published literature on the fabrication of more stable MOSFET devices, it has been stated that aluminum interconnections should be made by means of an electron beam evaporation rather than a filament evaporation. The reason for this is that a filament, when heated, deposits some sodium along with the aluminum onto the silicon dioxide surface. During the subsequent alloying process, this sodium migrates into the oxide and causes a positive charge, tending to make the surface more N-type.

Several months ago when working on a group of MOSFET devices along with some bipolar transistors, aluminum was evaporated onto some bipolar units by means of an electron beam. These units were compared with another group of bipolars which had been annealed by lead oxide processes and which contained filament-evaporated aluminum. The latter units behaved as anticipated, displaying high gains and low leakages. The electron beam-treated units showed moderately high gains and corresponding low leakages. When the two groups were packaged, however, the lead oxide, filament-treated units were found to decrease about 20 percent in gain during each high-temperature operation, (die bonding, ballbonding, etc.) while the electron beam-evaporated units increased in gain during each similar subsequent high-temperature operation. After several temperature cycles, the latter units stabilized at a higher gain than the filament units. These results indicate that electron beam-evaporation simplifies the fabrication of bipolar integrated circuits, while high-gain and low-leakage characteristics are retained.

**N67-51576**

**14. THE PROCESSING OF SCREENED RESISTORS ON CERAMIC SUBSTRATES**

**R. L. Stermer, Jr.  
Langley Research Center  
Langley Station, Hampton, Virginia**

Experimentation with a small pilot process for the fabrication of screened circuits on alumina substrate revealed that deposition blooming was nearly independent of deposition area from 0.030-inch to 0.050-inch line width. It further showed that minimum resistance change under electrical power load at atmospheric and vacuum pressures could be achieved with circuits fired at 1400°F on a belt moving through the curing oven at a rate of 1 inch per second. Thermal and mechanical shock testing showed that conservative applications of solder on contact points physically distributed on the substrate provided satisfactory physical integrity with no measurable resistance change during testing. These results indicate that a pilot process has been established with the capability of producing screened circuits having excellent reproducible characteristics within acceptable limits.

**INTRODUCTION**

Screen deposition is a process in which thick films of inks or cermets are deposited and fired on a substrate to form a compatible all-ceramic passive network. A hybrid screened circuit is made by bonding discrete active components into the network. A typical screened circuit is shown in Figure 14-1. As can be seen, all passive components are deposited films, and the active devices are soldered onto the substrate.

One of the principal problems in developing a technology to fabricate screened circuits is the design of a process to produce screened resistors within the desired mechanical and electrical specifications. The objective of this paper is to consider this problem for the case of a small pilot operation. The problem can be broken into two areas: First, resistor geometry control, and second, the control of the curing or firing environment.

**PROCESS DESCRIPTION**

A resistor is fabricated by means of the controlled deposition and firing of electrode and resistor compositions on a substrate. These compositions are pastes made by the suspension of

metals, metal oxides, and glass in an organic binder. The specific compositions used in this work were the silver-palladium (see Reference 1) resistor and gold-platinum (see Reference 2) electroding compositions. The substrate material is 96 percent alumina.

The resistor geometry is deposited on the substrate by forcing the compositions through a stainless-steel screen masked with a photoemulsion. The material passing through the screen is printed on the substrate. The deposited geometry is cured in a high-temperature firing process to obtain the desired properties. Figure 14-2 is a block diagram of this process.

The first step is the preparation of the screen stencil. A screen is stretched taut over a steel frame and coated with a photosensitive emulsion. The photoemulsion is exposed to ultraviolet rays passing through a glass slide positive of the desired geometry. The exposed areas harden, while the unexposed areas wash out quite readily with hot water.

Figure 14-3 is a photograph of the screen press. The screen stencil is mounted in the press. Parallelism and screen height are adjusted by micrometers located on the press. A 0.002-inch compression of the squeegee is set by using a 0.001-inch mylar film as a feeler gage between the substrate and the screen. After this dimension has been determined, the squeegee is moved down another 0.003 inch. The resistor composition is then fired in a tunnel kiln at a peak temperature of 1400° F for a duration of 40 minutes. The conductor is fired in a periodic kiln since its firing temperature is less critical than that of the resistor films.

#### DIMENSION COMPENSATION

As the resistor is processed, errors are introduced into its dimensions. As can be seen in Figure 14-4, the resistor and conductor materials have a tendency to bloom or spread as the network is processed. Analysis of variations in width and length indicates that from 0.030- to 0.050-inch line width, the blooming is nearly independent of deposition area. Looking

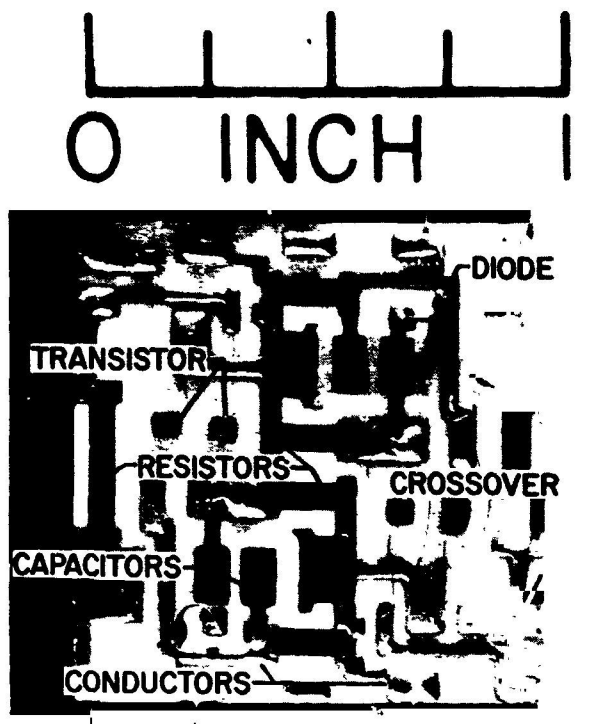


Figure 14-1—Typical screened circuit.

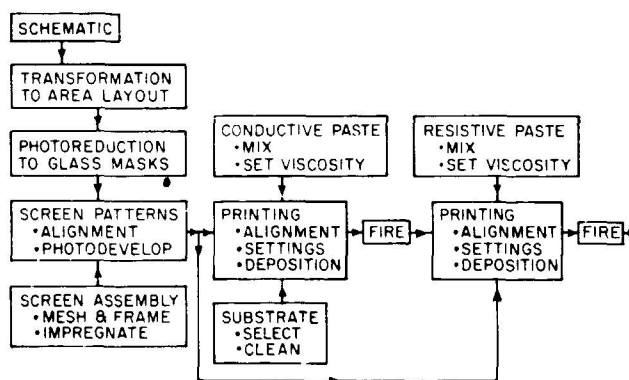


Figure 14-2—Screen circuit process block diagram.

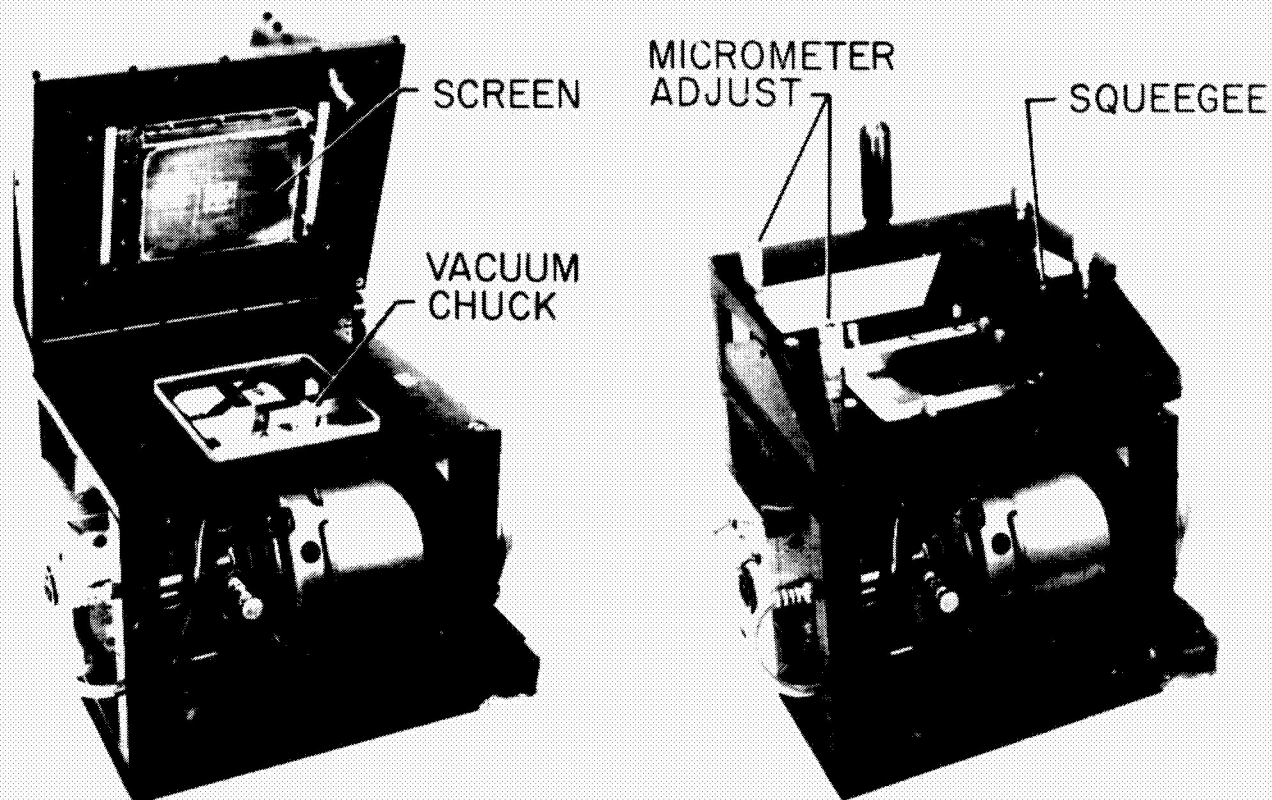


Figure 14-3—Screen printing press.

again at Figure 14-4, a correction factor  $k$  can be defined as the average deviation in the dimension. As can be seen,  $k$  has about the same value for length and width so that

$$-\Delta L = \Delta w = k. \quad (1)$$

This correction factor can be applied to the resistivity equation in the following manner.

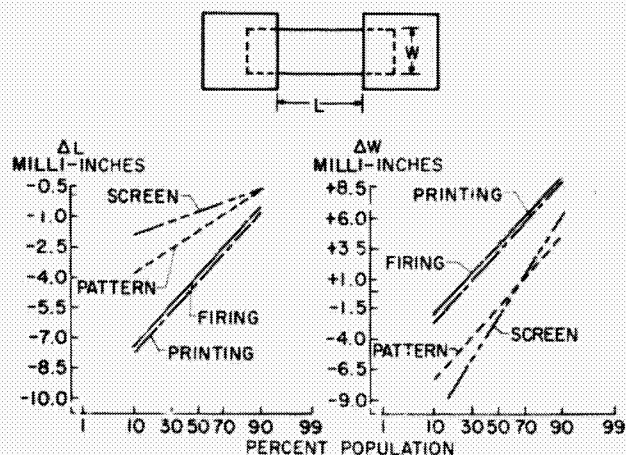


Figure 14-4—Accumulation of dimensional error.

Let  $\sigma'$  be a corrected sheet resistivity (that is, a design sheet resistivity different from the actual resistivity by some  $\Delta\sigma$  which exactly compensates for the nominal variations in dimensions). Then,

$$\sigma = \sigma' + \Delta\sigma, \quad (2)$$

where  $\sigma$  is the true sheet resistivity. Write the fractional variation of resistance equation, setting the deviation in resistance to zero:

$$\frac{\Delta R}{R} = \frac{\Delta\sigma}{\sigma} + \frac{\Delta L}{L} - \frac{\Delta w}{w} = 0. \quad (3)$$

Solving for  $\Delta\sigma$ ,

$$\Delta\sigma = -\frac{\Delta L}{L} - \frac{\Delta\omega}{\omega} \sigma. \quad (4)$$

The corrected sheet resistivity  $\sigma'$  can be obtained by substituting Equation 4 into Equation 2 and solving for  $\sigma'$ :

$$\sigma' = \left[ 1 + \left( \frac{\Delta L}{L} - \frac{\Delta\omega}{\omega} \right) \right] \sigma \quad (5)$$

Recalling Equation 1, arrived at from the data,

$$\sigma' = \left[ 1 - k \left( \frac{1}{L} + \frac{1}{\omega} \right) \right] \sigma \quad (6)$$

Now the corrected resistor design equation can be formed:

$$R = \sigma' \frac{L}{\omega} = \left[ 1 - k \left( \frac{1}{L} + \frac{1}{\omega} \right) \right] \sigma \frac{L}{\omega}. \quad (7)$$

Using this equation, a table of resistance values for given dimensions was computed. At the present time, over 1000 resistors have been designed and processed using this equation. The resulting resistance distribution is shown in Figure 14-5. As the figure indicates, 60 percent of all resistors processed fall within  $\pm 10$  percent of design value. Another 20 percent of the processed resistors fall in the range between -20 percent and -10 percent. These can be trimmed within tolerance. As can be seen in the figure, the design nominal is biased at a -5 percent to weigh the distribution on the low side to increase trimmable resistor yield.

## FIRING ENVIRONMENT

Figure 14-6 shows a tunnel kiln fabricated to fire the resistor compositions. This kiln has a 40-inch tunnel with a thermocouple located in the center approximately one-half inch above the belt. The temperature at the thermocouple was controlled using silicon-control rectifiers with proportional control. The zones on either side of the center were connected electrically so that about one-half center zone power was divided between the side zones. The resulting temperature profile is shown in Figure 14-6. This profile was taken with a belt speed of 1/4 inch per minute to minimize loading effects due to injection of a cold belt.

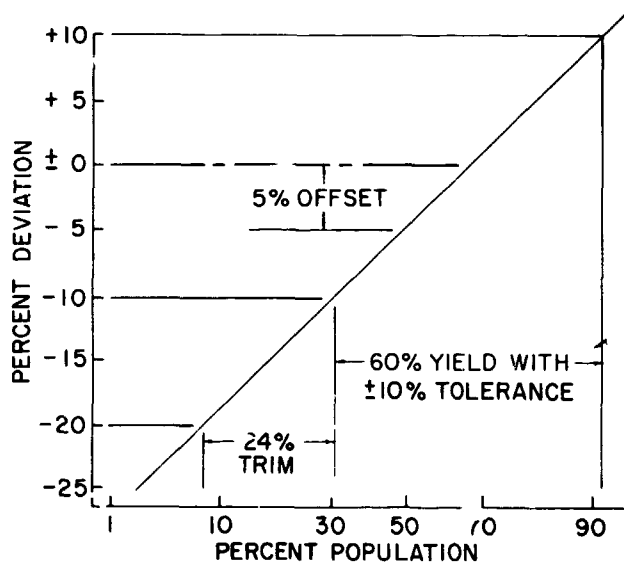


Figure 14-5—Distribution of resistance values.



TUNNEL KILN

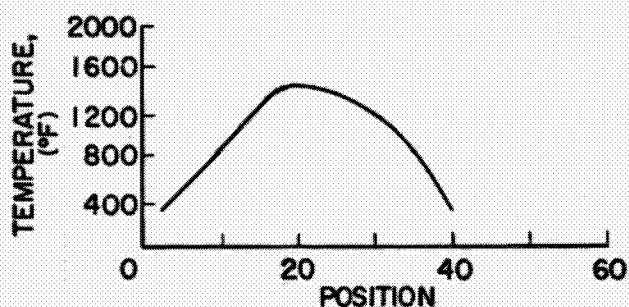


Figure 14-6—Temperature profile for tunnel kiln.

coefficient of resistance (TCR) versus peak firing temperature curve. The top curve represents the average value of TCR in the range 25 to 100° C, and the bottom curve represents the average value between -10 and +25° C.

After determining the basic physical characteristics of noise, TCR, and resistivity, it was observed that the resistivity drift was strongly dependent on the peak firing temperature. Samples were fired in the 1200 to 1450° F range to determine this dependence. Figure 14-9 indicates the change in sheet resistivity as a function of firing temperature with humidity as a forcing function. The ordinate is the percent change due to the environment. In this test, samples were placed in hot water (170° F) for 24 hours and then air dried on a hot plate at 200° F. Figure 14-9 also represents the change in sheet resistivity versus firing temperature using normal handling as a

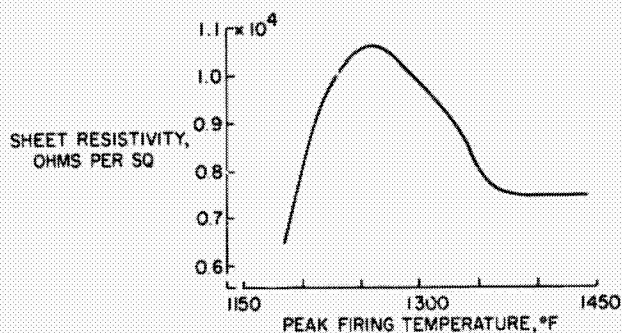


Figure 14-7—Evaluation of physical properties—resistivity.

Sample resistor lots were fired in the kiln at 25° F increments in the range of 1200 to 1450° F using a constant belt speed of 1 inch per minute. Data were taken to determine the characteristics obtained by the firings.

Figure 14-7 represents the variations in sheet resistivity as a function of firing temperature. This curve indicates that in the vicinity of 1400° F, the resistivity becomes relatively independent of peak firing temperature. Resistor current noise was measured in accordance with MIL-STD-202C. Figure 14-8 shows the resulting curve of noise versus firing temperature. Minimum noise resulted for firing temperatures above 1350° F. Two resistors were selected from each firing at temperatures between 1200° F and 1450° F, for measurement of the temperature coefficient of resistance. Figure 14-8 also indicates the resulting temperature

coefficient of resistance (TCR) versus peak firing temperature curve. The top curve represents the average value of TCR in the range 25 to 100° C, and the bottom curve represents the average value between -10 and +25° C. After determining the basic physical characteristics of noise, TCR, and resistivity, it was observed that the resistivity drift was strongly dependent on the peak firing temperature. Samples were fired in the 1200 to 1450° F range to determine this dependence. Figure 14-9 indicates the change in sheet resistivity as a function of firing temperature with humidity as a forcing function. The ordinate is the percent change due to the environment. In this test, samples were placed in hot water (170° F) for 24 hours and then air dried on a hot plate at 200° F. Figure 14-9 also represents the change in sheet resistivity versus firing temperature using normal handling as a forcing function. Normal handling is defined as one dip solder cycle; two temperature cycles between +60 and -25° C; and exposure to room temperature, dust, and humidity for 400 hours. Again, it is seen that as the peak firing temperature goes above approximately 1350° F, little drift is experienced.

A test was performed to establish the material stability under power load and vacuum. Areas of possible concern were the loss of oxygen from the resistor because of low oxygen partial

$$TCR = \frac{R_t - R_r}{R_r \Delta t} \times 10^6, \text{ PPM}$$

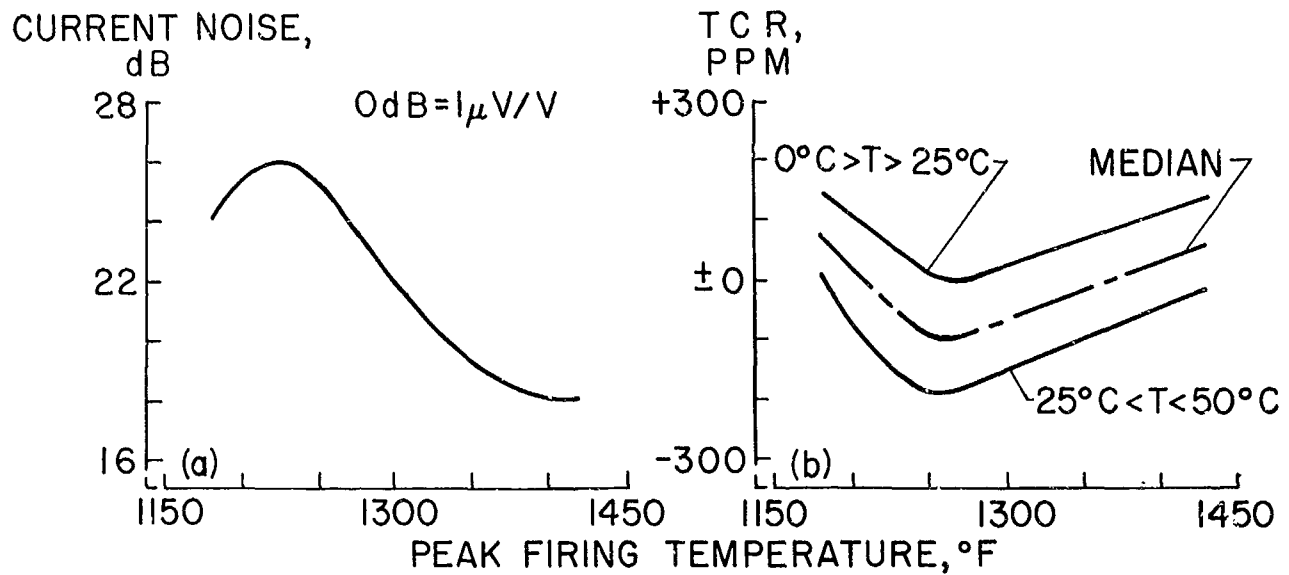


Figure 14-8—Evaluation of physical properties—current noise and TCR.

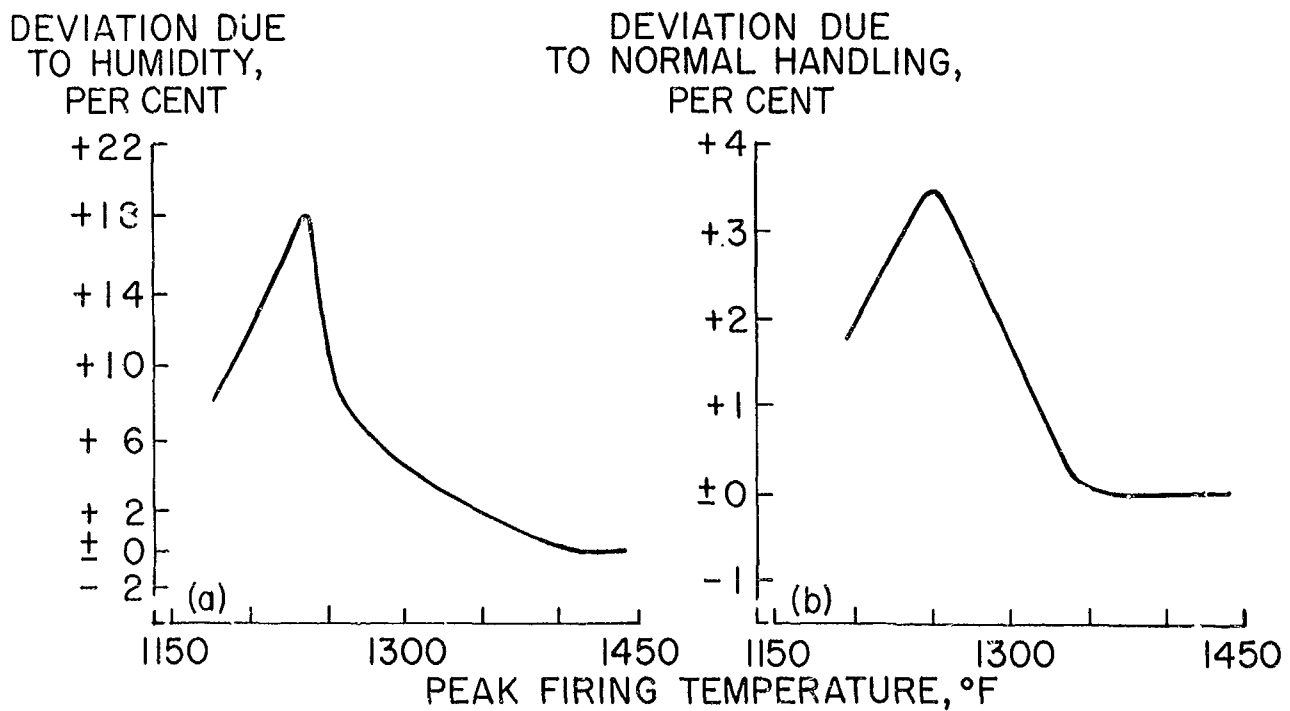


Figure 14-9—Evaluation of environmental characteristics.



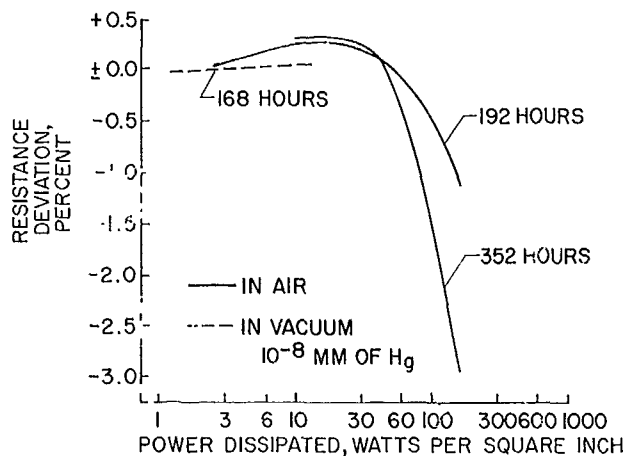


Figure 14-10—Resistance deviation due to power level for resistors fired at 1400°F.

pressures which may exist within the resistor and the possibility of chemical change which could be excited by elevated temperatures due to  $I^2R$  loss. Figure 14-10 shows the percent change of resistance as a function of power level for atmospheric and vacuum environments. In this test, 40 resistors were fired at 1400°F. Fifteen of these were placed in a vacuum of  $1 \times 10^{-8}$  millimeters of mercury for 168 hours with dissipations of 1.1 to 21.0 watts per square inch. The remainder were exposed to 1 atmosphere for 192 and 352 hours with dissipations of 9.3 to 166 watts per square inch.

Figures 14-7 through 14-10 all have one thing in common. They indicate that for a belt speed of 1 inch per minute, the optimum peak firing temperature is at or near 1400°F. The peak firing temperature was then specified at that value. To optimize belt speed, sample resistors were fired at 1/4, 1/2, 2, and 3 inches per minute. The previous data were used to obtain a point at 1 inch per minute. Figure 14-11 shows the variations in resistivity and temperature coefficient as a function of belt speed. With these data the optimum belt speed was determined to be 1 inch per minute.

It is felt that with the near optimization of peak firing temperature and belt speed, plus the design correction of the resistor blooming, a basic well-controlled screen circuit process had been established.

## MECHANICAL STRESSING

A series of mechanical stresses were placed on the resistor-substrate system to test its mechanical integrity. These stresses were designed to evaluate the match in temperature coefficient

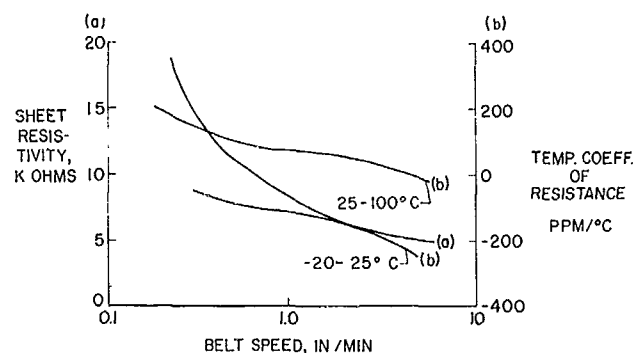


Figure 14-11—Evaluation of physical properties as a function of belt speed.

of expansion of the resistor and substrate, the capacity to take mechanical shock, and immunity to vibration. In this test, 12 substrates with the standard 5-resistor test pattern were fired at 1400°F. These resistors were divided into groups of 25, 15, and 20 resistors for thermal shock, mechanical shock, and vibration tests, respectively.

Thermal shock was achieved by soaking the resistors for 25 minutes in an oven set at 200°F and then dropping them into liquid nitrogen.

After soaking the resistors in nitrogen for 20 minutes, they were placed on a 200° F hot plate to dry the condensate. No deviation in resistance greater than instrumentation error (0.05 percent) was noticed. After 10 days, cracks were noticed in the substrate. Figure 14-12 is a photograph of these cracked substrates. Two very interesting facts can be seen in the photograph. First, the crack propagated through the points where the leads were connected to the substrate. Secondly, these points are on a straight line through points of maximum metallic mass and temperature coefficient mismatch.

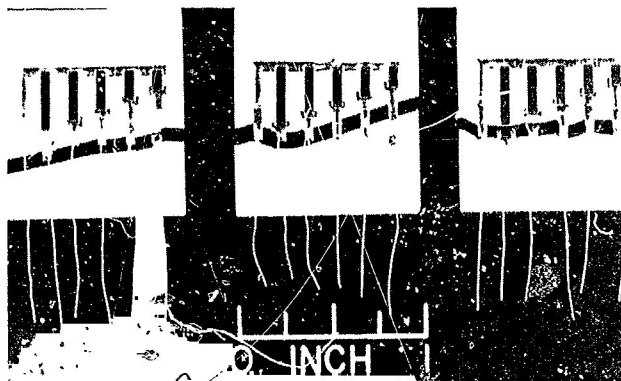


Figure 14-12—Substrate damage due to thermal shock.

Because of this failure, a new layout was made distributing the contact points. In addition, a more conservative application of solder was used. The test was then repeated in the hot-to-cold direction and vice versa without any failures.

Resistor substrates were mounted on three supporting points in a vibration test jig. All substrates were vibrated in the sinusoidal mode from 20 to 2000 cycles per second at a scan rate of 2 octaves per minute. Initial stress level was 10g along worst-case vibration axis. Resistance was recorded before and after each stress for nominal 10g step stressing up to 57g. No deviation in resistance greater than instrumentation error was noticed.

Three substrates with five resistors on each were shock tested to destruction. Resistance was measured before and after stress at 1.0, 2.1, 3.0, 4.4, 5.4, and 8.0 thousand g levels. Three substrates fractured, one each at the 2.1, 3.0, and 8.0 thousand g levels. All substrates fractured because of the 3-point support construction of the jig before any measurable resistance change occurred.

## CONCLUSIONS

It is reasonable to conclude that a screen deposition process has been established since, by definition, a fabrication process is established when the devices produced by the process have predictable parameters. In addition, the resistance value distribution indicates that the devices are reproducible within acceptable limits. It can be further concluded that the resistors fabricated have excellent environmental characteristics. Temperature coefficients of  $\pm 100$  parts per million have been established. In addition, drifts of less than 0.25 percent have been indicated over vacuum, temperature, power dissipations, humidity, and mechanical forcing functions.

Dimensional control is the most critical problem in the screen circuit process. There are two principal sources of error. First, error is introduced in the transfer of the stencil geometry

from the glass mask to the coated screen. Improvement in screen fabrication will be required before this source of error can be reduced. The second principal source of error is introduced by uncontrolled variables in the screen deposition process. These variables include squeegee speed, material quantity, viscosity, and squeegee wear. To improve deposition control, mechanization of the process will be required.

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N64 31577

## 15. A THICK-FILM, INSULATED GATE FIELD EFFECT TRANSISTOR

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The principal problem in film technology is the lack of active devices. As a result, the technology has relied on either discrete active components or relatively crude thin-film devices. A thick-film, insulated gate field effect transistor is being developed to utilize the simple processing technology of thick-film circuits. At the present state of development, significant characteristics have been obtained in thick-film transistors. Data showing high transconductance, high output impedance, and excellent stability characteristics are presented and processing technology discussed.

### INTRODUCTION

About 4 years ago, the microelectronic group at Langley Research Center decided that screened circuit technology could serve as an interim packaging process. The process, including the controlled fabrication of the complete passive network, is essentially complete; but at present fabrication of large value inductors is not practical. Figure 15-1 is a typical circuit using this technology. The circuit is an integrated device except that the active components (transistors) are bonded into the circuit. Screened circuit technology is, in this form, a hybrid system and has limitations when ultimate reliability is compared with that of a totally integrated system.

Langley Research Center, in an attempt to obtain the full potential of an integrated screened circuit technology, has initiated a preliminary effort to determine the feasibility of fabricating a thick-film active device. Portions of this work are being done on contract by RCA in conjunction with the continued screened circuit effort at Langley. This paper describes the results of initial experiments, indicates tentative conclusions based on these results, and outlines the current direction of this effort.

### PROBLEM DEFINITION

Materials deposited by screened circuit processing techniques are either fine grain or glassy structures. Therefore, consideration of minority carrier-type devices is eliminated because of the short carrier lifetimes in the screened material. For this reason, studies were initiated on

an insulated gate field effect device, which is a majority carrier device operable in materials of high dislocation densities. Table 15-1 provides a list of the work areas and associated problems involved in the successful fabrication of a thick-film insulated gate field effect transistor. Each of these work areas will be discussed in this paper.

#### CHANNEL LENGTH CONTROL

The basic problem associated with the screen deposition of the source-drain electrodes is the shorting of the channel when fabricating channel lengths of the order of 1 mil. This shorting occurs because of a basic tendency of the screen material to flow or bloom during the deposition. It has been determined (see Langley working paper LWP-190 for example) that the average amount of bloom was a constant of the process. It is, therefore, possible to allow for the bloom by designing a larger channel width.

A series of experiments determined that, under optimum conditions, blooming caused shortening of the channel length by 1.5 mils. Thus, to obtain a 1.5 mil channel length, a 3.0-mil length must be drafted into the artwork. To verify this, a second series of source-drain electrodes were processed using a 3.0-mil separation in the artwork. Figure 15-2 demonstrates the distribution of channel widths obtained in this experiment. As can be seen, the nominal value is just under 1.5

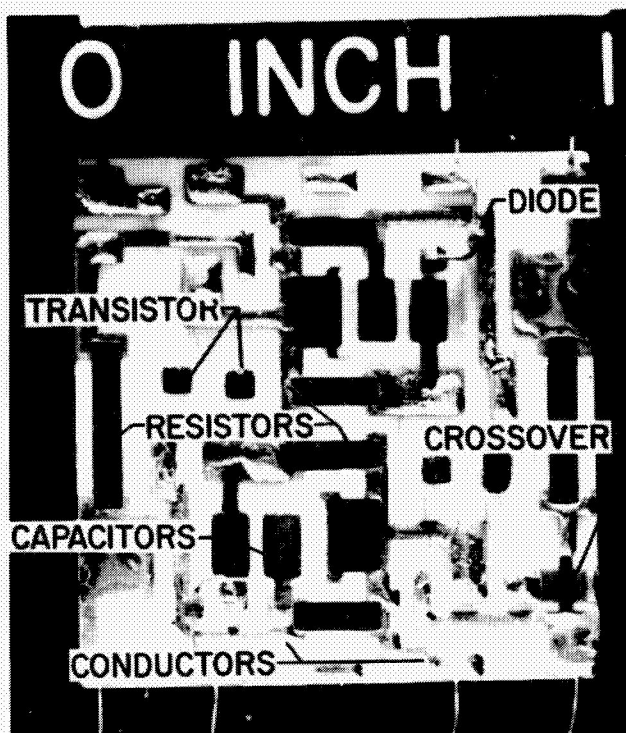


Figure 15-1—Typical screened circuit.

mils with  $\pm 0.3$  mil at the 10- and 90-percent points. These data suggest that channel lengths of less than a mil are practical.

WORK AREA	PROBLEM	EFFORT BY
CHANNEL LENGTH CONTROL	SOURCE DRAIN SHORTING	LRC
GATE REGISTRATION	HIGH ELECTRODE CAPACITANCE OR CHANNEL RESISTANCE	LRC
DIELECTRIC	SUFFICIENT ELECTRIC FLUX AT SEMICONDUCTOR SURFACE	LRC
SEMICONDUCTOR DEPOSITION	CONTROL OF PROCESS CHARACTERISTICS	RCA
SEMICONDUCTOR CHARACTERISTICS	CONTROL RESISTIVITY ACTIVATION ENERGY AND CARRIER TYPE	RCA
DEVICE CHARACTERISTICS	DEFINE DEVICE STABILITY	RCA

Table 15-1—Definition of Problems Associated with Fabrication of Thick-film Transistors.

#### GATE REGISTRATION

The basic problem in depositing the gate electrode is that the electrode must completely cover the channel. This is particularly true in enhancement devices since the area not covered would act as a high series impedance element in the source to drain circuit. If the approach to this problem is to make the gate sufficiently large to compensate for misregistration, the

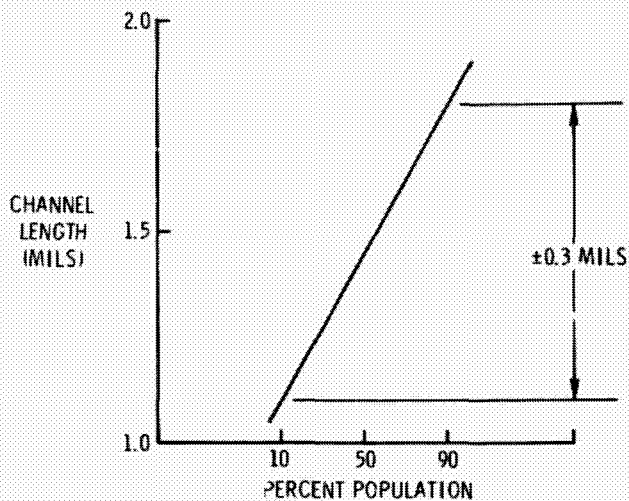


Figure 15-2—Distribution of screened channel lengths.

screened and used for the registration of the succeeding deposition. The variations in registration were measured using a reflected light optical comparator. Figure 15-3 shows the distribution of alinement of the gate over the channel. As can be noted, the registration was within  $\pm 1$  mil for the 10- and 90-percent points. With this information, it appears feasible to design gate electrodes with about a 1-mil overlap with the source and drain.

## DIELECTRIC MATERIAL

The most obvious problem associated with the fabrication of a screened insulated gate field effect transistor is establishing an electric flux sufficient to permit conduction at a reasonable gate turn-on voltage. If a surface state trapping density of  $2 \times 10^{12}$  states square per meter is assumed and a gate threshold of 4 volts desired, a silicon dioxide layer of  $10^3$  angstroms would be required. If, on the other hand, the thickness is limited to that of a screened process (about  $50 \times 10^3$  angstroms), a dielectric with an  $\epsilon$  of about 400 would be required. This presents two alternatives: first, existing screen processing can be used, and a dielectric material developed with a dielectric constant greater than 400 dielectric strength greater than  $10^8$  volts per meter, and no relaxation phenomena with rates greater than 0.5 microsecond; second, the method for depositing 1000-angstrom  $\text{SiO}_2$  films in a technique compatible with screened technology can be learned.

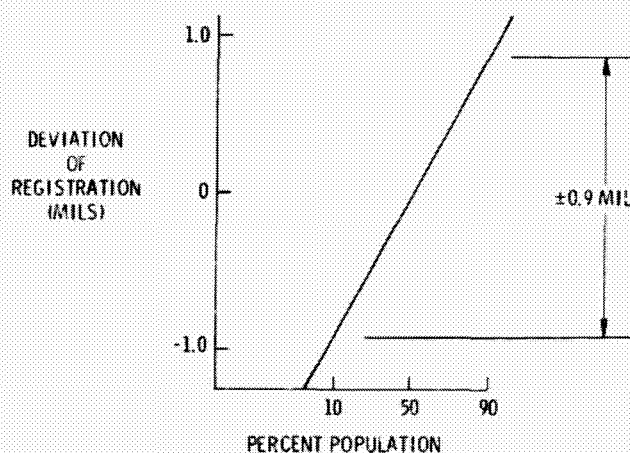


Figure 15-3—Distribution of deviations from registration of gate.

frequency response will be greatly reduced because of the interelectrode capacitance of the overlapping gate and drain, or gate and source electrodes. It is necessary to compromise between frequency response and impedance. The approach is to reduce misregistration to a tolerable limit and then compensate a minimum misregistration by making a larger gate.

An experiment was performed to determine the accuracy to which the gate could be registered over the channel. Registration points were placed in the artwork at approximately one-half inch from the transistor area. These marks and the transistor electrodes were



Experiments testing both approaches have been performed at Langley Research Center. A lead monosilicate glass was packed with barium titanate in colloidal suspension and used for the screened dielectric. Figure 15-4 shows the steps used to fabricate the transistor. First, the gate electrode was screened onto a substrate. Second, a 50,000-angstrom film of colloiddally suspended barium titanate was screened on the gate electrode. Third, the source-drain electrodes were screened on, and a chlorine dope CdS layer was screened. The resulting cross section is shown in Figure 15-5 with the appropriate dimensions. This structure was electrically tested, and control of the channel current was observed. On one device, a measurable gm of approximately 20 micromhos was noted. However, the estimated dielectric constant of the material was of the order of 80, indicating insufficient electric flux to overcome the surface trapping site density at any practical gate voltage.

A second experiment has been performed wherein the gate electrode was screen-deposited, and a 1000-angstrom film of  $\text{SiO}_2$  was pyrolytically deposited from a silane ( $\text{SiH}_4$ ) source. The application of  $\text{SiO}_2$  by this process is compatible with screened techniques; however, at the time of this writing, these units have not been tested electrically.

#### SCREENED SEMICONDUCTORS

A necessary portion of this program is the development of a screen technique for the deposition of thick semiconducting films with controlled impurity type and concentration. RCA has studied methods of depositing ZnS and PbS; to date PbS has been the most successful. PbS films on n and p carrier types have been screened. The resistivity has been

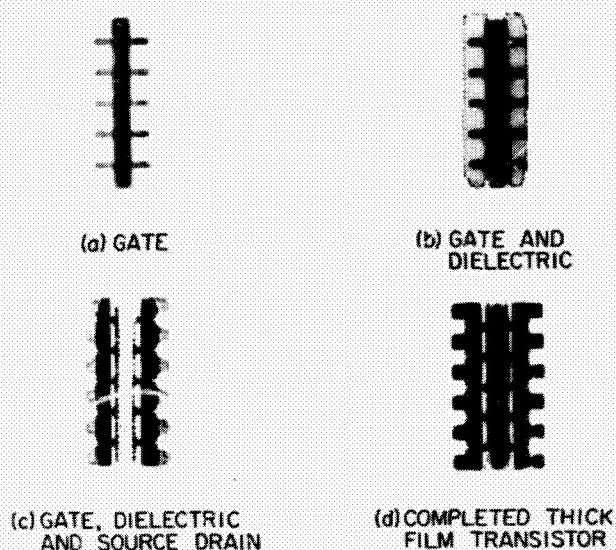


Figure 15-4—Steps in fabricating thick-film transistor.

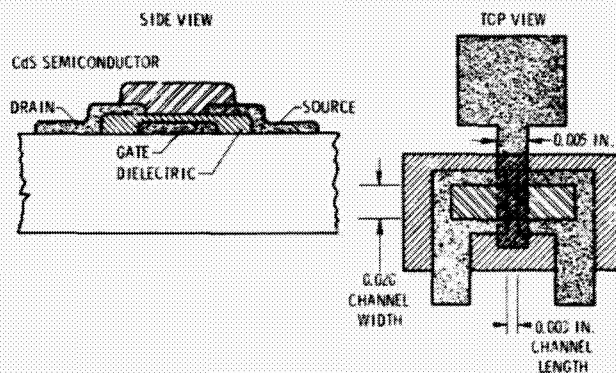


Figure 15-5—Langley thick-film transistor geometry.

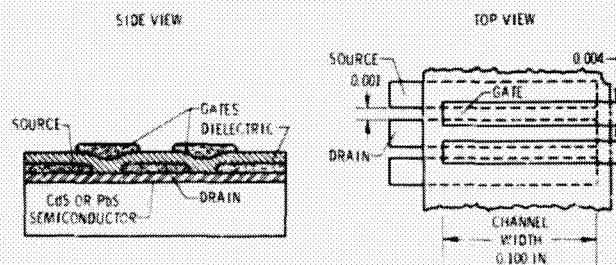


Figure 15-6—RCA thick-film transistor geometry.



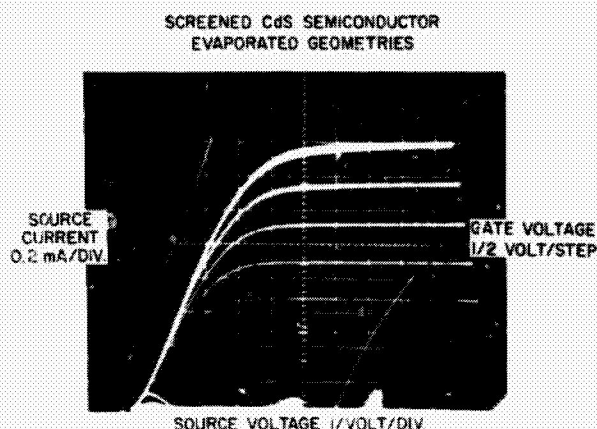


Figure 15-7—Source characteristics of RCA device No. 1.

fabricated by first screening a thick film of CdS. On top of the CdS film, the source and drain electrodes were evaporated, followed by a SiO<sub>2</sub> evaporation for the dielectric. The gate electrode was evaporated last. Figure 15-7 shows the source characteristics for the resulting device. These characteristics show several important features: the transconductance is of the order of 500 micromhos, and the leakage currents are quite low (less than 1 microampere).

A second device was fabricated using a sprayed thick-film semiconductor. The source characteristics of this device are shown in Figure 15-8. As can be seen, this device is quite similar to that shown in Figure 15-7.

To test the stability of these devices a 60,000-angstrom coating of SiO<sub>2</sub> was deposited over the transistor area, and six devices were placed in a constant current configuration with gate voltage of 2.0 volts and channel voltage at 4.0 volts. Over a period of several hours, only variations of a microamp or so could be observed.

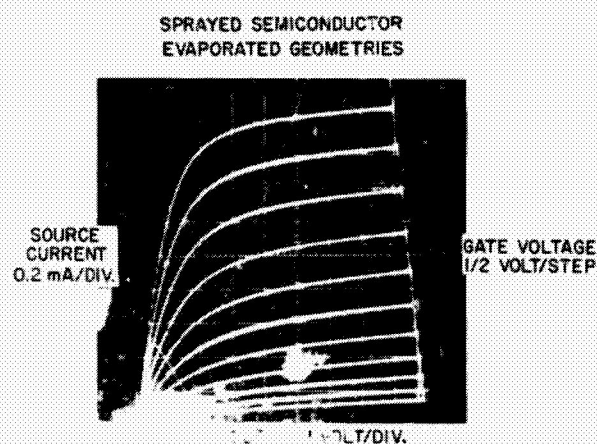


Figure 15-8—Source characteristics of RCA device No. 2.

controllable over the range of 1.0 to  $1 \times 10^4$  ohm-cm. P-type conduction has been obtained by the introduction of copper into the structure. N-type conduction has been obtained by substituting chlorine for sulfur. In both cases the activation energy has been of the order of 0.10 ev.

## DEVICE STUDIES

Figure 15-6 shows the thick-film transistor structure fabricated by RCA. As can be seen, the channel length is 1.0 mil. This device was

## CONCLUSIONS

The basic conclusion to be obtained from the data presented is that after an initial investigation, no basic limitations have been determined which make it impractical to fabricate a thick-film transistor. In addition, lateral geometries with sufficient controls for thick-film transistors have been demonstrated using screen deposition techniques. Basic problems exist in dielectric screening, but early results of pyrolytic deposition of SiO<sub>2</sub> appear to present a realistic alternate.

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N67-3-578

## 16. COMPATIBLE THIN-FILM TRANSISTORS

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Several approaches have been attempted to obtain thin-film transistors which are compatible with passive components. Results of recent efforts in developing the thin-film, field effect triode are described. Device geometry, as pertains to both performance and process limitations, is discussed from practical and theoretical standpoints.

### INTRODUCTION

Presently, satisfactory thin-film passive elements can be evaporated onto a substrate, but active elements are not entirely satisfactory. Many different approaches have been attempted toward fabricating a thin-film transistor. Figure 16-1 shows a thin-film, space charge limited triode which is similar to a vacuum tube. This type of thin-film triode has met with very little success. One of the principal difficulties is that the grid spacing must be less than a micron. Another configuration (Figure 16-2) is the tunnel emission triode, which is similar to the metal base transistor configuration which uses a semiconductor instead of a dielectric. This device has

difficulties because of pinholes and lack of film thickness.

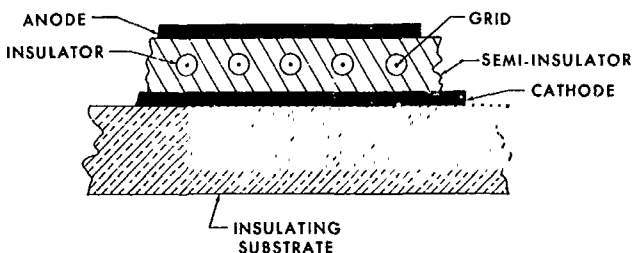


Figure 16-1—Space charge limited triode.

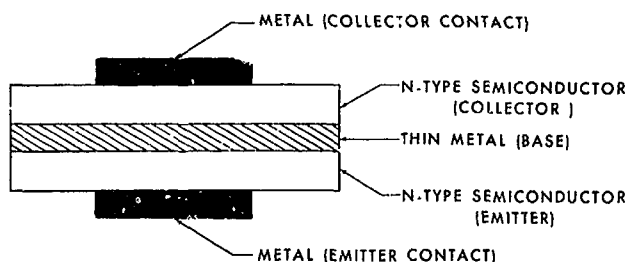


Figure 16-2—Structure of the metal base transistor.

There has been some success in the development of the metal base transistor. The current problems with the metal base transistor are that the metal base must be sufficiently thin and of the correct thickness to transmit electrons efficiently. Moreover, the semiconductor-to-metal barriers must be of the proper height or else inefficient transmission of current occurs. The insulated gate, thin-film, field effect transistor (FT) has been much more successful. This device is easier to construct and has been used to form successful devices (see Figures 16-3 through 16-5).

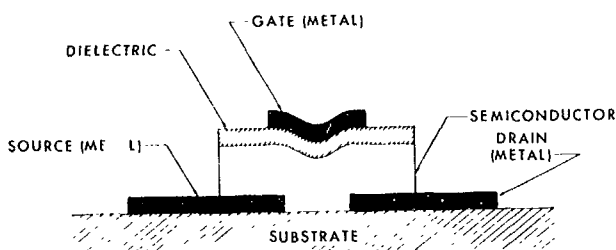


Figure 16-3—Insulated gate, thin-film, field effect transistor (TFT) structure, staggered configuration.

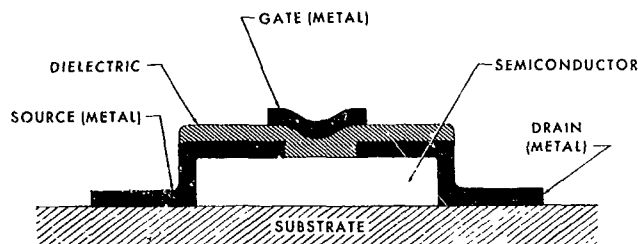


Figure 16-4—Insulated gate, thin-film, field effect transistor (TFT) structure, coplanar configuration.

## FABRICATION

Of the three configurations for insulated gate, field effect transistors, the staggered configuration (Figure 16-3) lends itself most easily to form a thin-film transistor (TFT) (Reference 1). Hence, this paper will be primarily concerned with this configuration. The difficulties with the staggered configuration are (1) making a very narrow source-drain spacing, (2) placing a gate the width of the source-drain spacing over the source-drain spacing, and (3) oxidation of the electrodes when the substrate or semiconductor is heat-treated. The gate should be as narrow as the source-drain spacing to avoid extra capacitance introduced by the gate overlapping the source or drain electrode, which reduces the frequency response. The coplanar configuration (Figure 16-4) has the advantage of having the semiconductor already on the substrate before the electrodes are deposited. In this manner, the semiconductor can be heat-treated without oxidation of the electrodes. The planar configuration (Figure 16-5) allows the electrodes to be formed by photographic etching techniques if the dimensions are not too small. The source, drain, and gate are the parts with critical dimensions and can be formed accurately by photographic etching.

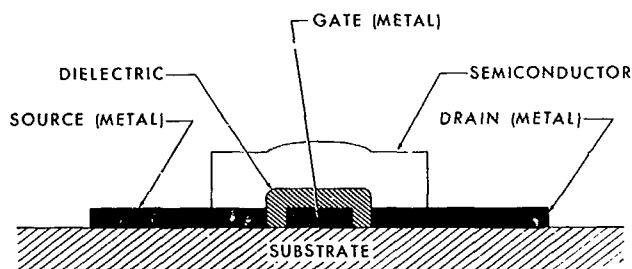


Figure 16-5—Insulated gate, thin film, field effect transistor, planar configuration.

These devices are produced by evaporating the components onto glass substrates (Figure 16-6; see also Reference 2). Various glass substrate materials have been used, such as Corning microscope slides and Corning 0211, 7059, and 7052 glass substrates. While a high quality glass should be used, no particular glass gives significantly better results. Likewise, many complicated substrate cleaning methods have been used, but it has not been definitely shown that they give superior results. To be sure, the substrate must be cleaned well and protected from dust before it is used. One sample process consists of washing the substrate with water and an abrasive such as MgO. Then the substrate is rinsed with deionized (DI) water and then with acetone. This rinse is followed by washing in DI water and rubbing the substrate with "Joy" detergent. The substrate is again rinsed with DI water and placed in a detergent at 140° F. in an ultrasonic cleaner for 10 minutes. The substrate is removed and rinsed with DI water and then dried with dry nitrogen gas. The substrate is then placed in a petri dish or used immediately.

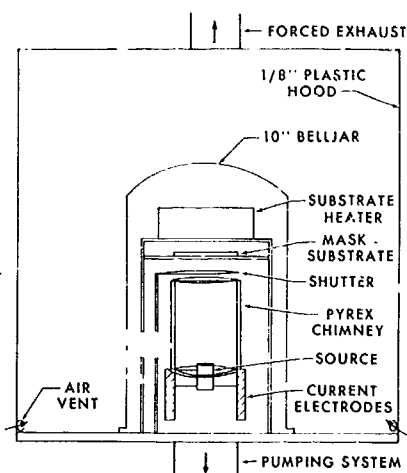
ENCLOSURE  
AND SYSTEM  
SETUP FOR Te  
EVAPORATIONS

Figure 16-6—Enclosure and system setup for Te evaporation.

The substrate is generally outgassed in a vacuum by heating the substrate at 400° C. for 5 minutes before depositing the source-drain electrodes. When the substrate cools to approximately 200° C., the source-drain electrodes of nichrome are deposited. The source-drain electrodes are generally nichrome since nichrome is more resistant to oxidizing and scratching than aluminum. The disadvantage of nichrome is that the substrate temperature must be approximately 200° C. to prevent peeling off the substrate.

The semiconductors used are CdS, CdSe, CdTe, and Te of very high purity (99.999 to 99.9999 percent). The semiconductor is evapo-

rated from a container called a boat. Care must be exercised in selecting the boat material to avoid contaminating the semiconductor. For CdS, CdSe, and CdTe, SiO<sub>2</sub> crucibles and molybdenum boats have been used successfully. Graphite and platinum boats have given poor results with Te, but molybdenum boats are satisfactory. The boat is electrically heated to 750° C. to 850° C. for CdS. When a semiconductor or dielectric evaporates, there is a tendency for particles to be splattered onto the substrate. To prevent this, quartz fiber or quartz paper is placed over the evaporating substance. Evaporation rates will vary from 10 to 100 Å/sec, and thickness will vary from 1000 to 10,000 Å. The boat and substrate must be at the correct temperatures for the film to form satisfactorily on the substrate.

The boat must be hot enough to evaporate the material at a satisfactory rate, but not hot enough to cause it to dissociate. To increase the evaporation rate, boats are made larger. The heat from the boat can cause the substrate temperature to rise. Therefore, the substrate must be kept at a proper temperature so that the material will adhere to the substrate. If dissociation takes place, it will affect the stoichiometry and the condensation rate of the semiconductor. Following the deposition of the semiconductor, the semiconductor is annealed. That is, the temperature of the substrate is raised for about two minutes, and then the substrate is allowed to cool. There are several approaches that can be used in annealing the substrate: (1) after annealing, the dielectric can be deposited, (2) the semiconductor can be exposed to air after cooling, and (3) the semiconductor can be re-annealed in air before depositing the dielectric. The annealing operation is essential to producing good devices. The exact process or change produced in the semiconductor or semiconductor dielectric interface has not been determined.

After the annealing step, a dielectric is deposited on the semiconductor. Dielectrics which are oxides are believed to give the best results. The dielectric most frequently used is SiO. The oxygen atoms of SiO are assumed to absorb oxygen on the surface of the semiconductor. For the

final process, an aluminum gate is deposited over the source-drain spacing. Aluminum is used instead of nichrome because aluminum can be deposited on a substrate at room temperature.

The source-drain resistance is a critical property of the TFT during fabrication. When source-drain spacings less than 1 mil are formed, the problem of depositing electrodes arises (Figure 16-7). While the material may be transparent under a microscope or Nikon Shadow graph, the resistance across the source-drain spacing can be very low (e.g., 100 ohms), whereas it should be above 100 megohms. After the semiconductor is deposited, the resistance should be high (e.g., 1 megohm). After depositing the dielectric, the resistance should drop from one to three orders of magnitude. If this resistance drop does not occur, poor devices are almost certain to result.

In order to achieve high frequency response, the source-drain space is made as narrow as possible. For a gain-bandwidth product of 300 mc, the spacing should be 0.1 mil for a semiconductor such as CdSe. This spacing is based on the theory of Weimer and Borkan. From this theory, the frequency response is proportional to the carrier mobility and inversely proportional to the square of the source-drain spacing. There are several difficulties in forming such a narrow spacing. When photographic and etching techniques are used, the source-drain spacing has ragged edges. Chemically etching 0.1-mil widths in metal foil masks was not successful because of metal grain boundaries. Also, electroforming of nickel masks results in difficulties with irregularities in base metals. The electrodes of these masks also have ragged edges. The solution to this problem is to use a fine tungsten wire (see Reference 3). The wire used is 0.1-mil tungsten wire. Tungsten wire is stretched on a molybdenum mask (Figure 16-8). The tungsten wire is very elastic and has a lower coefficient of expansion than molybdenum. Hence, heating the mask before depositing nichrome causes additional tension in the wire. The gate theoretically must be the same width as the source-drain spacing and must be precisely above the spacing. Overlapping of the gate and source-drain electrodes increases capacitance and lowers the frequency response. To form very narrow gates, two 1-mil wires were used spaced 0.1 mil apart (Figure 16-9).

Thin-film field effect transistors have been formed from many different semiconductors. A partial list includes CdSe, Te, CdS, CdTe, PbTe,  $\text{Ag}_2\text{Te}_3$ , AgTe,  $\text{Bi}_2\text{Se}_3$ , MnTe, and SnS. With the exception of the first three, the foregoing compounds display a weak field effect, and unsatisfactory TFT devices have been constructed.

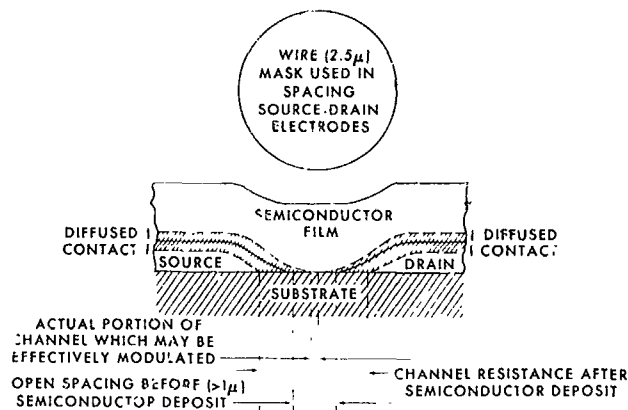


Figure 16-7—Electrode deposition in TFT formation.

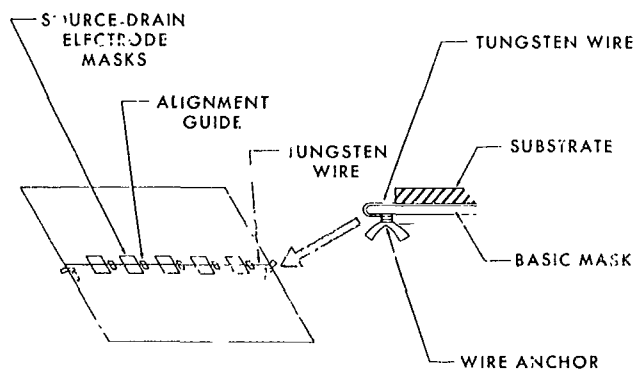


Figure 16-8—Basic source-drain mask.

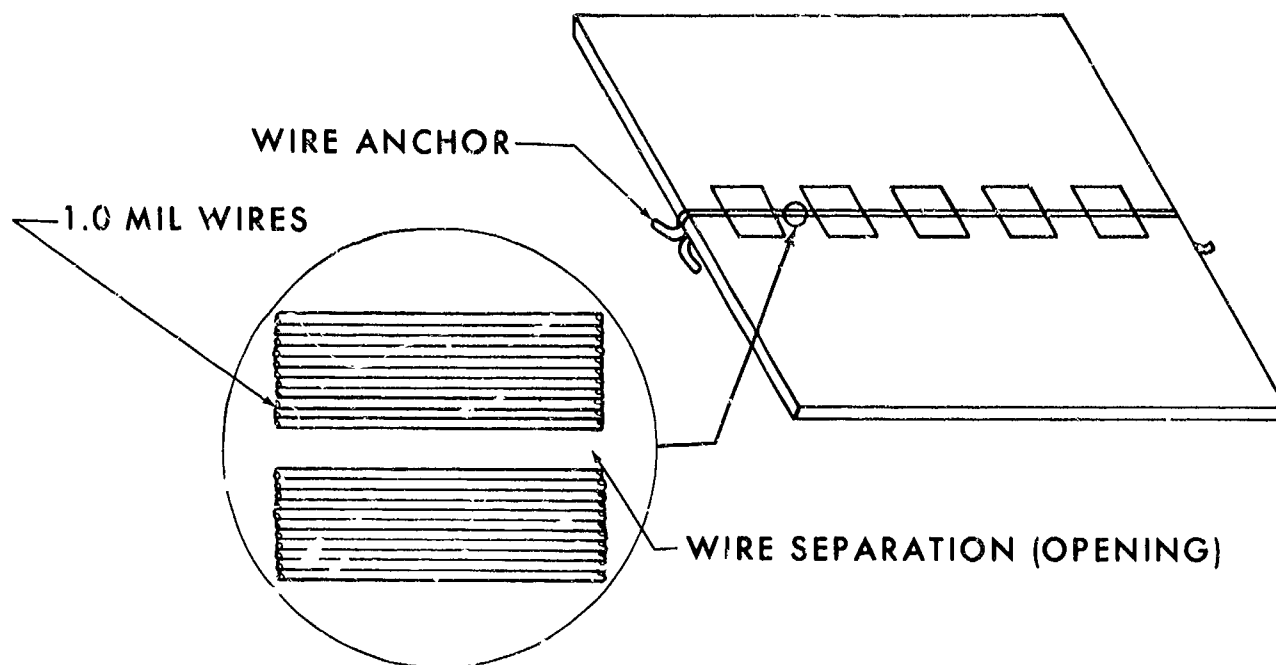


Figure 16-9—Gate electrode masking method.

The best semiconductors are CdSe, Te, and CdS, which can be made to display pentode-like characteristics. CdSe is probably superior to the other Cd compounds because it is less likely to dissociate during evaporation, and, of course, Te does not dissociate.

Contract NAS 9-3924 with Melpar, Incorporated resulted in TFT's which had a gain-bandwidth product of 33 mc for Te and CdSe devices. Theoretically, the response should have been greater than 80 mc. These devices had a gate width of 0.2 mil and an input capacitance of 10 pf. The yield reached 95 percent.

#### CURRENT PROBLEMS WITH FET'S

One of the current problems with FET's is that of reproducing their characteristics. Although investigators agree that good characteristics can be obtained for a specific device, there is little discussion concerning variation of characteristics of different devices on a substrate and variation from deposition to deposition. Also, while some devices have functioned for prolonged periods of time, the longevity of the devices is not very well established at present. Furthermore, there are other problems to be solved before completely satisfactory devices are developed. For example, devices often exhibit hysteresis loops (Figure 16-10). These hysteresis loops may disappear upon placing the devices in a vacuum, although good devices do not display these characteristics. There have been many reasons hypothesized for the hysteresis curves. These include (1) internal heating, (2) stray capacitance, (3) humidity, and (4) the existence of a nonhomogeneous, stratified insulator layer. No experimental evidence has explained the mechanism causing the hysteresis loops.

Another characteristic is a slow drift of characteristic curves with applied voltage and time (see Reference 4). Changing the applied grid voltage causes the characteristic curves to slowly drift. The devices are also sensitive to light although this effect can be remedied by encapsulation. These devices are affected by temperature changes; for example, the drain current often increases with temperature. One demonstration has shown that the devices which have hysteresis loops lose them with increasing temperature, and then regain them.

#### STATE OF THE ART IN TFT DEVICES

Weimer's group at RCA has constructed several devices which employ closely spaced TFT's. This group has recently fabricated a 180-stage Integrated Thin-Film Scan Generator (see Reference 5) composed of 180 field effect diodes, 360 thin-film transistors, 360 resistors, and 180 capacitors on a glass substrate. All the components must function in order for the device to operate, and RCA claims that the device can be reproduced under laboratory conditions. The device functions from 12 kc to 2 mc, and some devices have operated at 85° C. for 5000 hours. This device was fabricated using a wire grill with 480 wires per inch (Figures 16-11 and 16-12). The individual stages are spaced 2.08 mils apart. The device is fabricated during one pump-down of the vacuum system, during which time 20 to 30 individual evaporations are carried out.

#### CONCLUSION

Satisfactory thin-film, passive devices have been fabricated with reliable and predictable characteristics; however, field effect thin-film transistors (FETFT) are still in the laboratory stage of development. For frequencies below 2 mc, devices have been fabricated with field effect thin-film transistors which are compatible with passive components. For frequencies above 2 mc, the gain-bandwidth product has been extended to 33 mc with transconductances of more than 25,000 mhos. The source-drain spacing is probably made as small as possible with the wire-mask technique. Further reduction in the source-drain spacing may be accomplished with improved photographic and etching techniques. Further improvement in the performance and reproducibility of FETFT characteristics will probably require a better understanding of the interaction of the dielectric-semiconductor interface and the conduction mechanism in the semiconductor.

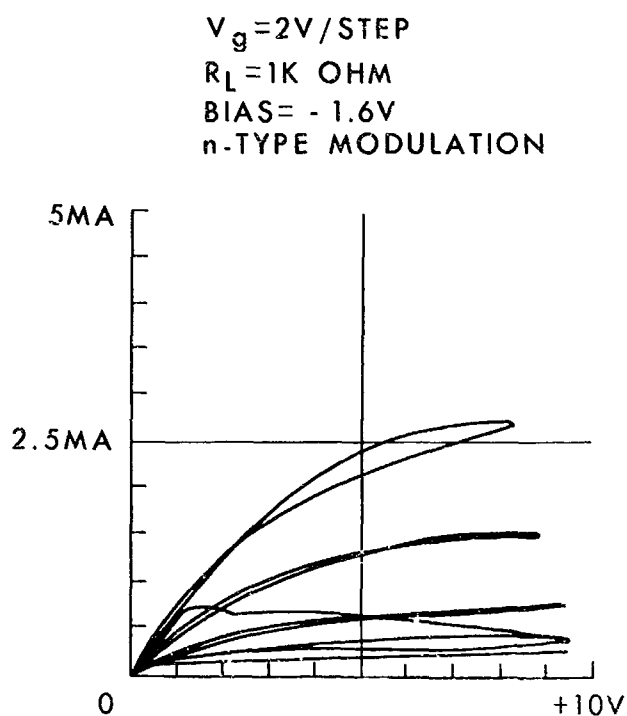


Figure 16-10—Output characteristics of CdTe doped with indium TFT.



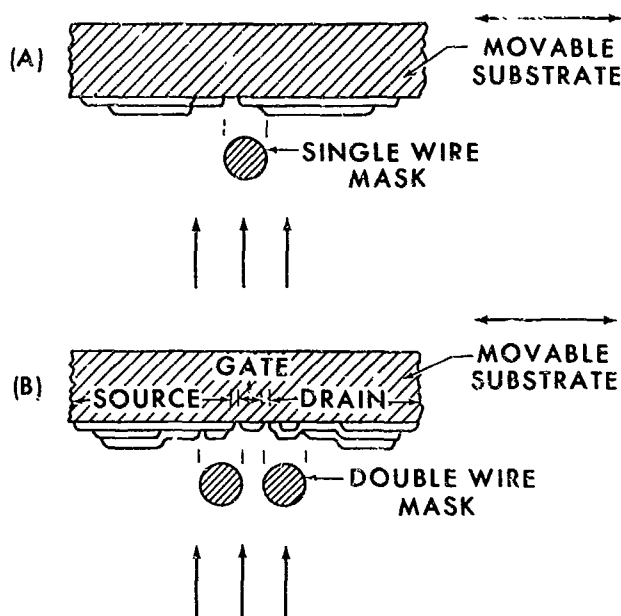


Figure 16-11—Use of single and double masks to form evaporated patterns having spacings much less than the wire diameter.

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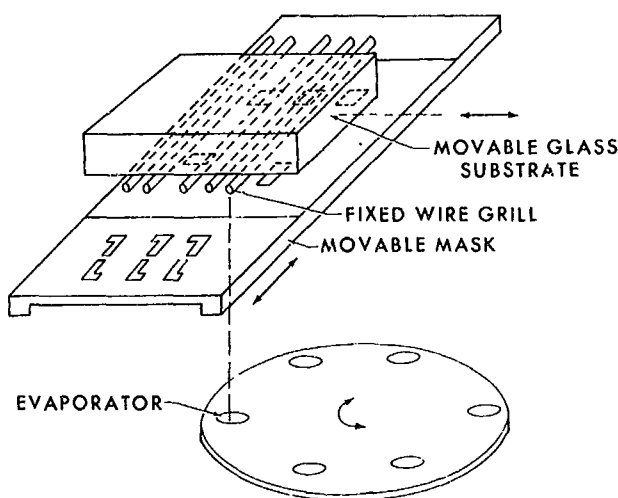


Figure 16-12—Grill and aperture plate masking technique.

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## APPENDIX

The following derivation follows that given by Borkan and Weimer (References 1 and 6).

The geometry of the TFT is given by Figure 16-13. The following assumptions are made.

1. The mobility of the carriers is independent of gate voltage.
2. The gate capacitance is constant and independent of gate voltage. The gate voltage induces a charge per unit area of

$$q\Delta N(x) = \frac{C_g}{wL} [V_g - V(x)], \quad (1)$$

where

$q$  = electronic charge,

$\Delta N(x)$  = induced number of electrons,

$C_g$  = capacitance across insulator,

$L$  = source-drain spacing,

$Z$  = width of source-drain spacing,

$a$  = thickness of semiconductor,

$V_g$  = gate potential,

$V(x)$  = potential in semiconductor at point  $x$ ,

and

$I_d$  = drain current.

The drain current is given by

$$I_d = a Z \mu_d q \left[ \frac{N_o}{aLZ} + \frac{\Delta N(x)}{a} \right] E_x, \quad (2)$$

$\mu_d$  = drift mobility (cm /volt-sec),

$E_x$  = electric field from source to drain (volt/cm),

and

$N_o$  = total number of charges originally in gap region.

Substituting Equation 1 into Equation 2,

$$I_d = \frac{\mu_d C_g}{L} \left[ q \frac{N_o}{C_g} + C_g - V(x) \right] \frac{dV(x)}{dx} \quad (3)$$

Since  $E_x = \frac{dV(x)}{dx}$ , integrating Equation 3 over  $(x)$ ,

$$I_d \int_0^L dx = \frac{\mu C_g}{L} \int_0^V \left[ \frac{qN_o}{C_g} + V_q - V(x) \right] dV(x), \quad (4)$$

$$I_d = \frac{\mu C_g}{L^2} \left\{ \left[ \frac{qN_o}{C_g} - V_q \right] V_d - \frac{V_d^2}{2} \right\} \quad (5)$$

Let  $V_o = \frac{qN_o}{C_g}$ , then

$$I_d = \frac{\mu C_g}{L^2} \left[ (V_g - V_o) V_d - \frac{V_d^2}{2} \right]. \quad (6)$$

Equation 6 is valid over the range  $0 \leq V_d \leq V_g - V_o$  or to the knee of the  $I_d$  vs.  $V_d$  curve, where  $\frac{\partial I_d}{\partial V_d} = 0$ . From Shockley's unipolar field effect transistor, the curve is assumed to be constant beyond the knee of the curve.

The transconductance below the knee is given by

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{\mu_d C_g V_d}{L^2}. \quad (7)$$

The gain-bandwidth product is given by

$$G \cdot B_w \approx \frac{g_m}{2\pi C_g}. \quad (8)$$

Using Equation 8,

$$G \cdot B_w \approx \frac{\mu V_d}{2\pi L^2}. \quad (9)$$

At the knee of the curve,  $V_d = V_g - V_o$ ,

$$I_{d(max)} = \frac{\mu_d C_g}{2L^2} (V_g - V_o)^2, \quad (10)$$

and

$$g_m = \frac{\mu_d C_g (V_g - V_o)}{L^2} \quad (11)$$

Hence

$$G \cdot B_w \approx \frac{\mu_d (V_g - V_o)}{2\pi L^2} \quad (12)$$

at or above the knee.

The following derivation of the thin-film triode in the depletion mode follows that of Wilson and Gutierrez (Reference 7). This derivation assumes that (1) the mobility remains constant with field, (2) charge distribution is uniform, (3) the capacitance and voltage across the dielectric are given by  $C_1$  and  $V_1$ , respectively, and (4) the capacitance and voltage across the semiconductor are given by  $C_2$  and  $V_2$  respectively. The impurities in the semiconductor are assumed to be ionized, and the potential across the depletion layer is calculated from Poisson's equation

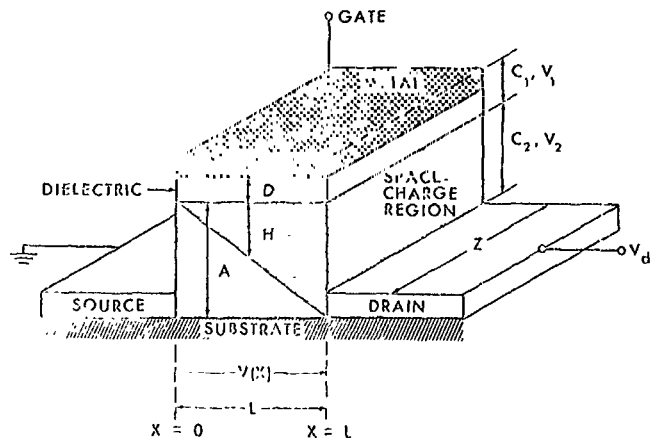


Figure 16-13—Geometrical Model of Operating TFT.

$$\nabla^2 V_2 = - \frac{\rho}{\epsilon_0 k_2} . \quad (13)$$

$$V_2 = \frac{qNh^2}{2k\epsilon_0} , \quad (14)$$

where

$N$  = impurity density,

$q$  = electronic charge,

$k$  = dielectric constant,

and

$\epsilon_0$  = permittivity of free space.

Hence the relationship between the potential in the depletion layer in the semiconductor and the channel voltage is calculated. The potential in the channel is given by

$$V(x) = V_1 + V_2, \quad (15)$$

where  $V_1$  is the potential across the dielectric.

The dielectric and depletion layers are considered as capacitors in series. The voltage  $V_2$  may be written as

$$V_2 = \frac{C_1}{C_1 + C_2} V(x), \quad (16)$$

where

$$C_1 = \int_0^L \frac{k_1 \epsilon_0 Z}{d} dx = k_1 \epsilon_0 Z \frac{L}{d} , \quad (17)$$

and

$$C_2 = \int_0^L \frac{k_2 \epsilon_0 Z}{h} dx = \frac{k_2 \epsilon_0 ZL}{h} ; \quad (18)$$

then

$$V_2 = \left[ \frac{k_1 h}{h k_1 + d k_2} \right] V(x). \quad (19)$$

Using Equations 19 and 14,

$$V(x) = \frac{qN}{2k_2 k_1 \epsilon_0} \left[ k_1 h^2 + d h k_2 \right]. \quad (20)$$

Let

$$\beta = \frac{2k_2 k_1 \epsilon_0}{qN} \quad (21)$$

Rearrange Equation 7 so that

$$h^2 + \left(\frac{k_2 d}{k_1}\right)h + \left(\frac{-\beta}{k_1}\right)V(x) = 0, \quad (22)$$

$$b = \frac{k_2 d}{k_1} \quad (23)$$

$$c = \frac{-\beta}{k_1}. \quad (24)$$

Then

$$h = \frac{-b + [b^2 + 4cV(x)]^{1/2}}{2}, \quad (25)$$

where the negative root is not a desired solution.

When the depletion layer extends across the channel, pinch-off is said to occur. The pinch-off voltage occurs at

$$V_p = \frac{a(a+b)}{c}. \quad (26)$$

From Ohm's Law,

$$J(x) = \sigma E(x) = \sigma \frac{dV}{dx}. \quad (27)$$

In terms of the depletion layer thickness,

$$J(x) = \frac{I}{Z(a-h)}. \quad (28)$$

Inserting Equation 15 into Equation 14 gives

$$\frac{dV}{dx} = \frac{I}{\sigma(a-h)Z}. \quad (29)$$

Substituting Equations 25 and 26 into Equation 29 gives

$$\left\{ (b^2 + 4cV_p)^{1/2} - [b^2 + 4cV(x)]^{1/2} \right\} \frac{dV}{dx} = \frac{2I}{\sigma Z}, \quad (30)$$

$$6CV(x)(b^2 + 4CV_\rho)^{1/2} - [b^2 + 4CV(x)]^{3/2} = \frac{12CI_x}{\sigma Z} - b^3. \quad (31)$$

Putting Equation 31 in terms of the voltage across the drain gives

$$I = \frac{\sigma Z(2a + b)}{12CL} \left\{ 6CV + \frac{b^3}{(2a + b)} - \left[ \frac{b^2 + 4CV}{b^2 + 4CV_\rho} \right]^{1/2} (b^2 + 4CV) \right\}. \quad (32)$$

Pinch-off current  $I_p$  is given by

$$I_p = \frac{\sigma Z(2a + b)}{12CL} \left\{ 2CV_\rho + \frac{b^3}{(2a + b)} - b^3 \right\}.$$

The preceding derivation gives a good correlation with experiment.

An alternate theory has been proposed by Abraham and Poehler to account for the conduction mechanism in thin-film transistors (References 8 and 9). This theory proposes that the electrons are field-excited from shallow levels lying below the conduction band. The transition probability for these electrons and the associated drain current correlates very well with the gate voltage (Figure 16-14). An expression is stated for drain current as

$$I_d = Z\mu e \left[ N_o + n_1 \exp \left( - \frac{8\pi}{3} \frac{\sqrt{2m^*}}{h e} \frac{k}{V_g} (V_1)^{3/2} \right) \right] f(V_D)$$

where

$n_1$  = density of states at 1st level below conduction band,

$n_0$  = local density of free majority carriers,

$V_1$  = ionization potential of 1st level,

$f(V_D) = V_D$  if  $I_D$  does not saturate,

$V_g = KE$ ,

and

$E$  = excitation field.

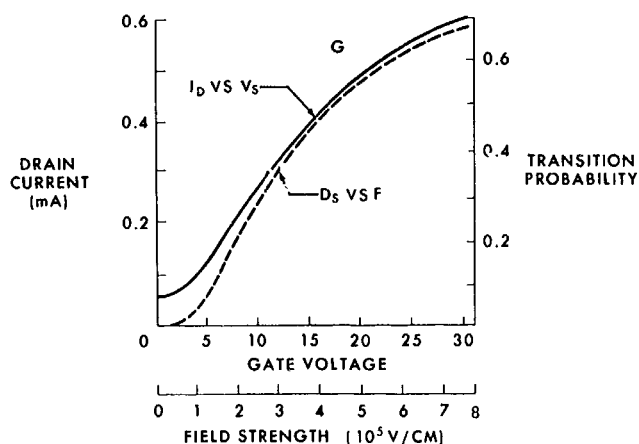


Figure 16-14—Drain-current-gate-voltage characteristic and the probability of field excitation of carriers.

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## 17. OPTICAL MEMORY WITH FERRIMAGNETIC STORAGE ELEMENTS

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This report summarizes a 15-month effort to fabricate a magneto-optic memory. The scope of work included efforts to produce a material that would operate without compensation at room temperature. The material was evaluated to determine its magnetic, optical, and thermal properties such that the design of the memory might be optimized. To demonstrate the results of the experimentation a feasibility model was designed and fabricated. The storage element chosen was gadolinium iron garnet doped with aluminum. Information is written into the memory by simultaneously applying heat and a magnetic field to a spot. Since the coercivity of the material is temperature dependent, only the heated portion of the garnet is affected by the field. The readout signal is derived from the Faraday rotation of a polarized beam of light by the element. The state of magnetization of a region is determined by observing the direction of Faraday rotation.

### INTRODUCTION

It is generally recognized that for large random-access systems (greater than  $10^6$  words) the most debilitating influence on the system comes not from the memory element, but from the peripheral interconnections and equipment. In these large systems, one is confronted with the reliability numbers game. One technique to eliminate the large numbers of access interconnections is the use of optics. With proper techniques, a beam of light may be steered randomly to any point within a memory matrix. This eliminates the large logic decoding trees and the attendant drive lines. Optical access memories using the Kerr effect have been devised, but the writing functions must still be line driven. Memories utilizing holographic and photochromic devices have been proposed; however, they have not progressed much beyond the conceptual stage of development. On the other hand, the ferrimagnetic memory is both written and read optically; thus, it has greater potential for mass memory application.

## COMPENSATION POINT MEMORY

The storage element used is a gadolinium iron garnet, which exhibits the necessary ferrimagnetic properties; that is, the magnetic moments of gadolinium and iron align in opposition, and the magnitude of the moments is temperature-dependent. The resulting magnetic moment of the element is the difference between these two sublattice moments. At a particular temperature the magnetic moments of gadolinium and iron are equal and opposite, thereby canceling each other. This temperature is called the compensation temperature or compensation point. At the compensation point there is no net magnetic moment; therefore, the element is unaffected by external magnetic fields. Since the magnetic moments of gadolinium and iron cancel exactly, no further reduction in energy would be accomplished by the application of a field. This point is illustrated by Figure 17-1. The memory described here operates around this compensation point.

The construction of the compensation-point memory is shown in Figure 17-2. The memory element is a thin slab of ferrimagnetic material which is held at its compensation temperature.

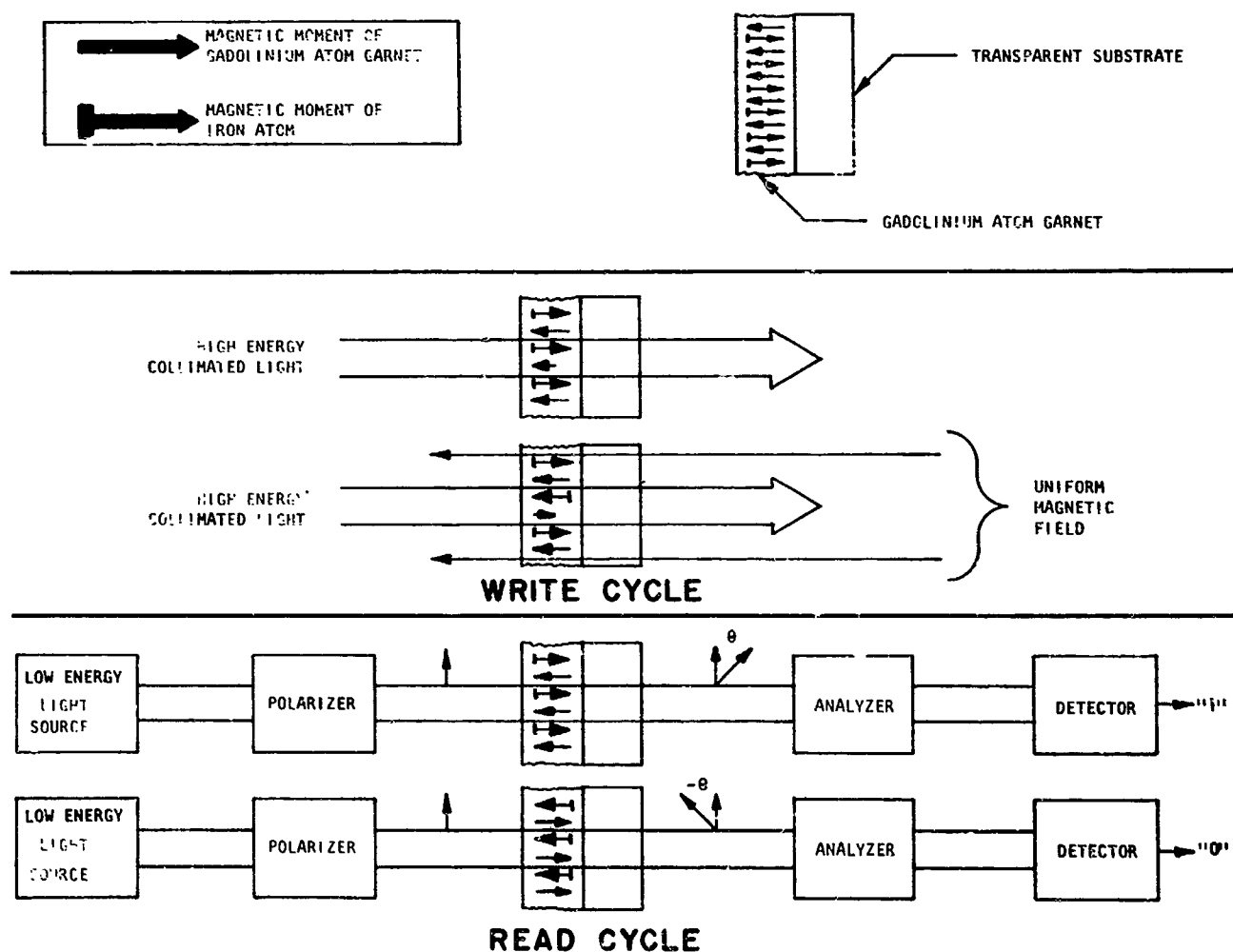


Figure 17-1—Read and write cycles, block diagram.



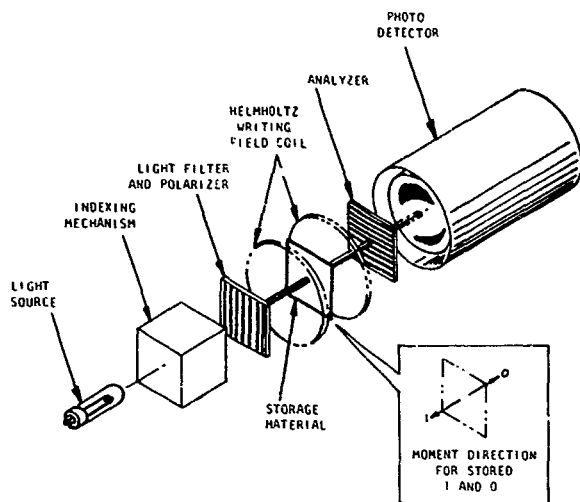


Figure 17-2—Compensation-point memory construction.

The magnetic easy axis is normal to the slab. Writing is accomplished by heating a local area to reduce the coercivity and then applying a magnetic write field to set the memory. The write field is applied by a single Helmholtz coil. The magnitude of the field is much lower than the coercivity at the compensation temperature, but is greater than the coercivity in the heated area. Consequently, only the magnetic moment in the heated area is oriented in the direction of the applied field. Reading is accomplished by applying a beam of polarized light to the spot to be read. The transmitted light is passed through an analyzer and detected by a phototube. Because of the Faraday effect,

the plane of polarization of the incident light is rotated as it passes through the magnetic medium. The rotation of the plane of polarization is clockwise or counterclockwise, depending upon whether the magnetization is parallel or non-parallel to the beam of light. One direction is defined as binary one, the other as binary zero. Consequently, a stored 1 can be distinguished from a stored zero by observing the amplitude of the transmitted light. The readout is obviously nondestructive.

The write-cycle time depends on the thermal relaxation time of the memory element, the temperature change required to take the element from a non-disturb to write state, and the magnitude of the write field. The variation of coercivity with temperature about a compensation point is shown in Figure 17-3. To write into the memory, the temperature of the selected bit must be raised to at least  $T_r$ , such that a write field of  $H_w$  may operate on the spot, and then reduced to  $T_c + T_a$  before the write field can be removed. Thus, the write cycle consists of selecting a spot, raising, and then lowering its temperature in the presence of a field. The cycle time depends upon how fast these operations can be performed. The writing time can be reduced by increasing the power of the heating pulse. The time required to lower the temperature will depend upon the thermal relaxation time constant of the material.

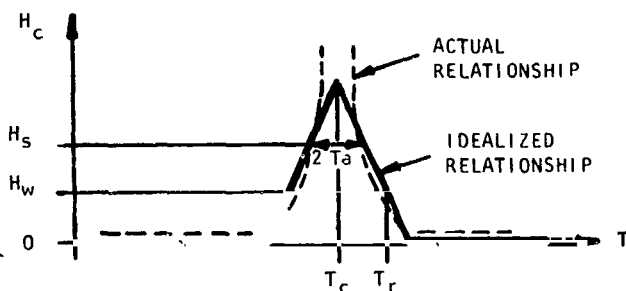


Figure 17-3—Idealized plot of coercivity versus temperature variation.

The material required for a fast-write-cycle memory should have an  $H_c$  versus  $T$  relationship with the general shape of that shown in Figure 17-3. The effective sheet coercivity,  $H_s$ , should be as high as possible for the specified variation in ambient temperature,  $T_c$ , and the slope of the curve should be as steep as possible. The material should have a large thermal conduction coefficient; or, preferably, it should be prepared on a transparent substrate

with a large thermal conduction and large specific heat. Since the element is heated by a beam of light, the storage element should be sufficiently opaque to absorb energy and sufficiently transparent to be heated internally.

The read operation is based on the use of polarized light and the Faraday effect. A large rotation of the plane of polarization of the read light beam is desired because this improves the discrimination between 1 and 0 outputs and relieves the requirements on the analyzer. Since the magnitude of the rotation is proportional to the thickness of the elements, thick elements are seemingly preferable. However, absorption of the light implies that thin samples are desirable. A figure of merit is the ratio of the rotation power to the absorption coefficient. Thickness considerations impose practical limitations on the choices for light sources and detectors. The read-cycle time is determined primarily by the indexing time and the detector speed. Since no switching is involved in the read operation, the time delay in the storage medium is negligible.

#### ELEMENT PREPARATION

Three primary methods of preparing the gadolinium iron garnet were investigated: thin films, polycrystalline samples, and single crystals. The results of the thin films were disappointing. Polycrystalline materials were obtained and found to be quite comparable in optical absorption and Faraday rotation to the single-crystal material. However, polycrystalline samples could not be made as thin as the single-crystal material, and the polycrystalline material did not exhibit magnetic anisotropy. Therefore, the direction perpendicular to the plane of the element could not be made into an easy direction. Single-crystal material was prepared by the molten-flux method.

#### TEMPERATURE COMPENSATION

In the gadolinium iron garnet,  $\text{Gd}_3\text{Fe}_5\text{O}_{12}$ , the iron ions occupy two different sites. Three of the atoms in the unit cell occupy tetrahedral sites, and the other two occupy octahedral sites. The iron atoms in the octahedral and tetrahedral sites are coupled antiferromagnetically. The resultant magnetization of the iron atoms is coincident with the iron atoms in the tetrahedral sites.

The gadolinium ions are coupled antiferromagnetically to the net moment of the iron ions. The coupling of the gadolinium ions is much weaker than that between the iron ions. As a consequence, the magnetization of the gadolinium ions drops very quickly with increasing temperature, approximately as  $1/T$ . Therefore, at temperatures near the Curie point, the magnetization of the iron ions is dominant. However, since the gadolinium has a saturation moment larger than the resultant magnetization of the iron ions, the moment of the gadolinium ions is predominant at low temperatures. The temperature at which the gadolinium and iron magnetic moments are equal is called the compensation point.

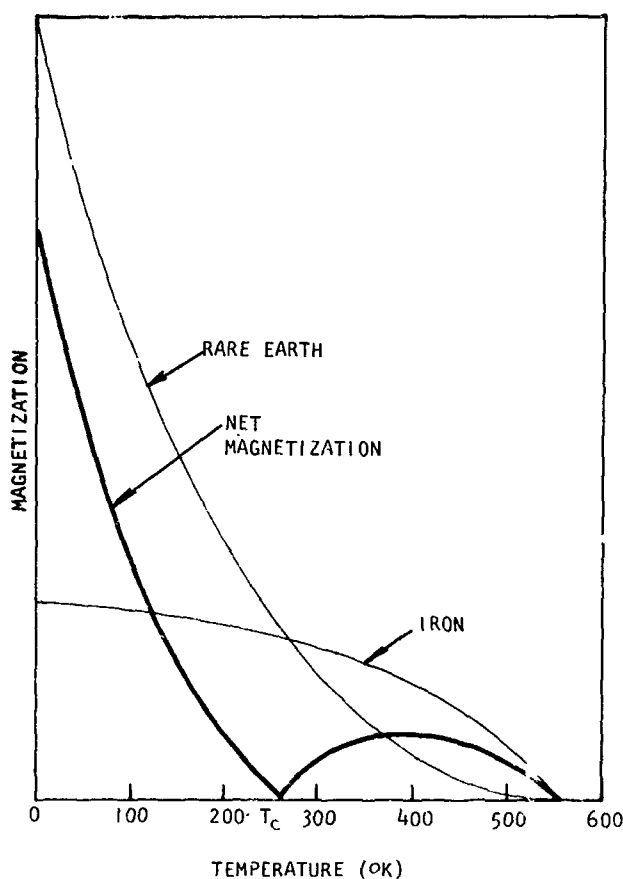


Figure 17-4—Magnetization of a typical rare earth (garnet).

## BASIC MEASUREMENTS

To design a memory based on gadolinium aluminum iron garnet, measurements of certain magnetic and optical properties of the material are essential. Both the compensation temperature and the coercivity were determined with the aid of a vibrating sample magnetometer, wherein a sample is vibrated in a dc magnetic field, and the magnetization is sensed with a pickup coil. Figure 17-5 illustrates plots of magnetization-versus-temperature of three different samples. The temperature at which the magnetization is minimum is the compensation point. Reversing the dc field and noting the reversal of magnetization gives the value of the coercive force. A typical plot is shown in Figure 17-6.

These results indicate the temperature stability of the memory. For example, if one planned to write by heating a bit  $6^{\circ}\text{C}$  above the compensation temperature, a field of 7843 A/m (100 oersted) would be needed to switch the heated area. This field would not affect the unheated portion of the platelet as long as the temperature is maintained within  $6^{\circ}\text{C}$  of the compensation temperature. The sharper the peak, the easier the writing; however, a sharp peak requires better temperature stability.

Figure 17-4 shows a plot of the magnetization of the iron ions and the gadolinium ions as a function of temperature. The total magnetization is also shown. At the temperature marked,  $T_c$ , the magnetization of the gadolinium and iron ions cancels. The compensation temperature of gadolinium iron garnet is  $15^{\circ}\text{C}$ . The substitution of aluminum for the iron reduces the moment of the iron lattice. The aluminum preferentially occupies the tetrahedral sites because the aluminum atom is smaller than the iron atom, and the tetrahedral sites are smaller than the octahedral sites. A reduction in the net magnetization of the iron lattice raises the temperature at which the iron lattice is compensated by the gadolinium lattice. This program dictated a memory which could operate at room temperature without compensation. It was found that 4 percent by volume of aluminum substituted for the iron resulted in crystals with a compensation temperature very close to room temperature.

The optical absorption measurements were obtained with a spectrophotometer. A typical run is shown in Figure 17-7. The optimum wavelength is one which has the largest rotation of polarization-per-loss by absorption. These results indicate that if the Faraday rotation is not significantly reduced, the longer wavelengths are more desirable. Faraday rotation measurements were obtained with the aid of the arrangement shown in Figure 17-8. The laser beam was modulated at 90 Hz, passed through a polarizer, the sample, and an analyzer, and then detected by a photomultiplier. The laser beam was also detected by a phototransistor and this signal in the differential amplifier. The results of a typical set of measurements are shown in Figure 17-9. From these curves it is evident that the temperature stability depends upon the magnetic field used for writing. With a field of 784 A/m (10 oersteds), no rotation occurs over a range of about 6°C. For a 1500 A/m (20 oersted) field, the temperature range over which no rotation occurred was reduced to about 3°C.

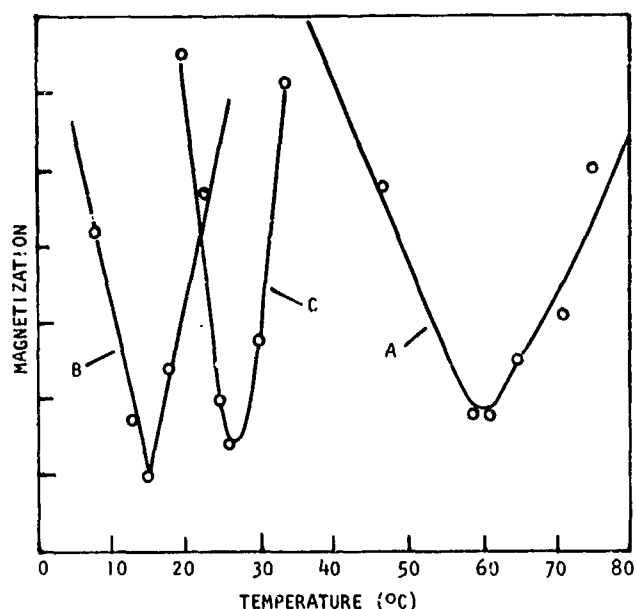


Figure 17-5—Magnetization versus temperature of three gadolinium iron garnet samples with different aluminum doping.

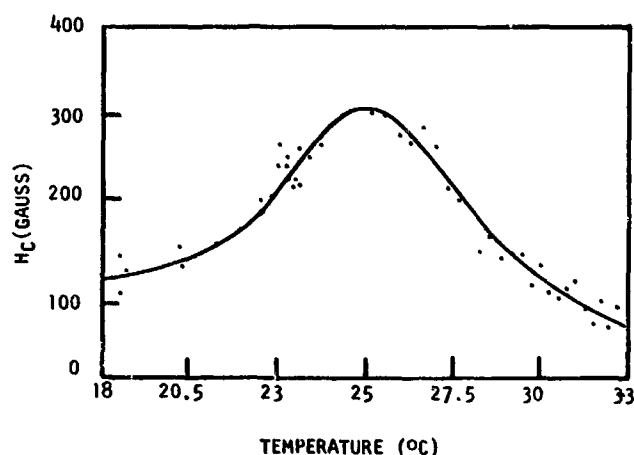


Figure 17-6—Coercive force of gadolinium iron garnet.

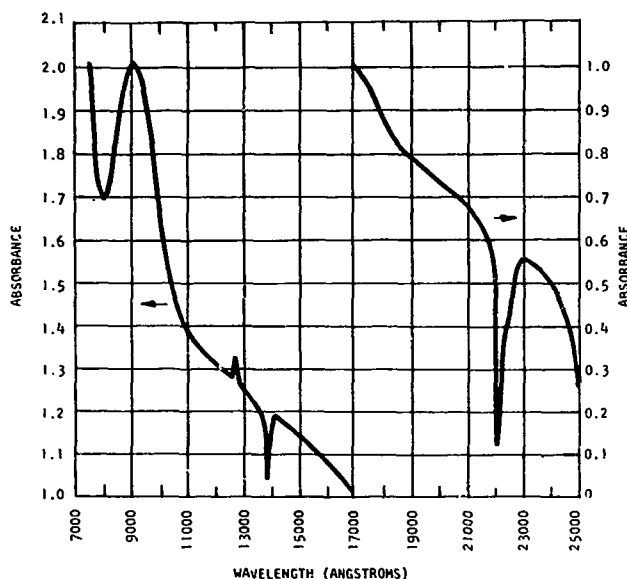


Figure 17-7—Optical absorption of gadolinium iron garnet.

## CONCLUSIONS

Based on the experimental information, a feasibility model of the concept has been designed and fabricated. A block diagram of the system is illustrated in Figure 17-10. The memory elements are on 25-micron (1-mil) centers, and it is proposed to reduce this to 2.5-micron (0.1-mil) centers. With an argon laser, Faraday rotations of 9 degrees are obtained, such that detection is no problem. The small memory

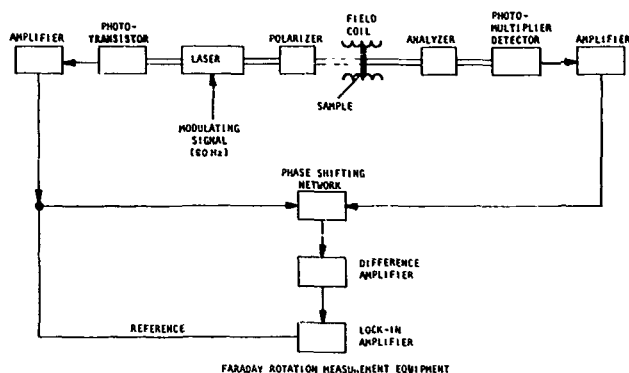


Figure 17-8—Faraday rotation measurement equipment.

elements have greatly enhanced the cycle times of the memory. Since the beam from the laser could not be reduced to this micron range, special diffraction-limited focusing lens had to be used. The present major difficulty is securing some type of nonmechanical laser-scanning apparatus. Various techniques have been proposed, such as modulating the index of refraction of crystals, employing standing waves in

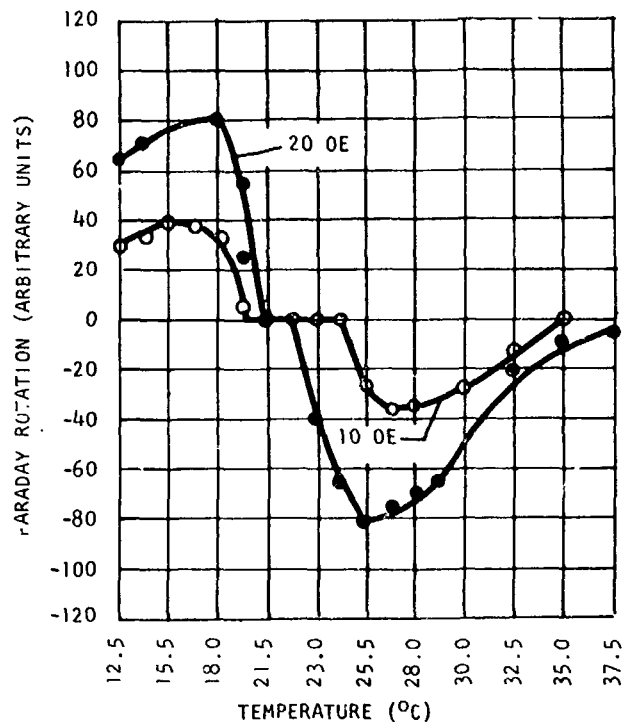


Figure 17-10—Block diagram of proposed system.

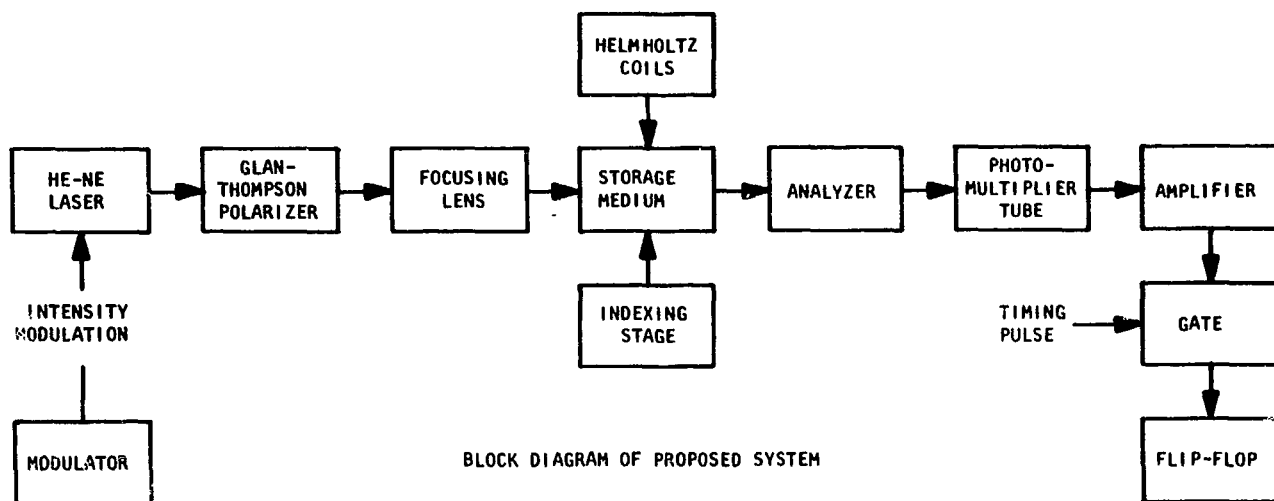


Figure 17-9—Faraday rotation versus temperature for two drive fields.

crystals, and revolving mirrors on the end of a dentist's turbine drill. All of these are basically mechanical operations and are, therefore, limited in speed. The technique offering the most promise is the combination potassium dihydrogen phosphate and calcite arrangement which can be driven by digital signals. Overall, this system promises a  $10^8$ -bit memory on a 6.5-cm<sup>2</sup> (one square inch) substrate, which can be randomly accessed without hard-line interconnections.

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## 18. RECENT DEVELOPMENTS IN THIN-FILM CAPACITORS

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There exist certain classes of materials which, due to complicated polarization mechanisms exhibit very high dielectric constants. Thin films of these materials are needed for capacitor dielectrics in order to satisfy the demand for large-value capacitors. The basic difficulty involved in the deposition of these materials is one of stoichiometry. Flash and multi-source evaporation appear to be the most promising deposition methods. Although barium titanate and lead titanate have received exhaustive study, there are several other materials, namely barium-lead zirconate, sodium niobate, and potassium niobate, which appear to have much to offer. Compatibility with silicon integrated-circuit processes is considered a prime requirement and, unless compatible deposition processes can be found, there is little likelihood that specific capacitances greater than  $1 \mu\text{f}/\text{in}^2$  will ever be widely used.

### INTRODUCTION

At the Manned Spacecraft Center (MSC), as well as elsewhere, there is a recognized need for high-value thin-film capacitors that can withstand high temperatures, occupy very small areas, and function reliably. It is the purpose of this paper, after a brief review of dielectric theory, to review the state-of-the-art of thin-film capacitors and to indicate areas in which research is being done, or needs to be done. Hardware applications will be described which require elements with high specific capacitances, i.e., high capacitance-to-area ratios.

### BACKGROUND

From electromagnetic theory it can be shown (Reference 1) that the capacitance between plane-parallel plates of area  $A$  and separation  $t$  is given by

$$C_0 = \frac{\epsilon_0 A}{t}, \quad (1)$$

where  $\epsilon_0$  is the permittivity of free space and has the value of  $8.85 \times 10^{-12}$  farads/meter in the rationalized MKS system of units. Of interest here are materials whose dielectric constants are higher than that of free space. Therefore, a relative dielectric constant  $K$  may be defined as follows:

$$C = K \epsilon_0 \frac{A}{t} . \quad (2)$$

Substituting in Equation 1,

$$C = K C_0 . \quad (3)$$

If the area is expressed in square centimeters and  $t$  is in centimeters, then the capacitance expressed in micromicrofarads is

$$C = 0.0885 K \frac{A}{t} . \quad (4)$$

In thin-film applications,  $t$  is usually expressed in angstrom units ( $\text{\AA}$ ), so one may go a step further and express the capacitance in micromicrofarads and the area in square centimeters as before, but now expressing  $t$  in angstroms ( $1 \text{\AA} = 10^{-10}$  meter).

The formula is thus in a final, workable form:

$$C = 0.885 \times 10^8 \times K \times \frac{A}{t} . \quad (5)$$

Since this formula neglects fringing, it is apparent that its accuracy depends upon the ratio of the area  $A$  to the thickness  $t$ . Corrections have been derived for fringing and may be found in the literature (Reference 2).

From the standpoint of materials, the key parameter in Equation 5 is, of course, the dielectric constant  $K$ . Dielectric constants much greater than that of free space are found in materials because of the existence of induced electric dipole moments in the individual molecules or atoms (References 3 and 4). These dipole moments give rise to a macroscopic polarization  $\bar{P}$  which is defined as follows:

$$\bar{D} = \epsilon_0 \bar{E} + \bar{P} , \quad (6)$$

where

$$\begin{aligned} \bar{D} &= \text{electric-flux density,} \\ \bar{E} &= \text{electric-field intensity,} \\ \epsilon_0 &= 8.85 \times 10^{-12} \text{ farads/meter.} \end{aligned}$$

For materials other than ferroelectrics, which exhibit hysteresis effects,  $\bar{P}$  is directly proportional to the applied electric field  $\bar{E}$ . Thus,



$$\bar{P} = k \epsilon_0 \bar{E}, \quad (7)$$

where  $k$  is a constant. Substituting Equation 7 in (6),

$$\begin{aligned} \bar{D} &= \epsilon_0 \bar{E} + k \epsilon_0 \bar{E}, \\ \bar{D} &= (1 + k) \epsilon_0 \bar{E}, \\ \bar{D} &= K \epsilon_0 \bar{E}. \end{aligned} \quad (8)$$

From Equations 7 and 8 it can be seen that the dielectric constant of a material is related to the degree of polarization present in the dielectric material. There are several mechanisms which may contribute to the total polarization  $\bar{P}$ . They are (1) the electronic polarizability, due to a displacement of the negatively charged atomic electrons in a direction opposite to the applied electric field; (2) the atomic polarizability, due to a distortion of the normal charge distribution in a molecule; (3) the dipole polarizability, due to the existence of a permanent dipole moment; (4) an interfacial polarizability, due to migration of charge carriers and entrapment by crystal defects.

The total polarizability is obtained by summing all the separate polarizabilities due to the previously-mentioned mechanisms. The total polarization  $\bar{P}$  can be found from the formula

$$\bar{P} = n \alpha \bar{E}', \quad (9)$$

where

- $\alpha$  = sum of all polarizabilities,
- $n$  = number of molecular dipoles, and
- $\bar{E}'$  = local electric field intensity.

The local electric-field intensity is proportional to the applied field, and is given approximately by the Mosotti relation for materials with no permanent electric dipole moment—

$$\bar{E}' = \frac{K + 2}{3} \bar{E}. \quad (10)$$

Therefore, when an electric field is applied to a polar or piezoelectric material (one which possesses permanent dipole moments), the electric dipoles tend to align themselves with the electric field and the polarization-vs.-field-strength curve is approximately linear.

It requires a finite length of time, however, for the different polarizabilities to respond to the applied field. When the applied frequency becomes of the order of  $\frac{1}{\tau}$ , where  $\tau$  is the response time, then there is a decrease in the polarizabilities and hence a decrease in  $K$ . In most dielectrics, however,  $\tau$  is very small, and the dielectric constant remains relatively constant over the whole radio-frequency spectrum.

In order to analyze the in-phase or resistive component of current in a lossy capacitor, a complex dielectric constant must be introduced:

$$K^* = K - jK', \quad (11)$$

where  $K$  is the real dielectric constant and  $K'$  is called the dielectric loss factor, which is zero for a lossless material.  $K'$  is related to the loss angle of a capacitor as will now be shown. Let

$$I = j\omega C V_0 e^{j\omega t},$$

where  $I$  is the total current through the capacitor and  $V_0 e^{j\omega t}$  is the applied voltage.

If  $C = K^* C_0$  is substituted, where  $C_0$  is the capacitance with free space as a dielectric, then

$$I = j\omega K^* C_0 V_0 e^{j\omega t}.$$

Substituting Equation 11:

$$I = j\omega C_0 V_0 e^{j\omega t} (K - jK'),$$

$$I = |I| \theta.$$

The phase angle,  $\theta = \tan^{-1} \frac{K}{K'}$ .

The loss angle  $\delta$  is defined as that angle by which the current fails to lead by  $90^\circ$ , or

$$\delta = 90^\circ - \theta,$$

$$\delta = 90^\circ - \tan^{-1} \frac{K}{K'},$$

$$\tan \delta = \frac{K'}{K}. \quad (12)$$

There is another group of materials which have dielectric constants much higher than those found in normal or paraelectric materials. These materials, called "ferroelectrics" may exhibit a spontaneous net polarization, that is net polarization with no electric field applied. Within certain temperature limits, dipole moments exist which are initially randomly oriented. Hence there is no initial net polarization in the crystal. With the application of a small electric field, the dipole moments begin to align themselves until there is a net polarization induced in the material (see Figure 18-1). Further increase of the field strength causes more and more dipoles to align themselves until a saturation point is reached where the degree of polarization is linearly dependent on

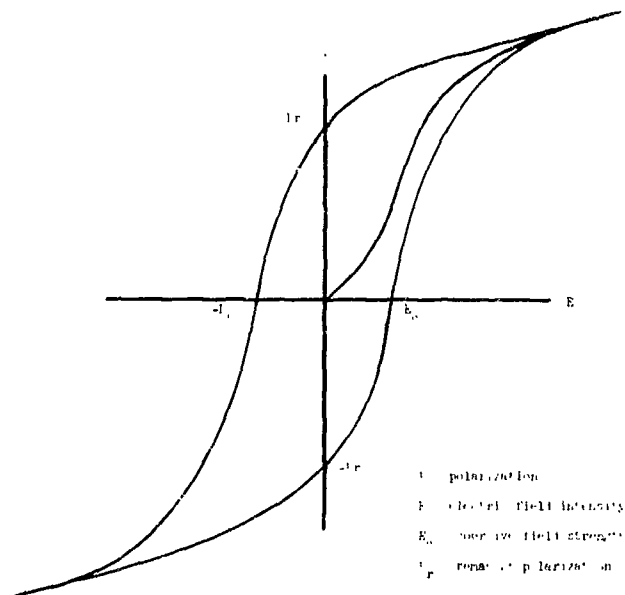


Figure 18-1—Ferroelectric hysteresis loop.

they behave as normal paraelectrics. A change in crystal structure also occurs at this temperature and is known as the Curie temperature. Above this temperature, thermal agitation destroys much of the dipole ordering and gives rise to spontaneous polarization; the dielectric constant is given by the Curie-Weiss law (References 5 and 6),

$$K = \frac{C}{T - T_c} \quad (13)$$

where

- K = dielectric constant,
- C = Curie constant,
- $T_c$  = Curie temperature, and
- T = temperature of dielectric.

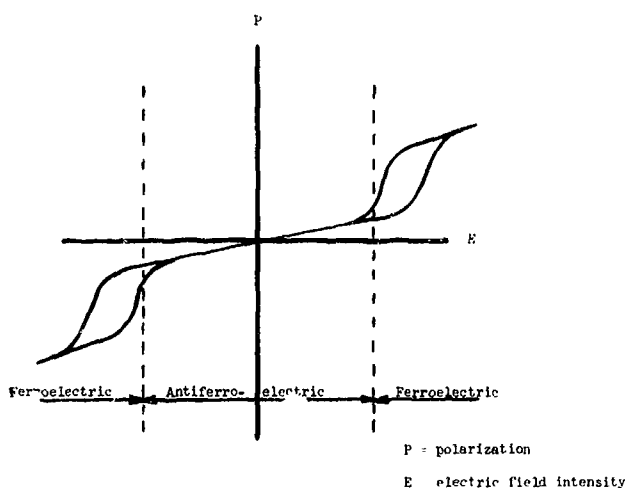


Figure 18-2—Antiferroelectric hysteresis loop.

field strength since the dipoles exist in antiparallel arrangements. That is, the material is spontaneously polarized, but the shift of one dipole moment is compensated by a similar reverse shift of another dipole moment. The application of a sufficiently high electric field eventually unbalances the antiparallel arrangements, and a net polarization is induced. At higher electric fields, the material behaves as a normal ferroelectric (see Figure 18-2).

field strength. If the field strength is then decreased, some of the dipoles will return to their initial position, although many will remain aligned with the electric field. If the field is reduced to zero, there will still be some dipoles aligned producing what is called "remnant polarization." It thus requires the application of a reversed electric field to reduce the polarization to zero. The field required to do this is called the "coercive field strength." Further increase of this reversed field will complete the polarization in the negative direction, and another reversal of the field strength will complete the hysteresis loop.

A curious property of ferroelectric materials is the existence of a temperature below which they behave as ferroelectrics and above which

## STATE-OF-THE-ART

Two of the big stumbling blocks to the realization of completely thin-film circuitry are the lack of a good high-frequency thin-film active device and the need for high-dielectric constant capacitors. The first problem is obviously out of the realm of this paper, but the latter problem will now be considered in detail.

By their very dependence on area, thin-film capacitors require a disproportionate amount of substrate space; depending, of course, on the actual value of capacitance desired. One means of achieving higher effective areas is the stacking of dielectric films interposed with electrodes. The electrodes may be connected externally to yield any combination desired, i.e., they can all be connected in parallel, in series, or in any other combination. To realize the maximum capacity, they would be connected in parallel. Degenhart and Pratt (Reference 8) made statistical studies on multilayer capacitors using silicon monoxide in a 7-layer configuration. The maximum capacity achieved was  $56 \text{ nf/cm}^2$ , with a breakdown of 20 volts. They found that the limiting factor in stacking capacitors is the rapid increase of d.c. failure probability. This is a result of the fact that the d.c. characteristics of a paralleled multilayer capacitor can never be better than the d.c. characteristics of any individual layer. Any short in an individual layer will also cause the whole structure to be shorted.

Multilayer capacitors also have been studied at MSC with much the same results. Nine-layer capacitors have been fabricated with a yield of  $0.16 \mu\text{f/cm}^2$ . Complete data is not available at this time, since leakage-current and breakdown studies have not been completed. During the course of this investigation, it was found that the pinhole problem is much more severe when dealing with multilayer films. The yield for multilayer capacitors was, therefore, found to be much less than for single-layer capacitors.

Specific capacitance, used in this paper to express the amount of capacitance available per unit, will be referred to quite often and is usually expressed in  $\mu\text{f/cm}^2$ . Specific capacitance is a function of only two parameters—the dielectric constant and the film thickness. Thus, from Equation 5 one obtains—

$$\text{Specific Capacitance} = \frac{C}{A} = 8.85 \frac{K}{t} \quad (14)$$

where  $A$  is in square centimeters,  $t$  is in angstroms, and  $C$  is in microfarads. (Table 18-1 lists typical characteristics of several thin-film dielectrics.)

The problem of getting large specific capacitances has proven to be a formidable one. From Equation 14 it can be seen that there are only two variable parameters available: One may either select a material with a higher dielectric constant, or he may decrease the film thickness. The latter is usually not practical since the capacitor must have a specified voltage rating, and decreasing the film thickness only lowers the voltage breakdown. Furthermore, it has been found

Table 18-1

Typical Properties of Common Thin-Film Capacitor Materials

Material	Formula	Dielectric constant	Specific capacitance, $\mu\text{f}/\text{cm}^2$	Thickness, Å
Silicon monoxide	SiO	6.8	0.02	3000
Aluminum oxide	Al <sub>2</sub> O <sub>3</sub>	9.0	0.04	2000
Tantalum pentoxide	Ta <sub>2</sub> O <sub>5</sub>	26.0	0.08	3000
Titanium dioxide	TiO <sub>2</sub>	56.0	0.50	1000

that films thinner than 1000 Å are subject to pinholes and are likely to be discontinuous. Thus, one is left with the task of selecting a material with a higher dielectric constant.

The search for materials with extremely high dielectric constants is not a very difficult one, but the achievement of certain bulk properties in a thin film is not an easy task. For example, bulk barium titanate (BaTiO<sub>3</sub>) has a dielectric constant of well over a 1000 at room temperature, but it requires special techniques to deposit a film which exhibits any bulk characteristics. Deposition techniques will be described in another section of this paper. The tremendous difficulties in achieving films with dielectric constants much greater than 100 have led to the almost universal selection of silicon monoxide (SiO) as a dielectric material. The reason for the widespread use of SiO is that it has been used as a coating in the lens industry for some time and its properties are fairly well known. Also, it is a well-behaved material which is readily evaporated at approximately 1250°C in 10<sup>-2</sup> mm Hg to give films with dielectric constants of approximately 6. Various other materials have been investigated, using not only vacuum evaporation, but also anodization, sputtering, and chemical pyrolysis.

## DEPOSITION PROBLEMS

Before going into the details of the MSC contract program in the field of high K materials research, it would be best to review the problems encountered when attempting to evaporate high-dielectric-constant materials. The type materials to be discussed here are inorganic compounds, many of them containing titanium whose dielectric constants range up into the thousands (see

Table 18-2

## Typical High-Dielectric-Constant Materials

Material	Electrical properties	Dielectric constant	Remarks
BaTiO <sub>3</sub>	Ferroelectric	1500	Bulk
BaTiO <sub>3</sub>	Ferroelectric	1000	Film
PbTiO <sub>3</sub>	Ferroelectric	300	Film
Ba <sub>0.4</sub> Pb <sub>0.6</sub> ZrO <sub>3</sub>	Paraelectric	2600	Bulk
NbNbO <sub>3</sub>	Antiferroelectric	500	Bulk
KNbO <sub>3</sub>	Ferroelectric	500	Bulk

Table 18-2). Since BaTiO<sub>3</sub> is typical of this class of materials, it shall be considered as an example. Bulk barium titanate has been studied for quite some time, and its polarization mechanisms have been explored quite thoroughly (References 9, 10, 11). Above its Curie point of 120° C, it exhibits the cubic structure of calcium titanate, or perovskite, in that each titanium ion is surrounded by six oxygen ions forming an octahedral, whereas the barium ions are placed at the corner of the cube and are surrounded by 12 oxygen ions. Below the Curie point, spontaneous polarization takes place, and the cell structure changes from cubic to tetragonal. It is this dimensional change that is responsible for the appearance of ferroelectric properties in the barium titanate and the associated large electrostriction. The actual mechanism involved in the paraelectric-ferroelectric transition is quite complicated, but it is essentially due to the vibrational modes of the titanium ion against the oxygen ions. Above the Curie point, the titanium ion is in its equilibrium position in the center of the octahedra; whereas below the Curie point, the titanium ion is no longer in the geometric center, but is displaced slightly toward one of the oxygens.

It is obvious that any BaTiO<sub>3</sub> film which does not have a certain degree of the crystal structure just described will not exhibit the characteristics associated with the bulk material. The difficulty associated with the evaporation of BaTiO<sub>3</sub> is that, upon heating, it decomposes into barium oxide (BaO) and titanium dioxide (TiO<sub>2</sub>). The vapor pressure of BaO is much higher than that of TiO<sub>2</sub>, and, unless special precautions are taken (such as evaporating to completion) evaporated films will be rich in BaO and deficient in TiO<sub>2</sub>. The deposition process is further complicated by the fact that TiO<sub>2</sub> may be further reduced to either titanium monoxide (TiO) or titanium (Ti), depending on how much oxygen is present in the system. The first successful attempt to deposit ferroelectric films of barium titanate was reported by Feldman (Reference 12) who deposited a charge of BaTiO<sub>3</sub> to completion on a platinum substrate. The film was then baked in air at temperatures up to 1300° C. The resulting films displayed dielectric constants up to 270 and also displayed hysteresis loops

although the polarization values were lower than the bulk material values. The properties of the film were found to be highly dependent upon baking time and temperature.

A similar technique was employed by Green (Reference 13) who evaporated alternate layers of BaO and TiO<sub>2</sub> in stoichiometric proportions, and then heated the layers in air to form BaTiO<sub>3</sub>. The advantage of this technique was that the evaporation took place at considerably lower temperatures, since BaO and TiO<sub>2</sub> evaporate at lower temperatures than BaTiO<sub>3</sub> itself. Also, Feldman's films were graded in composition, beginning with the more volatile BaO at the substrate to almost pure TiO<sub>2</sub> at the surface of the film. Green's layered structure thus reduced the distance through which the constituents had to diffuse before reacting. The principal measurements made by Green were X-ray diffraction patterns and charge-voltage characteristics, the latter definitely exhibiting ferroelectric hysteresis.

The obvious disadvantage in the techniques of Feldman and Green was that the films had to have subsequent heat treatment in air. This is undesirable from the standpoint of breaking vacuum and possibly contaminating the film. It has, for example, been found that BaO reacts with carbon dioxide in the air to yield barium carbonate (BaCO<sub>3</sub>). For this reason, circuit design at MSC is approached from the standpoint of fabricating complete circuits in a vacuum chamber without breaking the vacuum.

One possible solution to this problem was suggested by the work of Sekine and Toyoda (Reference 14) who, oddly enough, were also baking their films at various temperatures in air or pure oxygen. The novelty of their approach, however, was that they fed BaTiO<sub>3</sub> powder little by little onto a tungsten-ribbon heater kept at about 2200° C. Thus, the BaTiO<sub>3</sub> was evaporated at a very high rate, and was deposited on the substrate in stoichiometric proportions. The result was films with dielectric constants of over 1000.

A much more comprehensive study of the deposition of BaTiO<sub>3</sub> by this flash-evaporation technique was performed by Muller et al. (Reference 15). The titanate films prepared at substrate temperatures between 400° C and 500° C were shown by electron diffraction patterns to be highly crystalline (cubic), and dielectric constants up to 500 were reported. The films showed no ferroelectric behavior, however, a result the researchers explained by referring to the work of Novotsiltsev and Khodakov (Reference 16). Novotsiltsev and Khodakov found that single crystals of BaTiO<sub>3</sub> prepared at temperatures lower than 850° C possessed a cubic structure and were not ferroelectric. Ferroelectric properties could be developed only by heating the crystals above 1100° C.

Another approach to the achievement of BaTiO<sub>3</sub> films in stoichiometric proportions was that of Feuersanger et al. (Reference 17) who evaporated BaO and TiO<sub>2</sub> simultaneously, using two separate electron-beam-heated sources. The films were not heated to restore oxygen; instead, evaporation took place in an oxygen atmosphere of 10<sup>-2</sup> torr. BaTiO<sub>3</sub> was formed at substrate temperatures as low as 600° C, and dielectric constants as high as 1330 were obtained. However, further studies showed that at substrate temperatures below 900° C the films were unacceptable as capacitor

dielectrics because of their relatively high-dissipation factors, resulting from the presence of unreacted oxides (Reference 18).

## DIRECTIONS FOR FUTURE RESEARCH

The foregoing information should have made it clear that the deposition of single-crystal  $\text{BaTiO}_3$  films is a difficult process. It requires rather sophisticated deposition techniques, and is not very compatible with other thin-film processes. To date, the best method seems to be dual-source evaporation. But even this process has a big disadvantage in that the  $900^\circ\text{C}$  substrate temperature required to deposit good films would probably modify the diffusion characteristics of the active devices. It has been found that the deposition of lead titanate at temperatures of the order of  $680^\circ\text{C}$  is more compatible with silicon-integrated circuit technology. Dielectric constants in the range of 200 to 400 have been reported (Reference 19).

The Manned Spacecraft Center has long recognized the need for a basic materials study in order to find dielectric materials whose deposition processes are compatible with the fabrication of silicon active devices. In line with this interest, MSC awarded a contract to Thompson-Ramo-Wooldridge Systems for a 1-year study of high-dielectric-constant materials and their potential application to thin-film capacitors. A literature survey was undertaken at the beginning in order to select potential candidates for study (Reference 20). It was decided not to invest any more money in a study of barium titanate and lead titanate, since these materials have already received intensive study.

The search for a good dielectric material among ferroelectrics is complicated by the fact that such materials usually exhibit radical property changes with temperature variations. For example, as seen in Figure 18-3, the dielectric constant of  $\text{BaTiO}_3$  not only varies radically with temperature, but also with the direction in which it is measured. Other factors may also have to be considered, such as remanant-polarization effects, placement of Curie points, and dissipation factors. The latter is normally large in materials having high dielectric constants. The literature search was, therefore, directed toward materials which presented a minimum of the foregoing problems. In particular, a material was desired whose dielectric constant was relatively constant over a wide temperature range.

Of all the materials considered, the most promising ones appear to be a barium-lead zirconate mixture, potassium niobate, and sodium niobate. Neither lead zirconate nor barium zirconate have very high dielectric

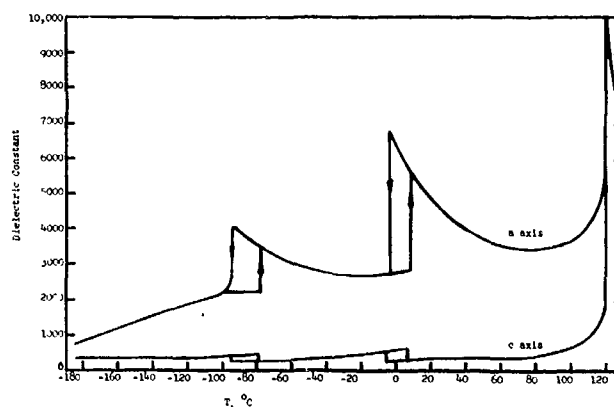


Figure 18-3—Dielectric constant of  $\text{BaTiO}_3$  as a function of temperature.



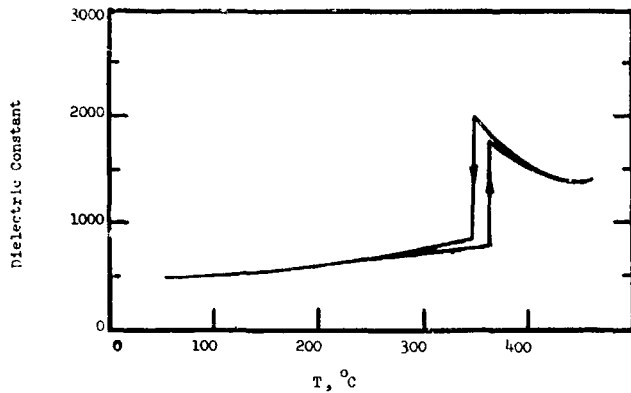


Figure 18-4—Dielectric constant of  $\text{NaNbO}_3$  as a function of temperature.

constants, but it has been found that mixtures of these two materials produce some very interesting results. In particular, it has been found that for high concentrations of barium zirconate ( $\text{BaZrO}_3$ ), the dielectric constant-temperature characteristics begin to flatten considerably to a room temperature value of about 2500 (Reference 21). At room temperature, potassium niobate has a dielectric constant of approximately 600 (Reference 22). It appears attractive as a capacitor dielectric because its dielectric constant is relatively flat from  $-10^\circ\text{C}$  to  $+200^\circ\text{C}$ .

Sodium niobate has a dielectric constant of about 500 at room temperature and increases slowly to about 700 at  $300^\circ\text{C}$  (Reference 23). Figures 18-4, 18-5, and 18-6, show typical dielectric-constant-versus-temperature characteristics for these materials. It should be remembered that all of these measurements were made on bulk materials. To date, there have been no known attempts to vacuum-deposit these materials.

The objective of this program with TRW is the achievement of thin-film capacitors whose physical and electrical characteristics represent an order-of-magnitude improvement over those available today. Present practical thin-film capacitors are limited to specific capacitances on the order of  $1\text{ }\mu\text{f/in}^2$ , although values as high as  $20\text{ }\mu\text{f/in}^2$  have been achieved in research labs using special techniques.

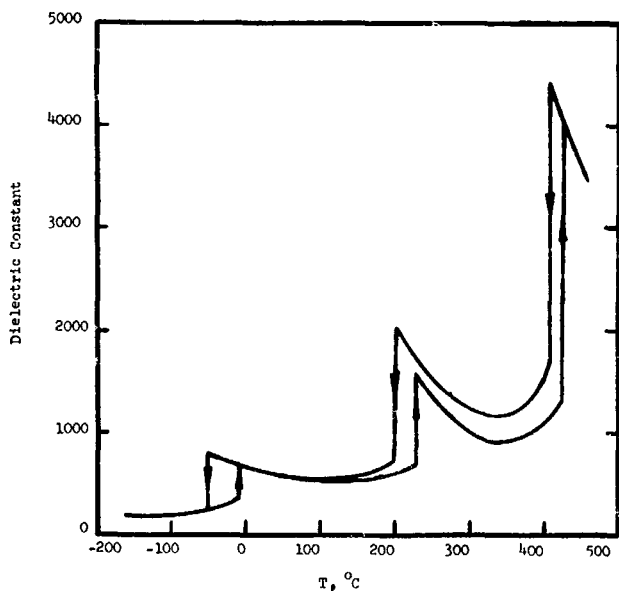


Figure 18-5—Dielectric constant of  $\text{KNbO}_3$  as a function of temperature.

## CONCLUDING REMARKS

The demand for capacitors with large specific capacitances is particularly evident in several Apollo systems. The Apollo personal communication system and the lunar TV camera contain filters and coupling networks which require large capacitive elements due to the low frequencies passed. In order to enable systems such as these to be completely microminiaturized, capacitor improvements are necessary. At the present time, capacitors too large to be thin-filmed are attached outboard as discrete elements—a method which not only presents tougher packaging problems, but also reduces reliability.

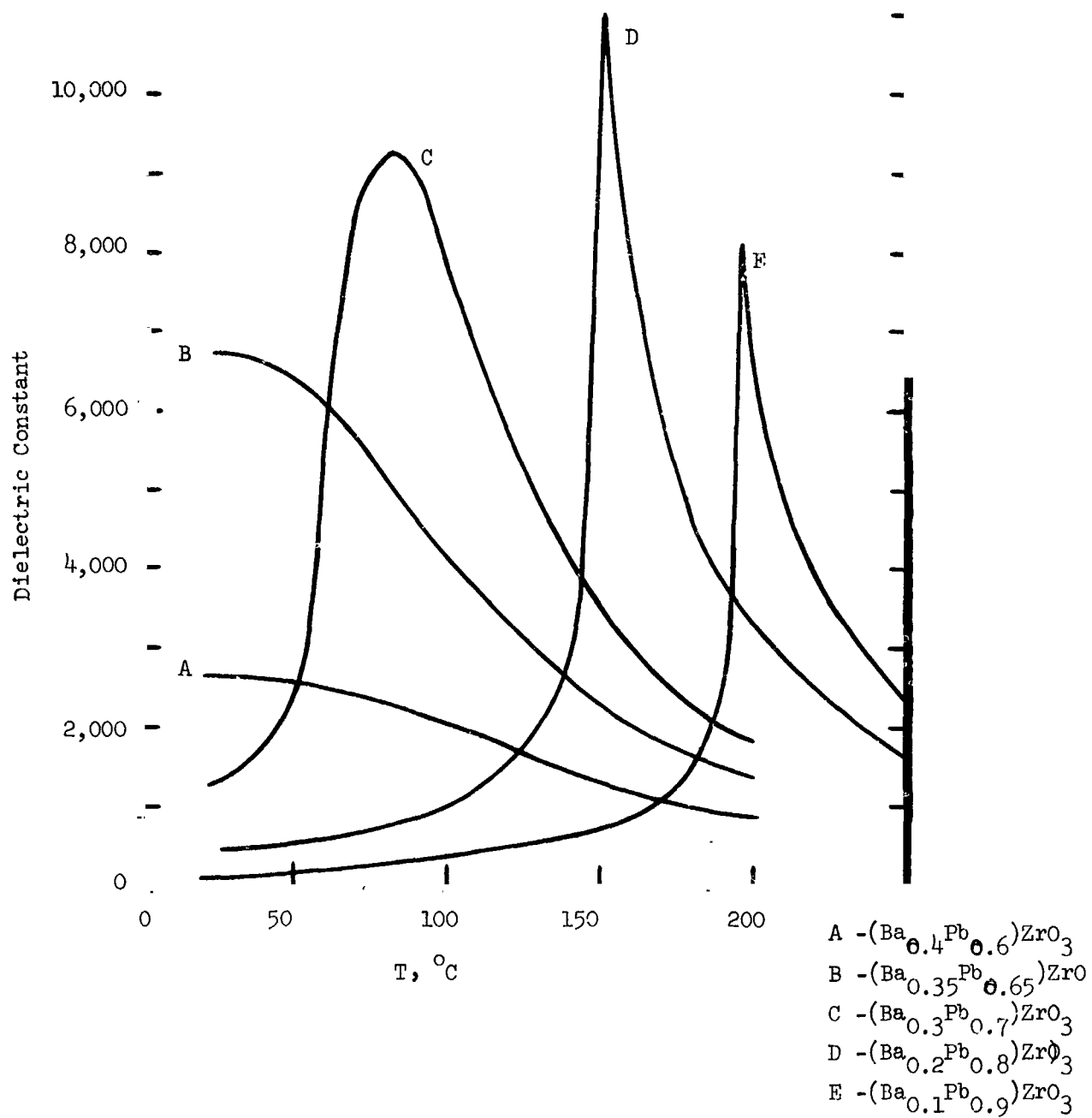


Figure 18-6—Dielectric constant of Ba-PbZrO<sub>3</sub> as a function of temperature.

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## 19. CURRENT THIN-FILM APPLICATIONS

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The present practical limitations of thin-film circuits are presented in terms of their application to the Apollo Thin-Film Personal Communication System now under development at Melpar, Inc. The system operates in the 300-Mc frequency range and imposes certain design requirements on thin-film devices which had not been considered previously. The design effort described includes research on thin-film field-effect transistors, metal-base transistors, high-frequency inductors, substrates, dielectrics, and high-permeability magnetic thin-films. The concept of the Personal Communication System, which has gone through several evolutionary phases, is described together with conclusions reached during the first phase of the development of the current thin-film version.

### INTRODUCTION

The following is a description of the development of a thin-film Personal Communication System which is currently under contract with Melpar, Inc. The system to be discussed represents one of several approaches taken by the Manned Spacecraft Center in an effort to develop the most effective and reliable system for the Apollo astronauts to use on extravehicular assignments. The system represents the communication link between an astronaut and an earth control station, as shown in Figure 19-1.

The design of the system permits voice communication between two astronauts using the spacecraft as a relay, or between the two astronauts directly by means of an emergency system. This emergency system also permits communication between the astronaut and the spacecraft. In addition, seven channels of FM telemetry data can be sent with voice by one astronaut. Telemetry from one astronaut is not retransmitted to the second astronaut. The entire voice transmission from both astronauts is, however, retransmitted to earth via the S-band link together with the telemetry data from either astronaut. Thus, a two-way path exists from the earth to the astronauts for real-time voice and data.

Figure 19-2 shows the operational concepts for the system in detail. Each backpack contains two separate and complete subsystems. The primary system operates in the duplex mode and

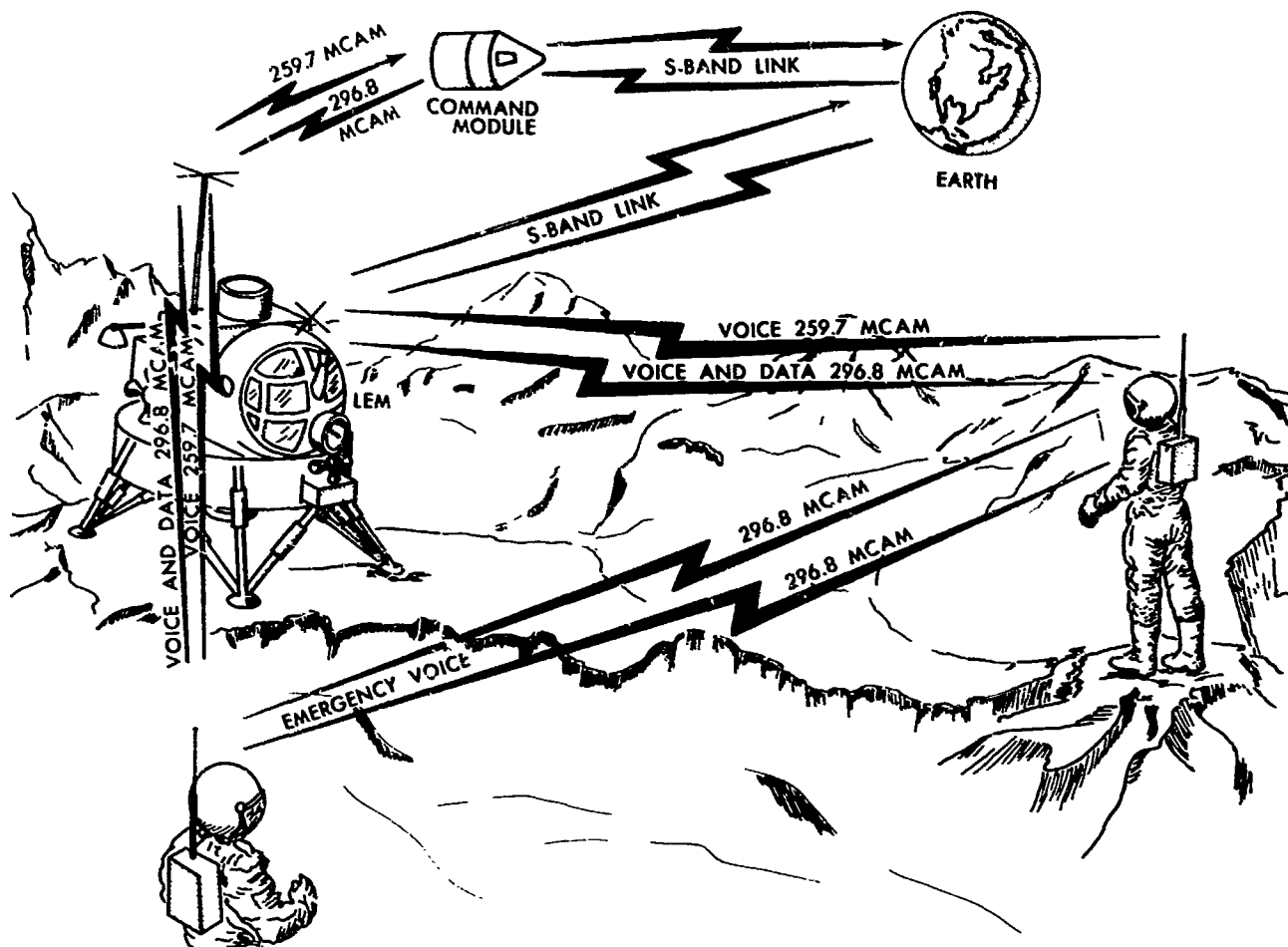


Figure 19-1—Communication link between astronaut and earth control system.

permits simultaneous voice and telemetry. The redundant system operates in the simplex mode and does not transmit telemetry. Table 19-1 shows the breakdown of the duplex and simplex systems.

The seven telemetry channels are provided to monitor the astronaut's life-support equipment. The telemetry is not demodulated on board the spacecraft because of the weight and space problems that would be involved. The parameters telemetered from the astronaut, frequency response, and subcarrier frequencies of each channel are given in Table 19-2.

Figure 19-3 gives the functional block diagram of the personal communication system. Each system is equipped with a voice-operated relay (VOX) to avoid the need for a press-to-talk switch. When telemetry is being sent, the VOX is bypassed to give the system an override feature in the event that the VOX should malfunction.

Table 19-1

## Design Considerations of the Extravehicular Communications System

Duplex mode	Simplex mode
Break-in  Operational check  Continuous telemetry  Relay advantages  (Telemetry from only one astronaut can be relayed).  Telemetry (seven channels)	Emergency voice  Redundant

## APOLLO SUIT T/M &amp; COMM SYSTEM

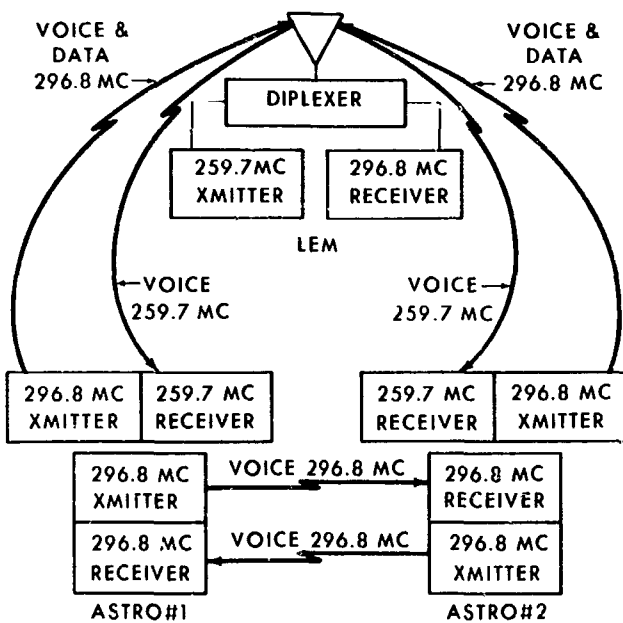


Figure 19-2—Apollo suit telemetry and communication system.

## THIN-FILM TRANSCEIVER DEVELOPMENT

The personal communication system described above has gone through several evolutionary phases since its first conception. The first-generation system, which weighed 5.6 pounds and occupied 120 cubic inches, can be compared to the current welded-cordwood version which weighs 30 ounces and occupies 30 cubic inches (see Figure 19-4). The system now under development is to be fabricated with thin-film circuits and has a design-goal weight of 10 ounces and a volume of 10 cubic inches.

Thin-film technology was chosen for the system under development, not only to take advantage of the size, weight, and reliability features of this type of fabrication, but also to use this piece of functional hardware to develop certain aspects of thin-film technology which

Table 19-2

## Extravehicular Suit Telemetry Channels

Channel no.	Data	Center frequency	Deviation (%)	Frequency response
	Voice			0.3-2.3 kc
1	O <sub>2</sub> Remaining	4.0 kc	±5	2 cps
2	Suit pressure	5.4 kc	±5	2 cps
3	Suit inlet temp.	6.8 kc	±5	2 cps
4	Battery voltage	8.2 kc	±5	2 cps
5	Body temp.	9.6 kc	±4	2 cps
6	Open	11.0 kc	±3	2 cps
7	Impedance	12.4 kc	±3	30 cps
	Pneumograph			

had previously been considered unrealizable in state-of-the-art devices. The Melpar program is a 3-year development study which is currently in the second of its three phases. The first phase involved the study of thin-film circuit elements to be used in the fabrication of the 300-Mc device. The second phase involves the functional design and fabrication of the thin-film circuits which are to be used in the actual system. The final phase will involve the actual fabrication of the transceiver.

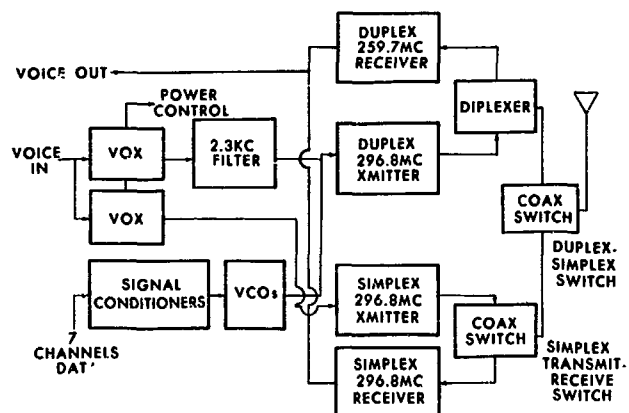


Figure 19-3—Personal communication system, functional block diagram.

In fabricating a system of this type, many aspects of the proposed design were considered



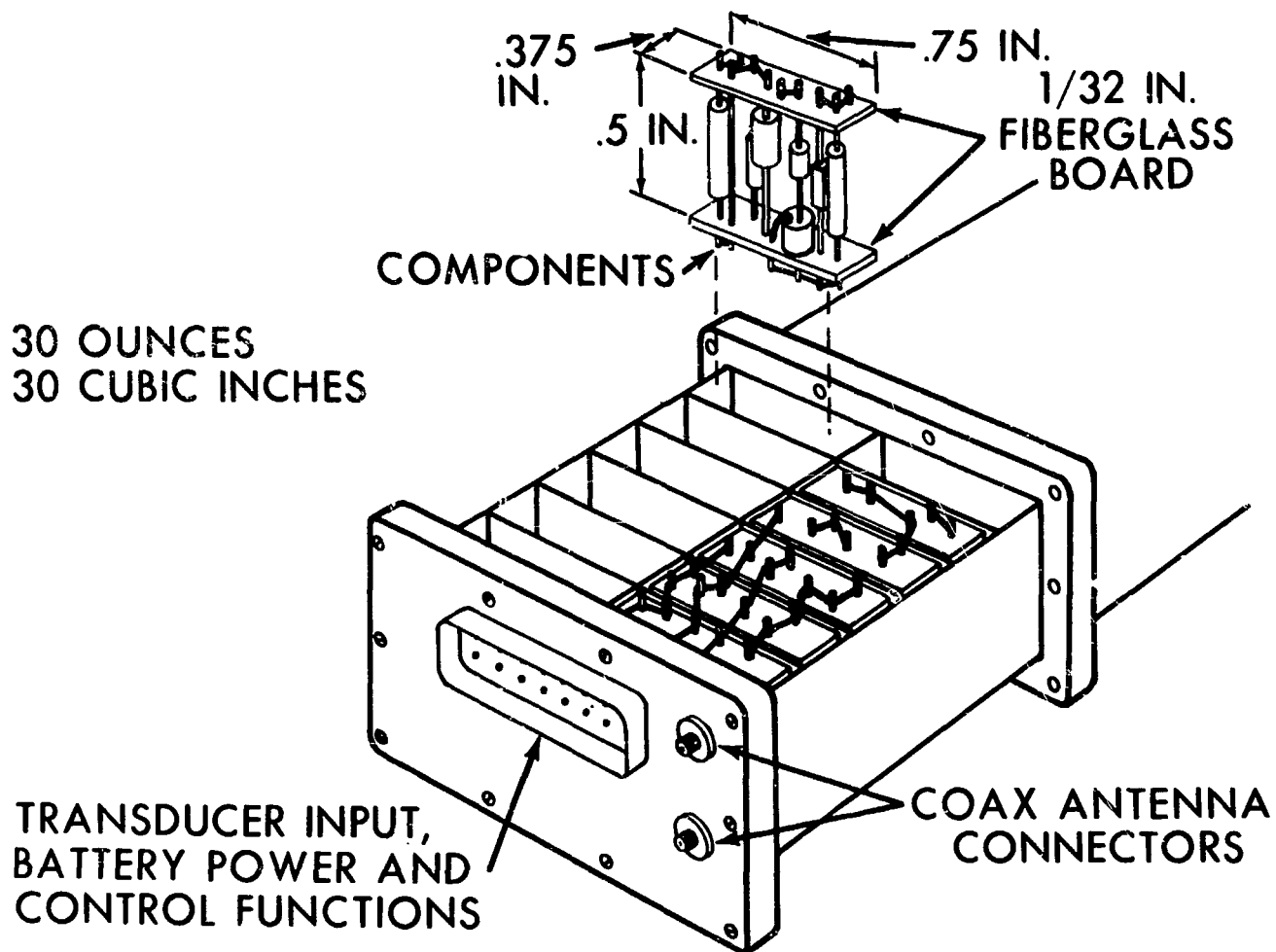


Figure 19-4—Thin-film transceiver, welded cordwood version.

to be well beyond the state-of-the-art. The first phase was, therefore, broken down into major task areas to perfect the components needed for the functional blocks in the second phase of the program. The remainder of this discussion will explore the major areas of thin-film fabrication which have been investigated, and will give an indication of the practical limitations of each phase of the technology based on the most recent developments of the program.

A detailed block diagram of the primary system is shown in Figure 19-5. The secondary system is identical except that the data channels are not included. The receiver local-oscillator and the transmitter-carrier frequencies are generated by tripling the output of a crystal oscillator. The IF frequency is 0.5 Mc, which allows the use of RC coupled stages. In thin-film form, the coils would not be practical at frequencies below 100 Mc. The crystals are designed to resonate strongly at the fifth overtone of the fundamental (approximately  $2\nu$  Mc).

Modulation of the transmitter is accomplished with gate modulation on the low-level RF stages. This method again avoids the use of a transformer, which would be beyond the range

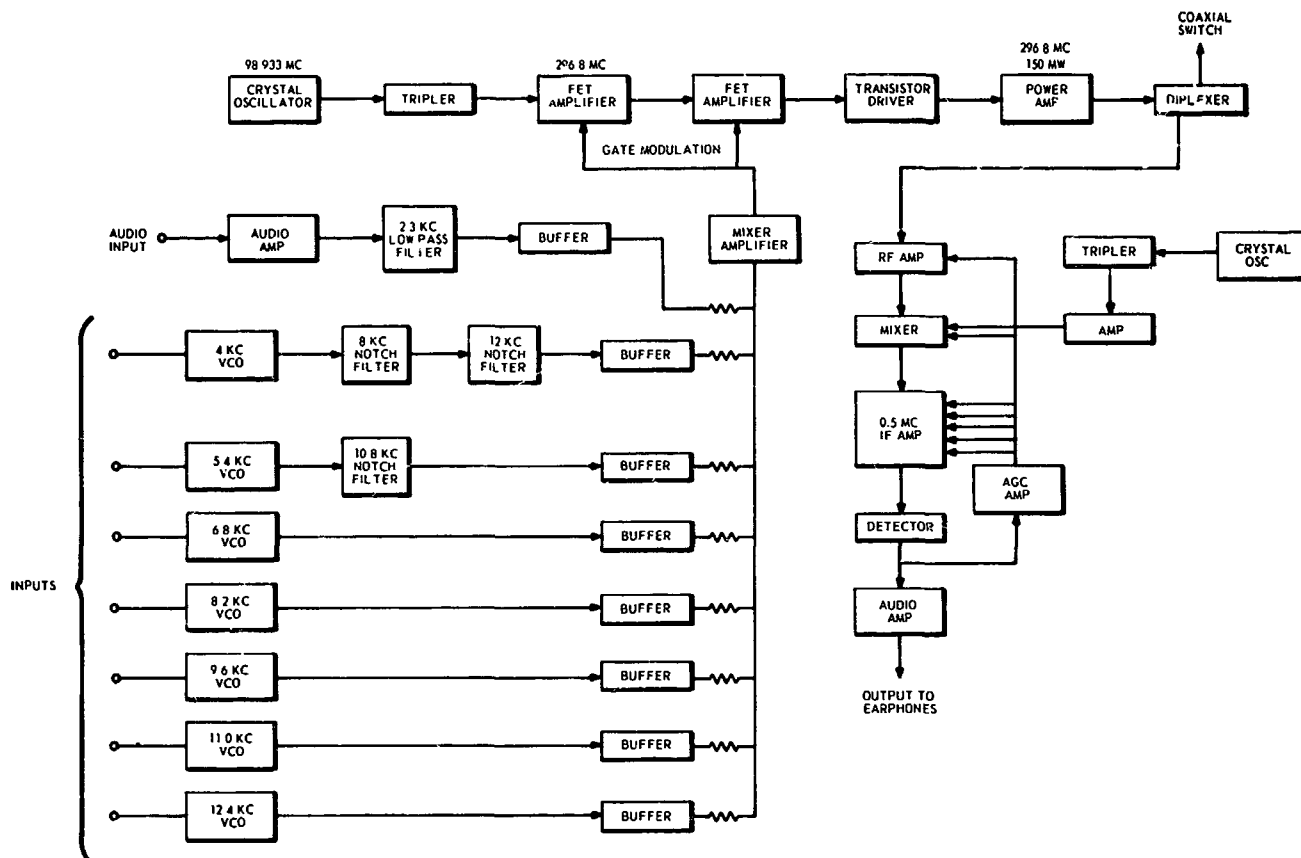


Figure 19-5—Primary system, detailed block diagram.

of thin-film capabilities. At present, the low-level RF stages are commercial FET's, and power output is provided with a conventional transistor. A full 150-mw RF breadboard has been constructed. Maximum utilization of thin films in the RF section will require further circuit improvements. Some of the coils in the present design are high  $Q$  ( $>150$ ), and, in two cases, the inductance exceeds 0.1 microhenry. The use of gate modulation eliminates the requirement for modulation power, but increases the power required in the RF stages. The present efficiency of the output stages is approximately 30 percent at 150 mw RF output.

The present technology permits approximately 90 percent of the system to be constructed in thin-film form. Table 19-3 gives a list of the circuits that are scheduled to be completely thin film.

#### HIGH-FREQUENCY THIN-FILM TRIODES

High-frequency thin-film triodes are considered to be one of the most difficult research and development areas of the program. Special geometries have been developed for high-frequency thin-film triodes (TFT's). New methods for completing the devices with extremely narrow gates

Table 19-3

## Component Estimates for Thin-Film Personal Communication Telemetry System

	Transistors	Coils	R	C	Diodes	Other
Duplex transmitter	4 (HF)	5	5	14	—	1 crystal
VCO's (7)	14 (LF)		42	14	14	—
VCO filters	—	—	18	18	—	—
VCO adder amplifier	2 (LF)	—	8	2	—	—
2.3 kc-filter	2 (LF)	—	5	5	—	—
VOX duplex	6 (LF)	—	18	6	1	—
Duplex receiver	4 (HF)	5	5	14	—	1
Simplex receiver	4 (HF)	5	5	14	—	1
Diplexer	—	5	5	—	—	—
IF duplex	15 (LF)	—	45	28	3	—
IF simplex	15 (LF)	—	45	28	3	—
Audio duplex	4 (LF)	—	12	9	—	—
Audio simplex	4 (LF)	—	12	9	—	—
Simplex transmitter	4 (HF)	5	5	14	—	1
2.3-kc filter	2 (LF)	—	5	5	—	—
VOX simplex	6 (LF)	—	18	6	1	—
Power supply	4 (High current)		15	10	4	—
	6 (Low power)				1 reference	
VCO regulators					7 references	
Totals	16 HF 76 LF	25	268	196	26 diodes	4
	4 high current	(2 large C)			8 references	

have evolved. Special attention has been given also to selecting new semiconductor materials and optimizing both new and standard TFT materials. The results have given an order-of-magnitude improvement from 1- to 2-Mc to 30-Mc devices. It is felt, however, that the design goal of 300-Mc devices can still be realized in the near future, but not within the time span of the current effort. A detailed discussion of TFT's is given elsewhere by Dr. Frank L. Baiamonte of Manned Spacecraft Center (MSC), and further consideration of these devices will be referred to that paper.

## METAL BASE TRANSISTORS AND DIODES

As a possible alternate to the high-frequency thin-film triode, metal-base transistors and diodes were also investigated during the first phase of the program. This type of solid-state

device is known as a "hot-electron" device, and gives promise as a method for achieving an ultrahigh-frequency thin-film amplifier.

Simply, this type of device consists of a thin metal film sandwiched between two n-type semiconductors, as shown in Figure 19-6. The metal-base layer is made thinner than the free path of the electrons and is accordingly transparent to injected electrons. Figure 19-7 shows an energy-level diagram illustrating the action of a metal-base transistor in equilibrium and under operating conditions. The barriers at the metal-semiconductor interface are of the Schottky type. As a forward bias is applied, the emitter interface decreases the barrier height and correspondingly increases the number of electrons which are injected into the base region by flowing over the emitter potential barrier. The injected electrons are very energetic, or hot, since they possess energies greater than the Fermi energy in the metal. The hot electrons which are transported across the "transparent" base are then collected by passing over a lower-energy base-collector barrier into the space-charge region of the reverse-biased collector. The control of the current flow from one semiconductor (emitter) to the other (collector) is exercised by varying the emitter-barrier height by means of the metal-base layer.

This type of device was considered in this program because it appeared to be especially suitable for thin-film deposition techniques, since the semiconductor portion of the device could be polycrystalline in structure, and because a very narrow thickness was required for the base region ( $100 \text{ \AA}$ ). Furthermore, the device has a predicted frequency capability of 100 Gc, which is made possible by the extremely small carrier-transit time through the base region ( $10^{-14} \text{ sec}$ ) and by the small base resistance offered by the metal film. In addition, the type of construction for this device should also provide good radiation resistance.

The approach involved in developing the metal-base transistors fabricated under this program has involved the following steps:

1. Developing suitable collector and emitter metal-semiconductor junctions. These were of an "all-evaporated" structure suitable for incorporation into thin-film integrated circuits.

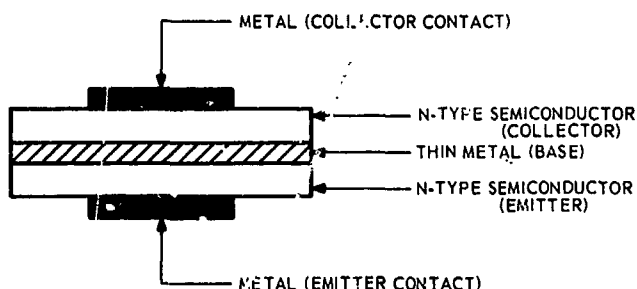


Figure 19-6--Structure of metal base transistor.

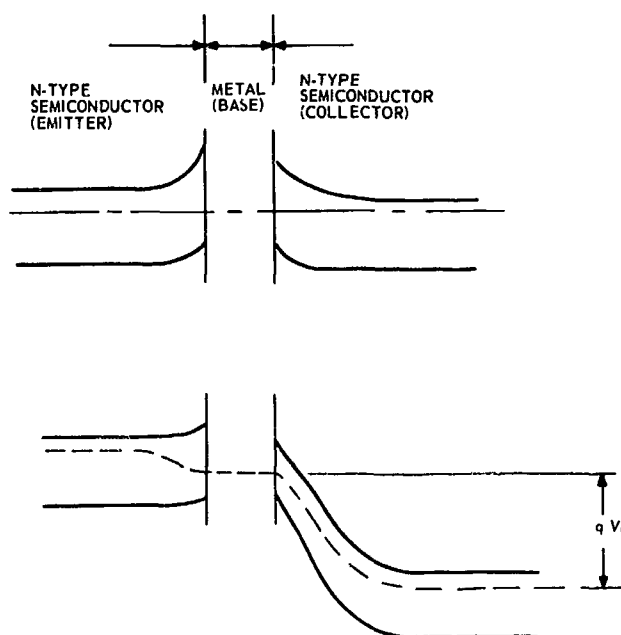


Figure 19-7--Energy diagram of metal-base transistor--  
a: equilibrium and b: under operating (biased) conditions.

2. Incorporating the junctions into a metal-base transistor structure to study device feasibility.
3. With feasible devices and encouraging amplifier characteristics, developing-high frequency operation.

The thin-film junctions for both emitter and collector sections of the metal-base transistor were fabricated by vacuum-depositing a graded CdSe-ZnSe film between two gold electrodes. Gold was considered to be a good electrode material, since the mean free path of electrons in gold has been reported to be about 740 Å for energies between 0.8 and 1.1 ev.

The semiconductor was deposited so that the ZnSe concentration was greatest at the boundary where the junction was desired. The barrier height could be varied from approximately 0.2 to 2.0 ev by changing the relative concentration of the compounds. The ability to control the barrier height made the junctions suitable for metal-base transistor fabrication, since collector efficiency is dependent on the relative barrier heights of the emitter and collector.

The varactor application of the Au-CdSe/ZnSe-Au junctions was also studied. Preliminary varactor measurements were performed on units with a 7500-Å-thick semiconductor and a  $5.81 \times 10^{-2}$  cm<sup>2</sup> area. Measurements were made with a capacitance bridge using a 1/2-volt, 100-kc signal. Typical values for capacitance ratio, obtained over a bias range of 3.5 volts, were from 1.1 to 1.2. The relatively large area restricted the zero-bias cutoff frequency to about 1.5 Mc. A reduction in junction area would have been necessary to increase the cutoff frequency by several orders of magnitude.

Metal-base transistors which exhibited a power gain better than unity were fabricated by coupling two Au-CdSe/ZnSe junctions back to back. Work has not progressed to the point, however, where a practical amplifier can be produced.

## HIGH-FREQUENCY SUBSTRATE INVESTIGATION

A number of substrate materials were investigated to determine their suitability for use in a 300-Mc system. The following substrate properties were evaluated:

1. Surface topology
  - a. Smoothness
  - b. Flatness
  - c. Edge margin
2. Compatibility with film materials
  - a. Adherence of the films to the substrate
  - b. Thermal expansivity
  - c. Chemical activity of substrate constituents

3. Resistivity
  - a. Surface
    - (1) Ultrahigh-frequency effective resistance
    - (2) Direct current
  - b. Volume (direct current)
4. Dielectric Constant
5. Thermal conductivity
  - a. Thermal shock resistance
  - b. Dissipation of circuit heat
  - c. Attainment of thermal equilibrium
6. Hygroscopicity
7. Thermal stability
  - a. Retention of physical and chemical properties
  - b. Mechanical durability

Of lesser importance, but deserving consideration, were radiation resistance, cost and availability, transparency, and ease of cutting.

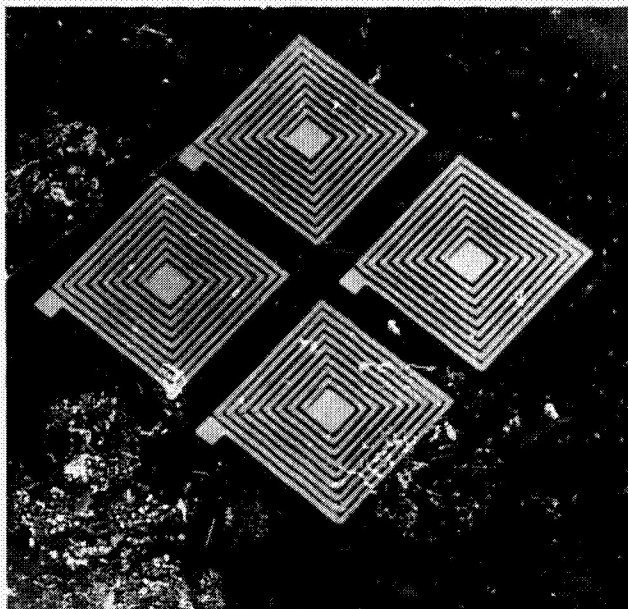
In general, most substrates were satisfactory for use in the Thin-Film Personal Communication System. The ac surface resistivity changed as a function of frequency (capacitively) for all substrates. The effective ac surface resistivity at 220 Mc was found to be of the same order of magnitude for all the substrates. The drawn-glass substrates were smoother and less costly than the ground-glass substrates. Of these, Corning Code 7059 had the highest ac surface resistivity and the lowest alkali content.

## DIELECTRIC INVESTIGATION

Two thin-film capacitor materials were studied for high-frequency application—borosilicate glass and SiO<sub>2</sub>, both with aluminum pads. Capacitors of both types were compared in operation to a commercial high-frequency silver-mica capacitor. At 400 Mc, there was no measurable difference in the performance of all three types, but borosilicate was chosen over SiO<sub>2</sub> because of its higher dc resistance, higher voltage breakdown strength, and better temperature stability.

## INDUCTORS

The purpose of the inductor study was to determine the feasibility of using thin-film inductors in the Thin-Film Personal Communication System. This means achieving usable Q values at the



Outer diameter = 0.4 inches  
 Conductor width = 0.010 inches (10 mils)  
 Spacing between conductors = 0.010 inches (10 mils)  
 Inductance = 0.5 microhenries  
 Q at 30 megacycles = 10

Figure 19-8—Thin-film inductors (completely vacuum deposited).

desired frequencies, and getting usable values of inductance at low frequencies to ensure the use of small-sized capacitors. The fact that thin-film inductors are only two-dimensional and relatively thin compared to the skin depth at high frequencies required that a detailed analysis be made of the coils which were formed.

The regular coils were deposited through 3-mil molybdenum masks in two steps. The first mask formed horizontal conductors, and the second mask formed the vertical conductors to complete a flat, spiraling square coil as shown in Figure 19-8. To provide adhesion to the substrate, a 500-Å film of chromium is first deposited, followed typically by a 29,000-Å layer of copper. The copper thickness varies as much as  $\pm 10$  percent across the substrate with typical ohms-per-square values of 0.0053. At these thicknesses, the ohms-per-square value approximates that of bulk copper.

Detailed measurements of the inductor included inductance ( $L$ ), self-resonance ( $f_o$ ),  $Q$ , resistance, and skin depth for a given area. Typical values for a multiturn coil were the following:

For a multiturn coil with 0.36-square-inch area—

$$\begin{aligned} L &= 1.5 \mu\text{h}, \\ f_o &= 110.0 \text{ Mc, and} \\ Q &= 5.0 \text{ at } 30 \text{ Mc.} \end{aligned}$$

For a multiturn coil with 0.64-square inch area—

$$\begin{aligned} L &= 0.6 \mu\text{h}, \\ f_o &= 160.0 \text{ Mc, and} \\ Q &= 12.0 \text{ at } 30 \text{ Mc.} \end{aligned}$$

Increased inductance values were obtained by depositing thin-film coils on both sides of a 40-mil substrate and interconnecting them in series at the center of the configuration. It was also attempted to stack several coils with SiO deposited between layers. Capacitance coupling, however, swamped out any possible increase in inductance value. The following results were obtained

by interconnecting multi-turn coils on either side of a 40-mil substrate with each coil having an area of 0.64 square inch—

$$\begin{aligned}L &= 2.7 \mu\text{h}, \\f_o &= 57.0 \text{ Mc, and} \\Q &= 8.0 \text{ at } 30 \text{ Mc.}\end{aligned}$$

As seen from these data, it is possible to obtain a fourfold increase in inductance, but the  $Q$  value remains essentially the same.

For high-frequency circuits, single-turn inductors were fabricated. Typical high-frequency coils exhibited the following properties.

For a single-turn coil with outside diameter of 0.4 inch—

$$\begin{aligned}L &= 0.04 \mu\text{h}, \\f_o &= 1345.00 \text{ Mc (theoretical), and} \\Q &= 50.00 \text{ at } 200 \text{ Mc.}\end{aligned}$$

For a single-turn coil with outside diameter of 0.8 inch—

$$\begin{aligned}L &= 0.04 \mu\text{h}, \\f_o &= 690 \text{ Mc,} \\Q &= 80 \text{ at } 200 \text{ Mc, and} \\D &= 0.08 \text{ inch.}\end{aligned}$$

The detailed circuit designs for the Thin-Film Personal Communication System have not been developed to the point where it is possible to establish if thin-film inductors in this performance range are usable.

## HIGH-PERMEABILITY MAGNETIC THIN FILMS

The investigation of high-permeability magnetic thin films during the first phase of the program was research-oriented. The efforts were directed toward the formation of thin-film ferrites by standard deposition techniques in complete vacuum. The goal for this effort is the possible fabrication of thin-film ferrites for use as magnetic planar cores for thin-film inductors.

Previously reported attempts to deposit ferrite films were accomplished by electron-beam evaporation of bulk ferrites in a partial pressure of oxygen, postoxidation of vacuum-deposited



metals or metal combinations, sputtering, and pyrolytic chemical reaction. The method developed under the current program involves the mixing of a small percentage of a stable and low-melting temperature oxide ( $B_2O_3$ ) with  $Fe_3O_4$  powder. The mixture is deposited from a tungsten boat on substrates at elevated temperatures at  $1 \times 10^{-5}$  torr.

The best films formed in this manner resulted from a  $Fe_3O_4$ - $B_2O_3$  mixture of 95:5 by weight. A larger ratio of  $B_2O_3$  resulted in films that were hygroscopic and light in color, whereas a lesser ratio of  $B_2O_3$  resulted in films that were reduced metal. Films of the 95:5 mixture, deposited on substrates at 200–400°C and then annealed in situ in the vacuum of  $1 \times 10^{-5}$  torr at 500–750°C, did exhibit various degrees of magnetic properties. Attempts to improve thin-film inductors by depositing these ferrites on them have not been successful because of the high dielectric loss and high film conductivity. It is felt, however, that high-resistivity ferrite films of mixed action oxides should be more useful; these are now being studied.

## CONCLUDING REMARKS

The developments discussed here are a part of a continuing effort, and it is difficult to show conclusions at this time. In predicting the performance of an operational 300-Mc system, the dielectric materials and substrates described previously are well within the current state-of-the-art. Small-value thin-film inductors are also capable of operation at 300 Mc where inductances in the 0.01- $\mu$ h range are desired. Larger-value multiturn inductors can also be applied to lower-frequency circuits. The development of a vacuum-deposited thin-film-metal semiconductor diode, which is similar in operation to the metal semiconductor junctions formed for use as gigacycle/second varactors, also points toward the future formation of thin-film junction transistors.

The effort on high frequency thin-film triodes to improve these devices for high-frequency use has evolved a TFT which, although an order of magnitude short of the 300-Mc design goal, has helped to define the operating characteristics of the field-effect mechanism. This, in turn, has been of assistance in solving device stability and lifetime problems.

The thin-film communication system described in these concluding remarks has been offered as a representation of the current state-of-the-art for this form of microcircuit technology. Since systems of this scope can now be fabricated in 90 percent thin-film form, it is felt that the space program will benefit from the size and weight savings and added reliability inherent in this method of fabrication.

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**20. A HYBRID MICROELECTRONIC A-TO-D CONVERTER**

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An 8-bit microelectronic analog-to-digital converter has been developed by Autonetics on a NASA-JPL contract. It consists of uncased monolithic digital circuits and transistors mounted on three thin-film substrates which contain precision resistors and interconnections. The substrates are encased in flat packages measuring 1.75 by 1.05 by 0.1 inches; the packages may be mounted on a printed circuit board or potted in a 3-dimensional module. The total volume of the three packaged substrates is 0.55 cubic inch, and their weight is less than 2 ounces. A conversion accuracy of 0.5 percent has been achieved with the converter. Design, fabrication, and test results are covered along with indicated problem areas, possible modifications, and improvements.

**INTRODUCTION**

The analog-to-digital converter (ADC) to be described was developed by Autonetics, a division of N.A.A., from an electrical design suggested by JPL. The work was done in the thin-film development laboratory of the Autonetics Electro-Sensor Systems Division. The purpose of the development was to investigate the feasibility of using hybrid, thin-film techniques to manufacture an ADC suitable for spacecraft use. The ADC operates on the principle of successive approximation, quantizing the input voltage into an 8-bit binary number. The input voltage range is 0 to +3 volts. This range gives the unit a resolution of approximately 11.7 millivolts. The maximum bit quantization rate is about 400 kHz, or 20 microseconds per word. The power dissipation is about 900 milliwatts.

**OPERATION**

The conversion of an analog voltage into an 8-bit digital number is accomplished by means of a series of trial comparisons between an internally generated, binary weighted voltage (BWV) and the input voltage. The comparisons take place in descending order of digital significance.

Figure 20-1 is a block diagram of the ADC, and Figure 20-2 is a simplified diagram of the logic section, showing the timing pulses and the analog decision (AD) criteria. The 8-bit register, composed of flip-flops  $Q_{11}$  through  $Q_{18}$ , serves a dual purpose in the operation of the ADC. During the quantizing period, the eight flip-flops are set, one at a time, by the timing register, composed of flip-flops  $Q_1$  through  $Q_8$ . These eight flip-flops control the digital-to-analog converter (ladder network), which transforms the reference voltage into a BWV which is then compared with the input voltage. If the BWV is greater than the input voltage, an analog

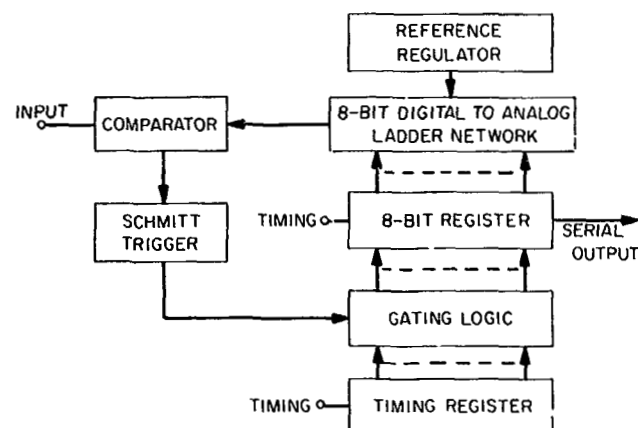


Figure 20-1—Analog-to-digital converter, block diagram.

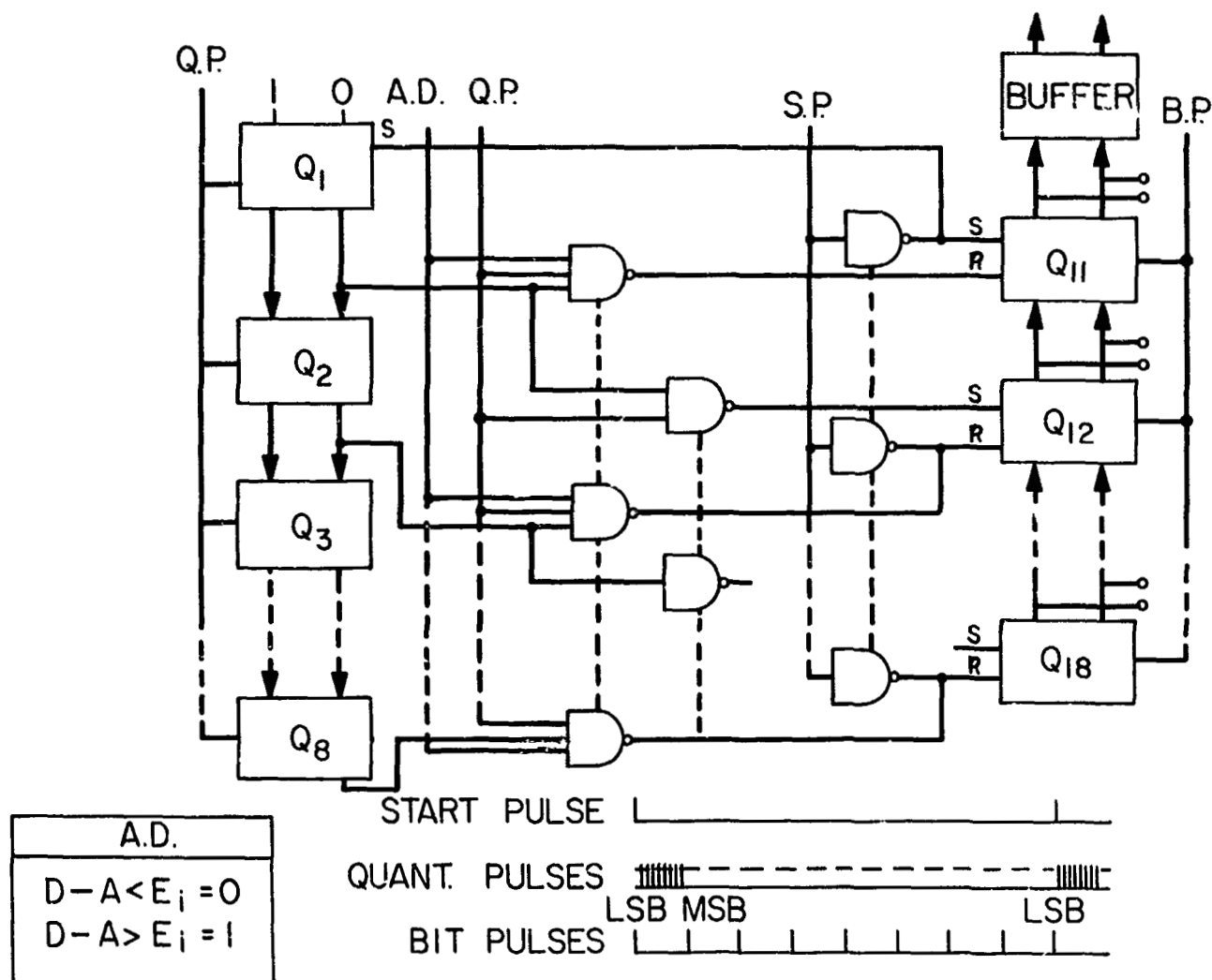


Figure 20-2—Logic portion of ADC with timing pulses and analog decision criteria.

decision is generated in the comparator which resets the flip-flop through the Schmitt trigger circuit and gating logic. The Schmitt trigger circuit simply provides logic level conversion. When the BWV is less than the input voltage, the flip-flop is not reset, and the BWV is retained in the ladder network to be summed with the next lower BWV during the next trial comparison. At any trial except the first, the BWV applied to the comparator is the sum of the BWV for that trial and all previous BWV's that resulted from successful trials, i.e., trials in which the flip-flop was not reset. After the 8th (final) trial, the ladder output becomes an 8-bit binary approximation of the input voltage; that binary number is then stored in the eight flip-flops. The eight flip-flops also are interconnected as a shift register to provide a serial readout of the binary number, with the most significant bit (MSB) appearing first.

Timing is generated externally to allow greater flexibility in the operation of the converter. The timing signals consist of start pulses, quantizing pulses, and bit pulses (see Figure 20-2). The start pulse initiates each conversion by setting a 1 into the MSB positions ( $Q_1$  and  $Q_{11}$ ) of both registers. As a precautionary measure, flip-flops  $Q_{12}$  through  $Q_{18}$  are reset to 0 by the start pulse to assure proper operation on the present voltage sample, regardless of the previous contents of the register.

The eight quantizing pulses follow the start pulse and sequence the converter through the quantizing process. At readout time, eight bit pulses are required to shift the digital number out of the register. It is not necessary that they be evenly spaced or synchronous with the start pulse as shown in Figure 20-2. There can be any amount of delay between quantization and readout or vice-versa.

## FABRICATION

The ADC was fabricated on three, 3/4 by 1-1/2 inch, thin-film substrates. The ladder network with voltage switches and reference regulator is on one substrate as shown in Figure 20-3. The comparator and Schmitt trigger circuit are on the second substrate, Figure 20-4. All of the logic is on the third substrate, shown in Figure 20-5. Integrated circuits are used only on the logic substrate.

The alumina ceramic substrates are fabricated by vacuum-depositing 100-Å, 200-ohm-per square, nichrome film onto the substrate. A 2000 Å gold film is then deposited over the nichrome. The substrates are then etched twice to expose the desired circuit pattern. Etching is controlled by standard chemical photoresists. The first etch removes gold and nichrome, leaving the resistor and connection pattern in gold on the substrate. The second etch removes the gold over the resistor pattern. Cleaning completes the thin-film fabrication process unless capacitors are needed in the circuit. Autonetics has the capability of manufacturing SiO capacitors, but none were needed in the ADC. Careful inspection of the alumina substrates for surface defects and tight control on the deposition and etching operations, here resulted in Autonetics resistor with a temperature coefficient of less than 10 ppm/°C and a stability of 0.1 percent per year. The tolerance of the resistor and capacitor values is approximately 5 percent.

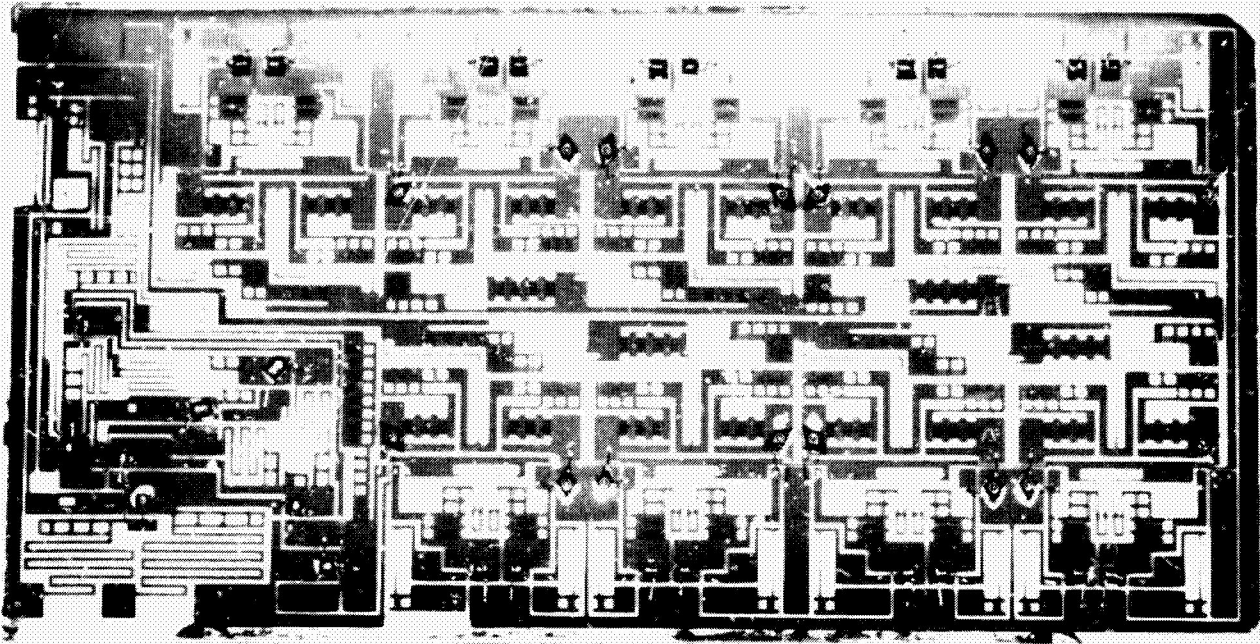


Figure 20-3—Ladder network and regulator substrate.

Most of the resistors shown on the ladder and regulator substrate are divided into segments by gold lines. This division facilitates passive trimming of the resistor value. When resistor tolerances of better than 5 percent are needed, as in the ladder network, the resistors are trimmed by adding or subtracting small resistor segments. When necessary, finer trim is achieved by scratching portions of the nichrome. The resistors in the ladder network were trimmed to 0.01 percent.

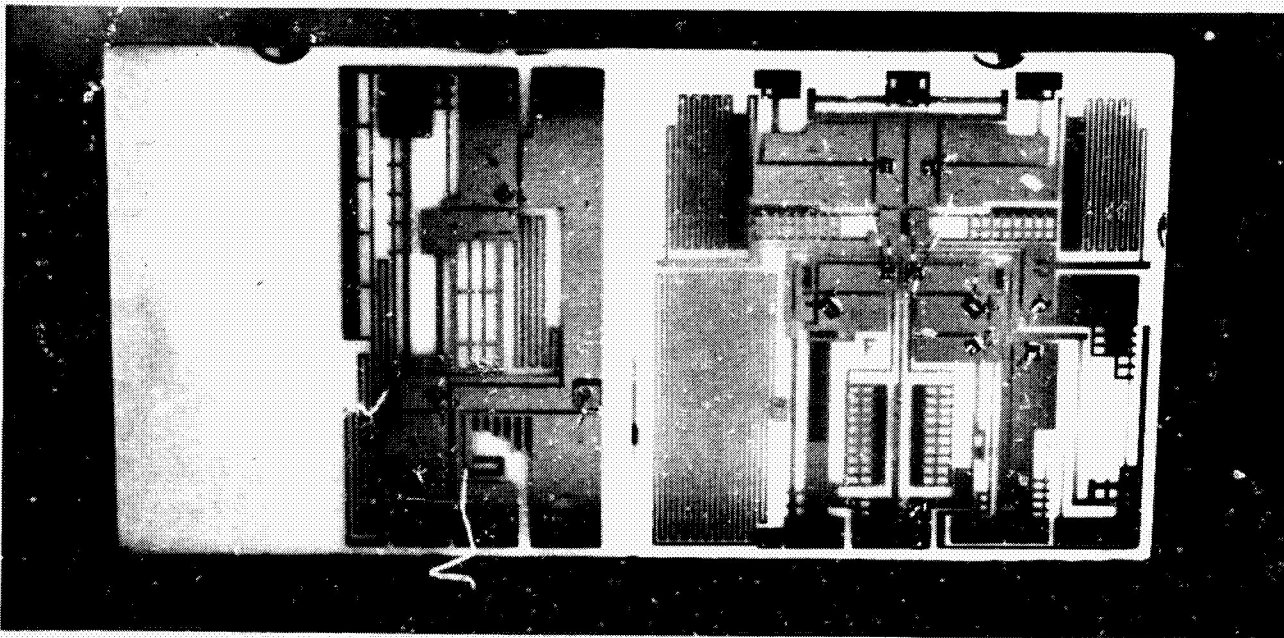


Figure 20-4—Comparator and Schmitt trigger substrate.



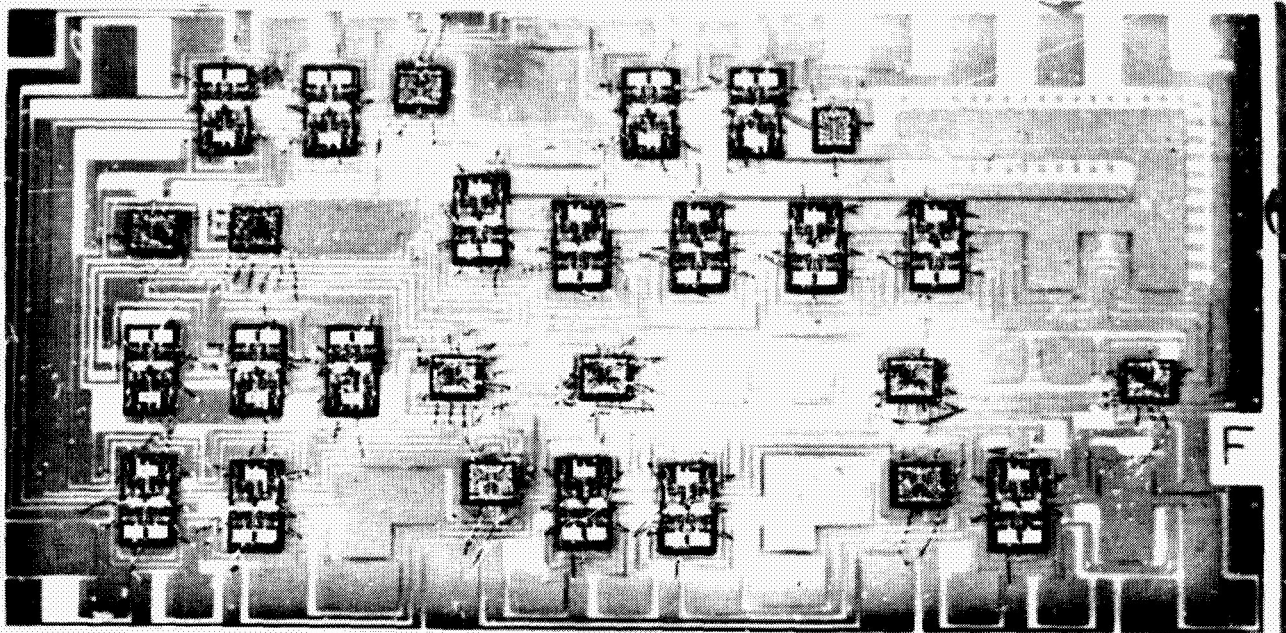


Figure 20-5—Logic substrate.

The uncased transistors, diodes, and integrated circuits were mounted on gold pads on the substrates by means of a silver epoxy. This technique allows placement of a single die on the substrate without affecting a previously bonded die. Ultrasonically bonded, 1-mil aluminum wire was used to make electrical connection between the semiconductors and the gold pads on the substrate. The substrates were mounted in special cans with a low outgassing ECCO bond adhesive which was cured at 150° C. Connection between the can leads and the pads on the substrate were made with 3-mil nickel ribbon, which was welded at both ends.

Some resistors in the comparator and regulator circuits were trimmed dynamically, with the circuit operating, before the cans were closed with Kovar lids. The three cans were mounted on an etched circuit board which provided interconnections. The completed unit is shown in Figure 20-6. The three components mounted on the board in addition to the cans consist of a resistor and capacitor to adjust and filter the reference voltage, and a resistor to adjust the comparator bias. The volume of the three cans is 0.55 cubic inch. The weight of the cans and the 3.2 by 3.45-inch etched circuit board is approximately 2 ounces.

#### FABRICATION PROBLEMS

The problems encountered by Autonetics on this task are too numerous to discuss in detail. However, the most troublesome ones and their solutions are described.

1. High saturation voltage in some of the chip transistors because of inability to make good ohmic contact to the back of the chip. The solution was the use of better transistors from another vendor.

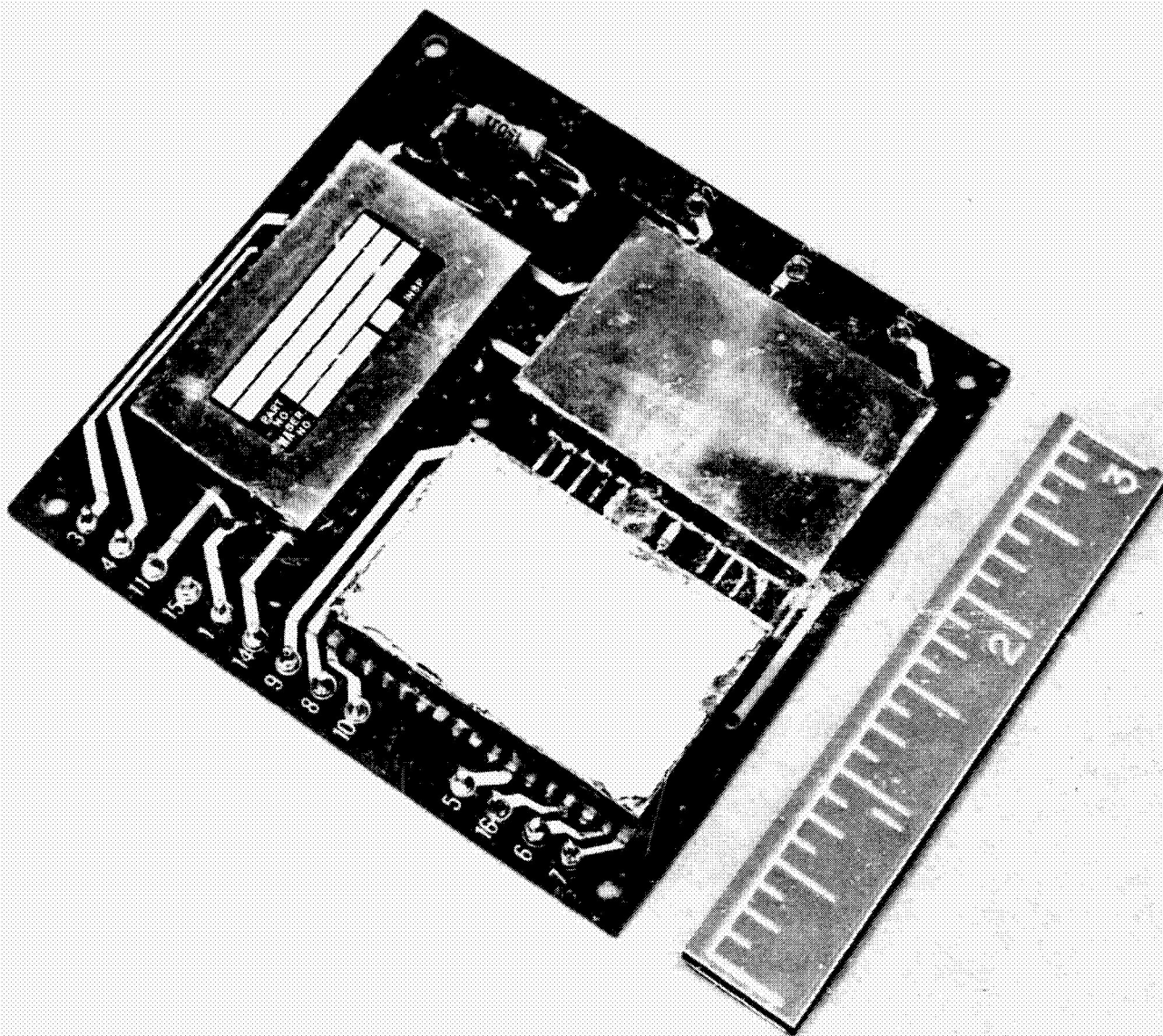


Figure 20-6—Complete ADC.

2. Intermittent shorting of input capacitors on Signetics flip-flops. Cause undetermined. The solution was the replacement of flip-flops.
3. Welding 3-mil nickel ribbon to the thin-film gold pads on the substrate. The solution lay in the extreme control of the welding process.
4. Shorts because of careless handling. The solution was the implementation of better quality control.
5. Scratches on thin film because of poor workmanship. The solution was implementation of better quality control.



6. Poor ultrasonic bonds to semiconductor chips or substrate. Some failed during vibration test. Others failed as a result of a +150°C. sterilization test. The solution was better control of the welding process.
7. Excessive length of 1-mil aluminum jumper wires on logic substrate caused shorting during vibration test. The solution was to change the substrate logic layout for shorter jumpers.
8. Excessive resistance in some of the gold film interconnections on the logic substrate. The solution was found to be lowering the resistance by plating 1 mil of gold over the thin film.

The first ADC delivered by Autonetics did not pass JPL's spacecraft environmental tests for the reasons given in items 6 and 7 above. JPL plans to have Autonetics build another ADC which will be required to pass tests for operational and sterilization temperatures, vibration, shock, and acceleration. Better quality control measures will be used.

A long-term solution to the jumper and bonding problems may be "flip-chip" mounting of the semiconductors. Autonetics, and others are working on this approach, but it is not ready for practical application where multilead integrated circuits are concerned.

## ELECTRICAL PERFORMANCE

The accuracy of the Autonetics ADC is approximately  $\pm 0.5$  percent of the full-scale input over the temperature range of  $-10$  to  $+75^\circ\text{C}$ . This accuracy was achieved, in part, by offsetting the ladder output by an amount equivalent to one-half of the least significant bit (LSB). This made the quantization error  $\pm 0.2$  percent instead of  $-0.4$  percent and  $+0$  percent. Other sources of error are the ladder network, 0.15 percent, mainly because of the switching transistor offset; the reference regulator, 0.06 percent; and indecision in the comparison function because of hysteresis, noise, and such, 0.13 percent.

The input impedance of the ADC is 1 megohm. The maximum bit quantization rate is 400 kHz at  $+25^\circ\text{C}$ ; 330 and 500 kHz at  $-10^\circ\text{C}$  respectively. The maximum readout rate is greater than 2 mHz per bit. Power dissipation is approximately 550 milliwatts in the digital section, and 380 milliwatts in the analog section, with little change over the temperature range.

## CONCLUSIONS

A hybrid, microelectronic ADC has been built and tested. The problems encountered appear amenable to corrective action. A second ADC is to be built to demonstrate the results of the

corrective action on the remaining problem areas, redesign of the logic substrate layout to eliminate long jumpers, and better quality control measures in ultrasonic bonding and handling. It is impossible to draw a final conclusion on this task at present because the ADC has not been fully qualified. However, it can be said that there is a reasonable expectation of success.

**N67-51583**

**21. PHOTON-ACTUATED, SOLID-STATE SWITCH DEVELOPMENT**

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Two types of solid-state switches with self-contained photon actuation have been under development for NASA-JPL by industrial contractors. One switch is for the precision multiplexing of low-voltage signals, and the other will be used at the outputs of a spacecraft command subsystem where complete electrical isolation is necessary for the prevention of ground loops. The switches utilize infrared radiation from a GaAs diode to turn on a phototransistor. The switches were designed to be encased in typical integrated circuit flat packages. The command isolation switch has an 8-input gate and diode driver circuit included in the package. Development, fabrication, test results, and problem area are covered.

**INTRODUCTION**

During the past few years, the planning and development of a new generation of telecommunications equipment have been in progress at JPL. This new generation of equipment is based on the use of microelectronics. Monolithic digital and analog circuits are being considered for use in all possible applications. Thin-film circuits may be used in some applications. However, it is difficult to perform certain functions with microelectronics. One such function is coupling a signal across an interface, while maintaining electrical isolation at the interface.

Signal coupling with electrical isolation is a useful and sometimes indispensable function in the design of electrical or electronic equipment. This function can be achieved by converting electrical energy into another form of energy which serves as the coupling medium. In a transformer or relay, for example, magnetic flux serves as the coupling medium. Transformers and relays are used for isolation in present day equipment, but are generally less reliable than solid-state devices and are not physically compatible with microelectronic form factors. Acoustic or mechanical force waves in a crystal can serve as a coupling medium, but the transducers are not suited to the needs of microelectronics. Heat can also be used as a coupling medium, but the response time is extremely slow. Light rays are another means of providing isolation of electrical signals. Light coupling has the advantages of being unilateral, physically compact, and capable of great speed. Until recently, however, the use of light coupling in electronics has been limited because of deficiencies in the light source.

The discovery of the phenomenon of infrared emission from the junction of a forward-biased gallium arsenide diode suggested a light source that might be suitable for microelectronic coupling. The GaAs emission spectrum peaks in the region of  $9000 \text{ \AA}$  where silicon photon sensitivity is greatest. Therefore, if the infrared emission could be efficiently coupled to a silicon phototransistor, a microelectronic, solid-state isolation device would result.

In April 1963, the Components Division of the International Business Machines Corporation was given a contract by JPL to determine if a practical photon-coupled isolation device of this type could be made. In January 1966, Texas Instruments, Incorporated was given a contract for development of another photon-actuated isolation device. The remainder of the paper will cover these developments.

## THE IBM DEVELOPMENT

The IBM contract provided for the development of a photon-actuated, solid-state switch for the precision multiplexing of analog voltages in a spacecraft telemetry system. This development lasted 18 months, and is reported in detail in IBM's final report (see Reference 1). A JPL report (Reference 2) was also prepared on this development. It is a condensation of the IBM report supplemented by JPL test results and conclusions, and is more user-oriented. The accomplishments and shortcomings of this development will be reviewed briefly. Interested persons are referred to the above references for further information.

The IBM multiplex switch is a variation of the Bright circuit, in which two transistors are connected in series and driven in the inverted mode to achieve switching with minimum offset voltage. Assembly of the switch components on a TO-18 header, and a top view of the silicon detector are shown in Figure 21-1. Note that the silicon detector is a dual-emitter transistor with common base and collector. This configuration was chosen to achieve optimum matching of the transistors for minimum offset voltage, thermal balance, fewer connections, ease of assembly, and compactness. The multiplex switch was an ambitious undertaking as a first effort in photon-coupling because certain severe requirements were placed on the silicon detector, which also had to serve as the switch element. The dual-emitter transistor was tailored to meet the difficult emitter-to-emitter requirements of high breakdown, low offset voltage, low leakage current, low on-resistance, and low capacitance. It also had to be a good light

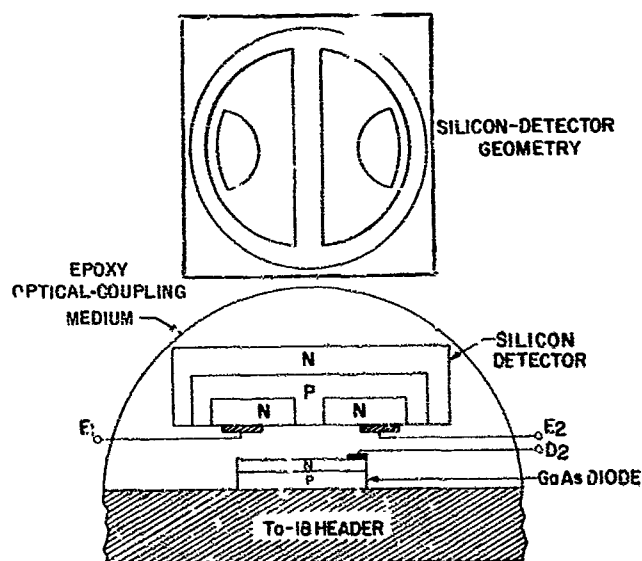


Figure 21-1—IBM multiplex switch assembly and silicon detector geometry.

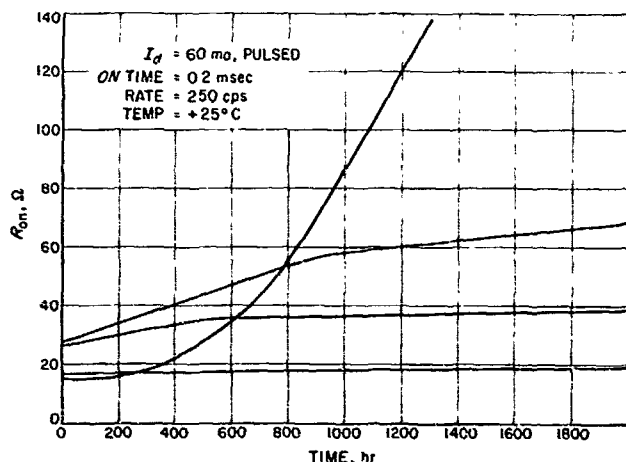


Figure 21-2—On-resistance vs. time for several IBM switches.

receiver, and have matched inverse betas of at least 20. Some of these requirements on the detector/switch were conflicting, as might be expected. For example, increasing inverse beta is a prime factor in lowering on-resistance; however, that decreases breakdown voltage. Another method of reducing on-resistance would be to increase the area of the detector, but that is not desirable because speed is an inverse function of area. Consequently, more time was spent trying to optimize the dual-emitter transistor parameters than was spent on the basic light generation and coupling problems.

Various combinations of single or double diffusion and single or double epitaxy were tried in making NPN and PNP detectors. The detector that gave the best trade-off in parameters was a NPN planar device with an epitaxial base. This device was used in assembled switches. When the multiplex switches were placed on life test, there was a gradual increase in on-resistance with time. Figure 21-2 is a graph of on-resistance vs time for several of these switches. The curves are typical of the different degrees of degradation observed. It is apparent from the different slopes that more than one mode of degradation was occurring. This instability was determined to be caused by a decrease in photon emission from the GaAs diode. A direct relationship was found between current density in the GaAs diode and deterioration of photon emission. The instability problem was first observed by IBM near the end of the contract period and was not investigated to any extent. It was theorized that the decrease in photon generation was caused by an increase in surface current, which is a nonradiative component of the total current in the diode. Bulk current is the radiative component. It was further theorized that a planar diode would minimize this problem, but IBM did not have a suitable capability for planar diffusion in GaAs at the time.

PARAMETER	CONDITION	VALUE (TEMP. RANGE -10° TO 85°C)
$R_{on}$	$I_d = 60 \text{ ma (75 mw)}$	30 $\Omega$
$R_{off}$	$V_{EE} = \pm 5 \text{ v}$	$\cdot 10^8 \Omega$
$I_{eeo}$	$V_{EE} = \pm 5 \text{ v}$	< 50 na
$R_{isolation}$	$V_{D-T} = 35 \text{ v}$	$\cdot 10^{11} \Omega$
$BV_{ee}$	$I_{EE} = 100 \mu\text{a}$	20v
$V_{oi}$	$I_d = 60 \text{ ma}$	100 $\mu\text{v}$
$t_{on}$	$I_d = 60 \text{ ma}$	< 2.5 $\mu\text{sec}$
$t_{off}$	$R_L = 10 \text{ k}\Omega$	< 10 $\mu\text{sec}$
$C_{ee}$		< 6 pfd

Table 21-1—Summary of IBM switch parameters.

The IBM contract ended with a demonstration of the parameters that could be achieved in a photon-actuated, multiplex switch, and an indication of a serious degradation mode. The parameters are summarized in Table 21-1. It is believed that they are useful parameters for many multiplexing applications. Although IBM packaged the switches in TC 18 cans for handling convenience, it was demonstrated that they could be packaged in conventional integrated-circuit flat packages, and that they were compatible with other microelectronic devices.

At the time that the IBM contract ended, Texas Instruments was doing a study (Reference 3) of degradation of light output in GaAs mesa diodes as part of an investigation of optoelectronic phenomena for the Air Force Avionics Laboratory. Two degradation mechanisms had been identified, and corrective measures were showing positive results. It was decided to wait until this work was complete before further work was initiated by JPL.

### THE T.I. DEVELOPMENT

In the latter part of 1965, it became apparent that T.I. had good control of the GaAs diode degradation problem. They had corrected the two major degradation mechanisms in mesa diodes, thermally induced stress and increasing surface current, and then had developed a low cost planar process that produced a considerable improvement in stability over their best mesa units. These planar diodes were operated for 1000 hours at 25° C at a bias current density of 1000 a/cm<sup>2</sup> with no degradation in light output (see Reference 4). Mainly because of these results, it was decided to renew JPL's development of photon isolation circuits. The multiplex switch development was not continued, however, because of the emergence of the MOS transistor as a good, low level, voltage switch. The extremely high input impedance of the MOS provides sufficient isolation for the multiplexing application.

In January 1966, T.I. was given a contract to develop a photon-actuated isolation switch for use at the outputs of a spacecraft command subsystem, where complete electrical isolation is necessary for the elimination of dc ground loops. The complete device, shown in Figure 21-3, consists of a diode AND gate, a current driver, and a GaAs diode, optically coupled to a phototransistor. The gate and driver circuit is an integrated circuit. All of these components are packaged in the 1/4 × 1/8 × 1/32-inch T.I. flat package as shown in Figure 21-4. The GaAs diode, D2, is glass-coupled to phototransistor Q3 for efficient light coupling.

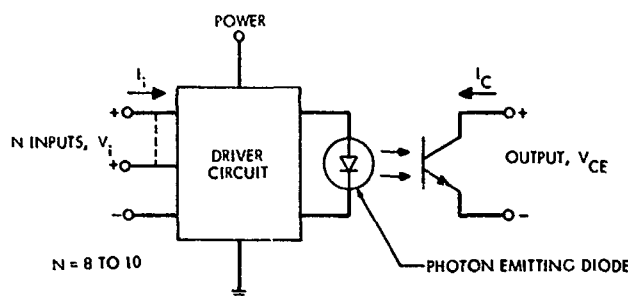


Figure 21-3—T.I. isolation switch.

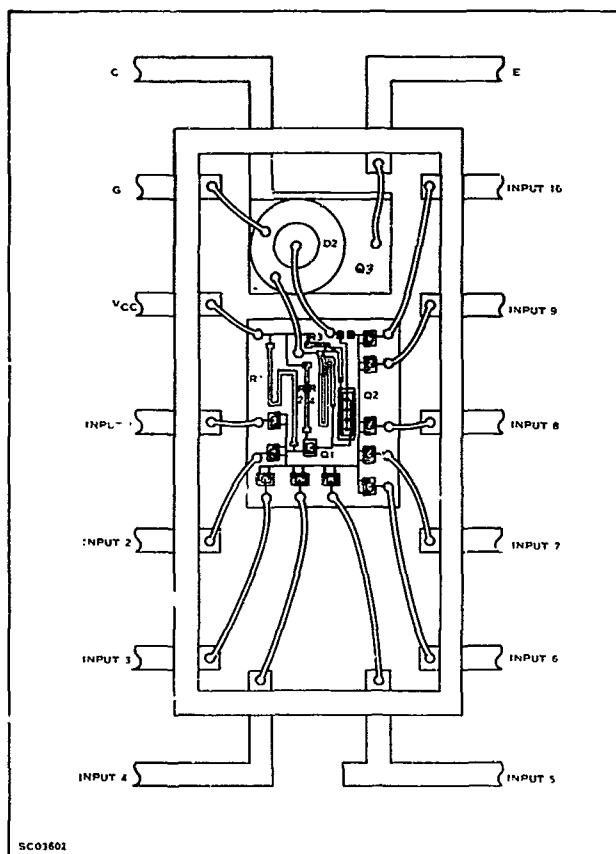


Figure 21-4—T.I. isolation switch in flat package.

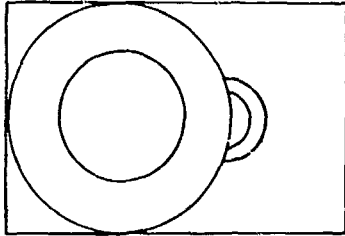


Figure 21-5—Side view of diode-transistor pair.

Figure 21-5 is a side and top view of the diode-transistor pair.

The isolation switch is being designed to have the electrical characteristics given in Table 21-2. The noise transmissibility parameter is a measure of the magnitude of a high-speed pulse that will pass through the phototransistor from emitter to collector when it is turned off. Figure 21-6 shows the test circuit for this measurement. Progress to date includes design and breadboarding of the gate-driver circuit, design and fabrication of the phototransistor, and assembly of diode-transistor pairs for testing. When the first diode-transistor pairs

Case Temperature (unless specified otherwise); -20°C to +100°C					
Parameter	Symbol	Conditions	Value		Units
			Min	Max	
Input Voltage: at "1" level	$V_i$		3.0	6.0	volts
at "0" level	$V_i$		0	1.0	volt
Input Current: at "1" level	$I_i$	$V_i = 6 \text{ v}$		50	$\mu\text{a}$
at "0" level	$I_i$	$V_i = 0.1 \text{ v}$		-1.0	ma
Output Saturation (ON) Voltage	$V_{ces}$	$V_i = 3.0 \text{ v}, I_c = 10 \text{ ma}$		0.6	volt
Output (ON) Current	$I_c$	$V_i = 3 \text{ v}, V_{ces} = 0.6 \text{ v}$	10		ma
Output Leakage (OFF) Current	$I_{ceo}$	$V_i = 1 \text{ v}, V_{ce} = 20 \text{ v},$ Temp. = +25°C Temp. = +100°C		0.1 20	$\mu\text{a}$ $\mu\text{a}$
Output Breakdown Voltage	$BV_{ceo}$	$V_i = 0 \text{ v}, I_c = 100 \mu\text{a}$	35		volts
Isolation Capacitance (between output and all other terminals)	$C_{iso}$	freq = 1.0 kc		10	pdf
Switching Times: Turn ON	$t_1$			10	$\mu\text{sec}$
Turn OFF	$t_2$			100	$\mu\text{sec}$
Noise Transmissibility	$V_n$			2.0	volts
Power Dissipation: Switch ON		$V_i = 3 \text{ v}, I_c = 0$		200	mw
Switch OFF		$V_i = 0 \text{ v}, I_c = 0$		1.0	mw

Table 21-2—T.I. isolation switch electrical characteristics.

were assembled with low temperature SeSAs glass; the transistor leakage and breakdown characteristics changed drastically with elevated temperature and time. All other parameters were satisfactory. Investigation of the leakage/breakdown problem revealed the cause to be surface inversion in the base and collector regions of the phototransistor. The inversion was caused by charge migration in the coupling glass when a potential was applied between diode and transistor. The phototransistor was modified to eliminate the collector inversion, by addition of a  $N^+$  guard ring around the base region and a field relief electrode overlapping the collector-base junction. The base concentration was increased to reduce inversion in that region.

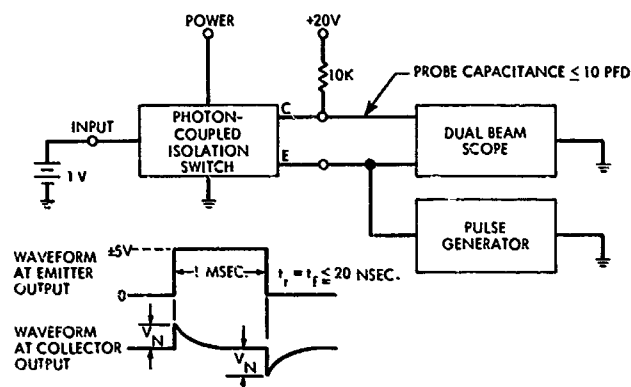


Figure 21-6—Noise transmissibility test.

Fabrication of the new phototransistor is in progress with good expectation of success. When diode-transistor pairs which meet the requirements of Table 21-2 have been assembled, T.I. will proceed with the task of integrating the gate and driver circuit and fabricating complete switches as shown in Figure 21-4.

In conclusion, it is believed that practical, photon-coupled isolation devices will be available soon. Texas Instruments is planning to make the diode-transistor pair and the complete isolation switch commercial products. They are also working on a photon-actuated multiplex switch with parameters similar to those given in Table 21-1.

Texas Instruments has had a contract, 33(615)-2643, with the Air Force for "Research on Optoelectronic Functional Electronic Blocks" for several years. At present, they are developing a commutator array and a read-only memory array, and doing supporting research in optoelectronic technology (see Reference 5). Hewlett-Packard Associates has recently published a report (Reference 6) covering their work on another Air Force contract, 33(615)-2388, for optoelectronics. The reader is referred to this material for further information on the subject.

## REFERENCES

1. IBM, "Integrated Electronic Gating System for Multiplexing Applications," NASA Document No. N65-19926, December 15, 1964.
2. D. Bergens, "Photon-Actuated Multiplex Switch Development," JPL T. R. No. 32-794, NASA Document No. N65-15347, December 15, 1965.



3. J. R. Biard, "Optoelectronic Functional Electronic Blocks, Interim Report No. 6," DDC Document No. AD 610 871, February 2, 1965.
4. J. R. Biard, Degradation of Quantum Efficiency in GaAs Light Emitters, in: 1965 IEEE Solid State Device Research Conference, Princeton, N. J., June 21, 1965, not published.
5. J. R. Biard, Research on Optoelectronic Functional Electronic Blocks, Interim Report No. 3, DDC Document No. AD 479 979, February 1966.
6. Hewlett-Packard Associates, Semiconductor Optoelectronic Phenomena Investigation, DDC Document No. AD 479 985, March 1966.

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N67-31584

22. DESENSITIZING OF MICROCIRCUITS TO VARIATIONS IN TEMPERATURE  
AND PRODUCTION SPREAD PHASE (iii):  
COMPUTER AIDED SENSITIVITY ANALYSIS

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An "In-house" NASA/ERC research task was completed as part of a long-range effort to establish design procedures for microcircuits in which the sensitivity of performance parameters to temperature variations is minimized. Representative examples from design practice are selected to develop a step-by-step procedure for design evaluation:

1. Selection of the equivalent circuit for computer-aided analysis.
2. Coding of equivalent circuit for data processing.
3. Description of computer-derived sensitivity functions.
4. Determination of optimum desensitized design configurations.  
Performance of fabricated circuits will then be compared with computer-predicted design specifications.

Phase (iii) reviews fundamentals of sensitivity analysis so that this report will be self-contained and useful to electrical engineers without any background in sensitivity analysis and computer-aided circuit design. A FORTRAN IV program is developed, which obtains a wide range of sensitivity functions from a coded input of an equivalent circuit. Several examples of increasing complexity are presented to illustrate the usefulness of the program as an aid in obtaining sensitivity functions in symbolic and numerical form.

## INTRODUCTION

The major matrix-based programs for circuit evaluation and analysis, such as ECAP and NET-2, have to use "brute-force" techniques for even the simplest sensitivity calculations. This is typically accomplished in NET-2 by changing numerical component values by 5 percent; in ECAP, this is accomplished by a series of numerical matrix inversions.

Dichotomous techniques provide sensitivities by tagging techniques without approximation. This process eliminates the errors incurred in matrix inversion, since sensitivities are computed first in symbolic form. These features are unique with dichotomous techniques, and offer advantages over the recently developed matrix-oriented techniques.

## SENSITIVITY ANALYSIS

### Sensitivity as a Design Criterion

Sensitivity,  $S_Q^P$  is defined as the ratio of the percentage change in a parameter,  $dP/P$ , to the percentage change in another parameter or element causing the change  $dQ/Q$ ; therefore,

$$S_Q^P = d \ln P / d \ln Q.$$

Typically, sensitivity is used to examine how the amplification for a given circuit varies with changes in component values because of aging. If, for example, the temperature sensitivity is too high, then the circuit is redesigned to minimize this sensitivity.

### Definition of Sensitivity (References 1-12)

If the gain of a flowgraph, Figure 22-1, is  $G = Y/X$ , then a closed flowgraph is constructed by defining  $T = X/Y$ .

Since  $H(T) = 0$  for the closed system, expansion of the topology equation yields

$$H(T) = H(\bar{T}) + TH(T'),$$

where

$$H(T') = \frac{dH}{dT}$$

and

$$H(\bar{T}) = H(T) = 0.$$

This gives the "disjoint loop" gain formula,

$$G(1/T) = -H(T')/H(\bar{T}).$$

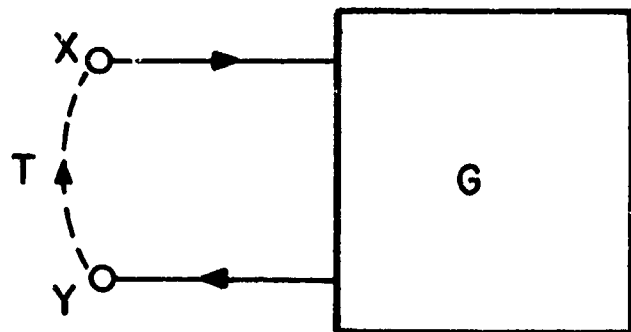


Figure 22-1—Closed system representation I.

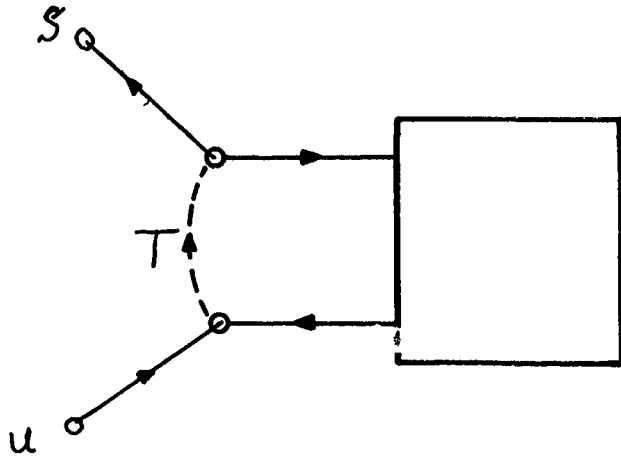


Figure 22-2--Closed system representation II.

It is valid and purposeful to assume that

$$H(G) = GH(T)$$

and

$$H(T) = TH(G).$$

Also,

$$H(\bar{G}) = H(T')$$

and

$$H(\bar{T}) = H(G').$$

Consider the transfer function illustrated in Figure 22-2:

$$S/U = TH(T')/H(T).$$

The same result is true for Figure 22-3, illustrating that this formula is independent of the location of  $T$ .

The absolute sensitivity, or the sensitivity of a closed system with respect to a parameter,  $T$ , is defined in terms of its topology equation.  $H(T) = 0$  as

$$S = S(T) \text{ if } U = 1,$$

or

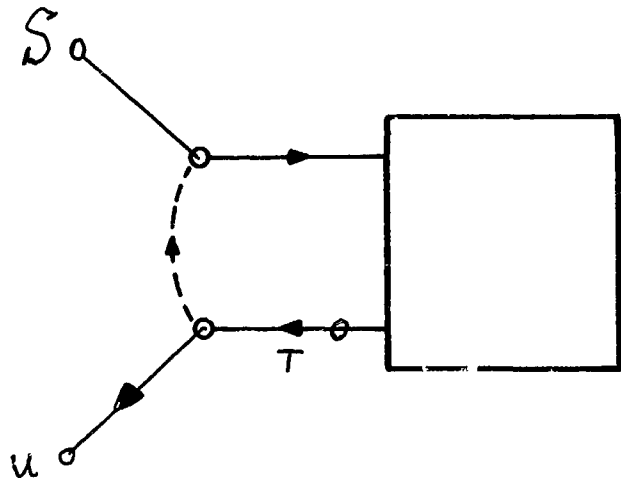


Figure 22-3--Closed system representation III.

$$S(T) = TH(T')/H(T)$$

$$= \frac{T}{H} \frac{dH}{dT}$$

$$= \frac{d \ln H}{d \ln T}.$$

The relative sensitivity, or the sensitivity of a parameter  $T$  with respect to a parameter  $R$ , both contained in a closed system,  $H(R, T) = 0$ , is defined as

$$S_T^R = \frac{d \ln R}{d \ln T}.$$

If the derivative,  $S_T^R$ , is taken at  $H = 0$ , and if  $S(T)$  is considered to be constant at  $R$ , and  $S(R)$  to be constant at  $T$ , then

$$S_T^R S_H^T S_R^H = - \frac{(\partial R / \partial T)_H}{(\partial T / \partial R)_H} \frac{(\partial T / \partial H)_R}{(\partial H / \partial T)_R} \frac{(\partial H / \partial R)_T}{(\partial R / \partial H)_T} = -1$$

Hence,

$$\begin{aligned} S_T^R &= - S(R)/S(T) \\ &= (T/R) H(T')/H(R') \\ &= - H(\bar{T})/H(\bar{R}), \end{aligned}$$

for any two variables  $R$  and  $T$  of a closed system.

### The Closed System Approach

Given a circuit containing a component  $Q$  and a desired performance specification  $P$  of this circuit, it is always possible to formulate a closed system which contains two parameters,  $P$  and  $Q$ . The topology equation  $H = 0$  is a constraint on the system from which the unknown  $P$  is calculated.

For a closed system,

$$H(P) = H(\bar{P}) + PH(P') = 0$$

and

$$H(P, Q) = H(\bar{P}, \bar{Q}) + PH(P', \bar{Q}) + QH(\bar{P}, Q') + PQH(P', Q'),$$

where  $H(\bar{P})$  is the part of  $H$  devoid of  $P$ ,  $H(P')$  is the part of  $H$  containing  $P$ ,  $H(\bar{P}, \bar{Q})$  is the part of  $H$  devoid of both  $P$  and  $Q$ , and similarly for  $H(\bar{P}, Q')$ ,  $H(P', \bar{Q})$  and  $H(P', Q')$ .

Differentiating  $H = 0$  yields

$$dH(P, Q) = H(P')dP + H(Q')dQ = 0,$$

or

$$dP/dQ = - H(Q')/H(P').$$

Since

$$S_Q^P = \frac{Q}{P} \frac{dP}{dQ} \text{ and } Q/P = \frac{H(\bar{Q})H(P')}{H(\bar{P})H(Q')},$$

then

$$S_Q^P = QH(Q')/PH(P') = -H(\bar{Q})/H(\bar{P}).$$

Thus, if

$$dH(P, Q) = 0,$$

then

$$H(\bar{T})/H(\bar{R}) = S(R)/S(T). \quad (1)$$

Therefore, when ratios are concerned,  $1/H(T)$  and  $S(T)$  are used interchangeably; this is nearly always the case in practice.

The so-called "return difference" formula,

$$S_R^G = -H(G, \bar{R})/H(G') + H(\bar{G}, \bar{R})/H(G), \quad (2)$$

where

$$H(G') = H(G', \bar{R})$$

and

$$H(\bar{G}) = H(\bar{G}, \bar{R}),$$

if  $R = 0$  describes the dependence of  $G$  on a parameter  $R$  of the system. In this expression for  $S_R^G$ , all elements can be obtained explicitly by tagging, and therefore contain no unknowns.

Since

$$G = -H(\bar{G})/H(G'),$$

and

$$S(A/B) = S(A) - S(B),$$

then

$$\begin{aligned} S_R^G &= S_R^{-H(\bar{G})/H(G')} \\ &= -S_R^{H(\bar{G})} + S_R^{H(G')}. \end{aligned}$$

Since

$$S_R^{H(\bar{G})} = -H(\bar{G}, \bar{R})/H(\bar{G}),$$

and

$$S_R^{H(G')} = -H(G', \bar{R})/H(G'),$$

the formula for  $S_R^G$  results.

Although these results are derived for linear systems, most results are not so restricted.

## DICHOTOMOUS TECHNIQUES

### Equivalent Circuit

An equivalent circuit or schematic is a generalized graphical representation of a plant. This graph is defined by the  $N$  elements of the plant. Each element is numbered and specified by an across variable (current) and a through variable (voltage).

To dichotomize, or split the problem into two parts, offers significant conceptual and computational advantages. It is implemented by describing each element as either an  $X$  element (voltage generator) or a  $Y$  element (current generator). Thus, each element is a generator of either a voltage or a current. For active as well as passive elements, each generator is controlled by either a voltage or a current. The ratio of generator variable to control variable is defined as a transmittance associated with each element, which may be frequency dependent. For a circuit with  $N$  elements,  $N$  equations relate  $2N$  variables by transmittances, which have a one-to-one correspondence with the  $N$  elements. The remaining  $N$  equations result from the interconnection of elements and are determined by the topology of the network. The interconnections of elements thus lead to  $N$  topology constraints, while the intraconnections are constraints imposed by dichotomy.

For each component of the plant, the topology and dichotomy are uniquely specified in terms of a code. This problem statement is a necessary and sufficient condition for symbolic evaluation. A further entry giving the numerical value associated with the element is required, to permit numerical evaluation.



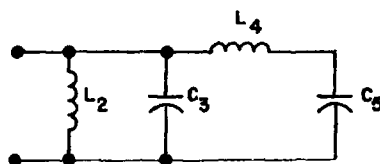
Table 22-1

Problem Statement for Example 1

A	B	C	D	E	F	G	H	K	Numerical
1	2	0	2	1	0	1	1	0	0.100E+1
1	2	1	2	2	1	0	0	1	0.666E+0
1	2	0	3	3	1	1	0	0	0.120E+1
1	3	0	4	4	-1	1	0	1	0.200E-1
3	2	1	5	5	-1	0	0	0	0.120E+3

### Coding Procedure

Each element of the plant (Figure 22-3) is assigned a code as shown in Table 22-1. Each vertex of the equivalent circuit is numbered. For each element, the vertices A and B describe the plant topology and define the positive



$$\begin{aligned} L_2 &= .66h \\ C_3 &= 1.2f \\ L_4 &= 50h \\ C_5 &= .0083f \end{aligned}$$

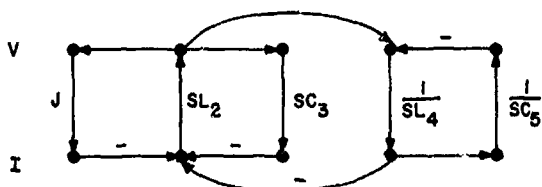
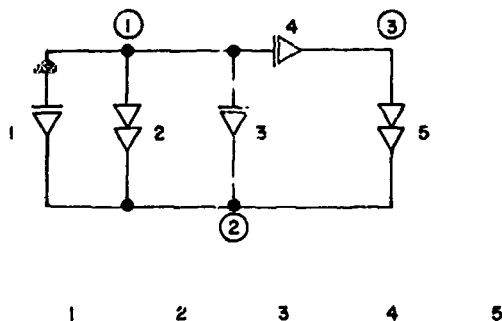


Figure 22-4—Example 1 — A.—Electrical circuit  
B.—Coded circuit  
C.—Flowgraph.

Table 22-2

Criteria for Dichotomous Assignment of C and G

G or C	Variable	Example
0	Across	Voltage
1	Through	Current
G	No Elements	
0	In parallel	
1	In series	
	Function	Node
C	Control	Contributive
G	Generator	Distributive
Z	Impedance	C = 0, G = 1
Y	Admittance	C = 1, G = 1
W	Amplification	C = 1, G = 1
V	Amplification	C = 0, G = 0

direction of the through variable (Figure 22-4B). The dichotomy is described for the generator by G, and the control by C, both C and G have binary values. The code for voltage is "0" and the code for current is "1". Values are assigned on the basis of criteria summarized in Table 22-2. Entry D in Table 22-1 describes the controlling element: for an active element, D = E, and for a passive element, D = E. Frequency dependence,  $s^F$ , is specified by Code F; if F = 0, the element is frequency-independent.

### Evaluation of Flowgraph

Routines are available for the evaluation of the flowgraph by a digital computer. A labyrinth routine obtains N first-order loops,  $L(1, N)$ , of the flowgraph, from the description contained in the  $\underline{V}$ ,  $\underline{W}$ , and  $\underline{I}$  matrices (Table 22-3). Loops

Table 22-3

V-W-T Matrices for Example 1

V	1	2	3	4	5	W	1	2	3	4	5	T	1	2	3	4	5
1								-					Y				
2	+		+	+										Z			
3								-							Y		
4								-			+					Y	
5				-													Z

of order  $k$  are obtained from the product  $P(n)$  of  $k$  disjoint first-order loops:

$$L(k, m) = \prod_{n=1}^k P(n) L(1, n).$$

The sum  $S(m)$  of all  $M$  loops of order  $k$  is directed as:

$$H(k) = \sum_{m=1}^M (m) L(k, m).$$

The topology equation,  $H = 0$ , for a closed system, is obtained by computing  $H$  from the sum  $S(k)$  over all  $K$  orders present:

$$H = \sum_{K=0}^K (k) (-1)^k H(k) \text{ with } H(0) = 1.$$

The three tagging variables,  $P$ ,  $Q$ , and  $s$  are contained in appropriate loops,  $L(1, N) = L(P, Q, s)$  depending on whether or not they include the tagging variables.

Thus,  $H = H(P, Q, s)$  yields the expansion

$$H = \sum_{\substack{p=0 \\ q=0 \\ n=0}}^{\substack{p=1 \\ q=1 \\ n=N}} (p, n) P^p Q^q s^n H(p, q, n),$$

which gives  $H$  as a function of the binary tagging parameters,  $P$  and  $Q$ , and the frequency  $s$ . Each term of this expansion is available from the computer print-out in both symbolic and numerical form.

## Construction of Flowgraph

A block diagram is a directed graph with two types of nodes, contributive nodes, or summing points, and distributive nodes, or sampling points. It is, of course, immaterial whether the description is expressed in matrix form or as a directed graph, either with "blocks" for transmittances, or in terms of Mason's improved notation.

A flowgraph is the block diagram of a system, such that each element of the system is described by two variables. This definition implies a binary decision by selecting a direction of functional dependence between these two variables, to illustrate  $z$  or  $y$  elements for a passive network (Table 22-2). The essential feature in this definition of a flowgraph is the dichotomy of elements; that is, the classification of elements into two mutually exclusive categories, subject to the rules of block diagram construction. The dichotomous choice of elements is presented in Table 22-3 by a matrix  $T$ .

The matrix in Table 22-3 describes the relationships among the cross variables, while  $W$  describes the relationships among the through variables in the system. The parameter descriptions in the  $T$  matrix always exhibit the functional dependence from contributive node to distributive node, regardless of whether the two elements are active or passive, or real or tagging elements. On the other hand, the functional relationship exhibited in the  $V$  matrix is the opposite of that exhibited in the  $W$  matrix.

Once the dichotomous selection has been made, a flowgraph is a unique description of a given plant, and no other flowgraph is possible. A program to construct the  $T$ ,  $V$ , and  $W$  matrices from a set of algorithms has been written, and can be obtained from COSMIC (Reference 28).

## Tagging Parameters

The  $H$  tag in Table 22-2 relates the quantities to be determined, such as ratio of response to drive. The code specifies that if  $H = 0$ , the parameter is known; and if  $H = 1$ , the parameter is unknown. The  $H = 1$  parameter converts the open flowgraph to a closed flowgraph by inserting an unknown, or "fictitious" transmittance  $P$ . The plant can essentially be viewed as a "black box," with input and output connected by an unknown transmittance. This unknown is to be determined by the topology equation,  $H(P) = 0$ . The mathematical artifice of setting  $P = j$  yields  $H(P) = H(\bar{P}) + jH(p')$ , which the computer carries as a known complex number. Both  $\text{Re } (H) = H(\bar{P})$ , the loop devoid of  $P$ , and  $\text{Im } (H) = H(p')$ , the loop containing  $P$ , are available from the flowgraph. Summing of loops, observing the  $H$  tag, yields

$$j = H(\bar{P})/H(p').$$

The  $K$  tag in Table 22-1 denotes the element  $Q$ , which induces a change in the performance  $P$ . The sensitivity,  $d \ln P / d \ln Q$ , is then obtained by tagging  $P$  by  $H = 1$ , and  $Q$  by  $K = 1$ .

For example, in

$$\begin{aligned} S_R^G &= \frac{H(G', \bar{R})}{H(\bar{G}')} - \frac{H(\bar{G}, \bar{R})}{H(\bar{G})} \\ &= \frac{H(1, 0)}{H(1)} - \frac{H(0, 0)}{H(0)}, \end{aligned}$$

all subsets in  $H(G, R)$  are known functions.

## THE CALCULUS OF SENSITIVITIES

### Definitions

If  $H = 0$  is not implied, then

$$\begin{aligned} S_P^H &= \frac{d \ln H}{d \ln P} \\ &= \frac{PH(P')}{H} \\ &= 1 - \frac{H(\bar{P})}{H}. \end{aligned}$$

Also,

$$\begin{aligned} S_{TR}^H &= \frac{d \ln S_T^H}{d \ln R} \\ &= S_R^{H(T')} - S_R^H + S_R^T \\ &= \frac{H(\bar{R})}{H} - \frac{TH(T', \bar{R}) + RH(R')}{TH(T')}. \end{aligned}$$

Usually,  $S_R^T = 0$ , which yields

$$S_{TR}^H = S_R^{H(T')} - S_R^H,$$

and

$$\begin{aligned}
S_{TRP}^H &= S_{RP}^{H(T')} - S_{RP}^H \\
&= \frac{H(T', P', \bar{R})}{H(T', P')} - \frac{H(R', P')}{H(T')} + \frac{H(\bar{P})}{H}.
\end{aligned}$$

### Chain Rule

If  $R = R(X, Y, Z)$ , then

$$S_T^R = S^R X^{S^X} T + S^R Y^{S^Y} T + S^R Z^{S^Z} T,$$

or

$$S(R) = S_X^R S(X) + S_Y^R S(Y) + S_Z^R S(Z).$$

To illustrate, if  $R = X + Y + Z$ , then

$$S_X^R = X/R,$$

and

$$S(R) = (X/R)S(X) + (Y/R)S(Y) + (Z/R)S(Z).$$

### Product Rule

$$S(AB) = S(A) + S(B),$$

and

$$S(1/A) = -S(A).$$

Since

$$S_R^T = 1/S_T^R,$$

then

$$1/S_{AB}^T = 1/S_A^T + 1/S_B^T,$$

and

$$S_{B/R}^{A/B} = (1 - S_R^A)/(1 - S_R^B).$$

### Sensitivity of Sensitivity

Assume that  $H(X, Y) = 0$ , and consider

$$\begin{aligned} S(S_Y^X) &= S(H(\bar{Y})) - S(H(\bar{X})), \\ &= -S(S_X^Y). \end{aligned}$$

If

$$\begin{aligned} S_R^{H(\bar{P})} &= \frac{dH(\bar{P})}{dR} \frac{R}{H(\bar{P})} \\ &= \frac{RH(\bar{P}, R')}{H(\bar{P})} \\ &= 1 - \frac{H(\bar{P}, \bar{R})}{H(\bar{P})}, \end{aligned}$$

and

$$\begin{aligned} S_R^{H(P')} &= \frac{dH(P')}{dR} \frac{R}{H(P')} \\ &= \frac{RH(P', R')}{H(P')} \\ &= 1 - \frac{H(P', \bar{R})}{H(P')}, \end{aligned}$$

then

$$S_R^{S_Y^X} = S_{YR}^X = \frac{H(\bar{X}, \bar{R})}{H(\bar{X})} - \frac{H(\bar{Y}, \bar{R})}{H(\bar{Y})}.$$

Therefore,

$$S_{PR}^T = -S_{TR}^P,$$

and

$$S_{PRQ}^T = -S_{TRQ}^P.$$

Also,

$$S_{(Y/R)}^X = \frac{S(X)}{S(Y) + S(R)},$$

and

$$S_{(Y/R)}^X = \frac{S(X)}{S(Y) - S(R)}.$$

## EXAMPLES

### Example 1

Example 1 evaluates the sensitivity of the input impedance of the two inductors of the circuit shown in Figure 22-4A. Figure 22-4B is the coded circuit. The coding with the coded input to the computer (described previously) is shown in Table 22-1. Table 22-3 displays the computer output of the flowgraph ( $v$ ,  $w$ , and  $T$  matrices) from which the actual flowgraph (Figure 22-4C) is constructed. Table 22-4 shows the flowgraph evaluation, by listing the transmittances contained in each loop, along with the  $S$  and  $J$  tags and the numerical value for each loop.

Table 22-5 lists the computer output of the function which is necessary for the actual input impedance and sensitivity evaluation. The ratio

$$H(j')/H(j) = (.66S + 1.6S')/(2.4S^{-1} + 2.9 + .8S^2)$$

gives the input impedance of the system. By solving for  $H(\bar{L}_2)/H(\bar{j})$ , one obtains the sensitivity of  $Z_{in}$  to  $L_2$ .  $(1. + 2.4S^{-2})/(2.4S^{-2} + 2.9 + 0.8S^2)$  according to Equation 2 with  $H(j', \bar{L}_2) = 0$ . The sensitivity of  $Z_{in}$  to  $L_4$  shows  $S_{L_4}^Z$  is then equal to

$$H(\bar{L}_2, \bar{j})/H(\bar{j}) = (1. + .8S^2)/(2.4S^{-2} + 2.9 + .8S^2) = -(.66S)/(.66S + 1.6S^{-1}) = H(\bar{L}_2, j')/H(j').$$

Table 22-4

Flowgraph Evaluation for Example 1

Loops	Transmittances	J	S	$\pm$	Numerical
L(i)	1 2 3 4 5				
1	1 2	1	1	+	.666E+0
2	2 3	0	2	+	.800E+0
3	2 4	0	0	+	.133E-1
4	4 5	0	-2	+	.240E+1
5	1 2 4 5	1	-1	+	.160E+1
6	2 3 4 5	0	0	+	.192E+1

Table 22-5

Necessary Data for Sensitivity Evaluation-Example 1

$H(j')$	$L_1/(L_2 C_2 S) + L_1 S$	$.66S + 1.6S^{-1}$
$H(\bar{j})$	$1/(L_2 C_2 S^2) + L_1/(L_2 C_2 S) + 1 + L_1/L_2$ $+ L_1 C_1/L_2 C_2 + L_1 C_1 S^2$	$2.4S^{-2} + 2.9 + .8S^2$
$H(\bar{L}_1)$	$1 + 1/(L_2 C_2 S^2)$	$1 + 2.4S^{-2}$
$H(\bar{L}_2, \bar{j})$	$1 + L_1 C_1 S^2$	$1 + .8S^2$
$H(\bar{L}_2, j')$	$L_1 S$	$.66S$

## Example 2

Example 2 shows a two-stage amplifier (Figure 22-5A) and the sensitivity of the voltage gain to several of the elements. Figure 22-5B shows the coded equivalent circuit, and Table 22-6 shows the problem statement for the amplifier. Table 22-7 shows the T, V, and W matrices from which the actual flowgraph (Figure 22-5C) is constructed.

Table 22-8 shows the flowgraph evaluation, while Table 22-9 shows the variables necessary for the evaluation of the sensitivity functions. The sensitivity of the voltage gain to  $B_1$  is  $H(B_1)/H(\bar{j}) = .111 E + 2/.111 E + 2$ , or 1. The sensitivity of the voltage gain to  $R_g$  is  $.110 E + 2/.111 E + 2$ , or approximately 1. In determining the sensitivity of the gain to  $R_2$ , according to Equation 2, we have a case where  $H(\bar{R}_2, j')$  is not zero, and hence the sensitivity is equal to  $.110 E + 2/.111 E + 2 - (-.100 E + 5/-.100 E + 5) = 0$ .

Table 22-6

Problem Statement by Two-Stage Amplifier

A	B	C	D	E	F	G	H	Numerical
1	2	0	9	1	0	0	1	.100 E+1
1	2	0	2	2	0	1	0	.100 E-2
1	2	0	3	3	0	1	0	.100 E-1
3	2	1	3	4	0	1	0	.100 E+2
3	2	1	5	5	0	0	0	.100 E+4
3	2	0	6	6	0	1	0	.100 E-1
4	2	1	6	7	0	1	0	.100 E+2
4	2	0	8	8	0	1	0	.100 E-2
4	2	1	9	9	0	0	0	.100 E+2

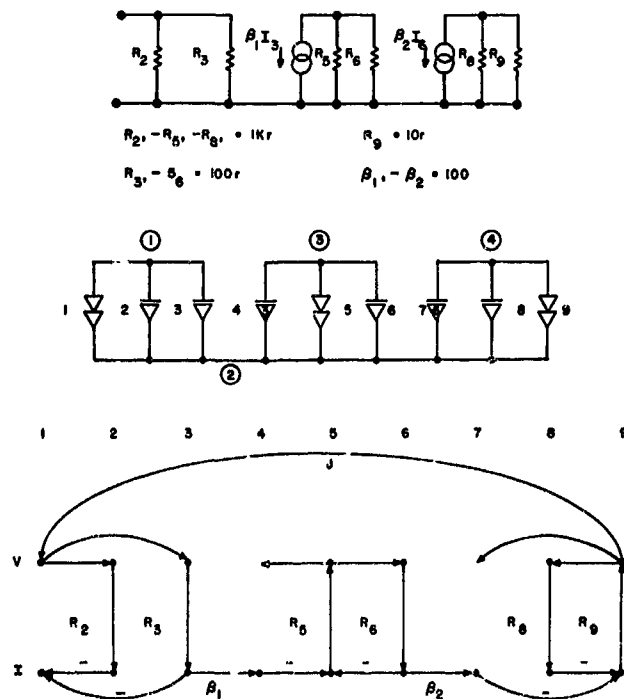


Figure 22-5—Two-stage amplifier --  
A.—Electrical circuit  
B.—Coded circuit  
C.—Flowgraph.



Table 22-7

T-V-W Matrices for Two-Stage Amplifier

T	1	2	3	4	5	6	7	8	9	V	1	2	3	4	5	6	7	8	9	W	1	2	3	4	5	6	7	8	9
1										1		+	+							1									
2		Y								2										2	-								
3			Y	I						3										3	-			I					
4										4										4				-					
5					Z					5			+		+					5									
6						Y	I			6										6				-		I			
7										7										7								-	
8								Y		8										8								-	
9	E								Z	9	E							+	+	9									

Table 22-8

Flowgraph Evaluation for Two-Stage Amplifier

Loops	Transmittances	J	$\pm$	Numerical
L(i)	1 2 3 4 5 6 7 8 9			
1	1 3 4 5 6 7 9	1	-	.100 E+5
2	5 6	0	+	.100 E+2
3	8 9	0	+	.100 E-1
4	5 6 8 9	0	+	.100 E+0

Table 22-9

Necessary Data for Sensitivity Evaluation -- Example 2

$H(j')$	$-B_1 B_2 G_3 R_5 G_6 R_9$	$-.100 E+5$
$H(\bar{j})$	$1 + R_5 G_6 + G_8 R_9 + R_5 G_6 G_8 R_9$	$.111 E+2$
$H(\bar{B}_1)$	$1 + R_5 G_6 + G_8 R_9 + R_5 G_6 G_8 R_9$	$.111 E+2$
$H(\bar{R}_9)$	$1 + R_5 G_6$	$.110 E+2$
$H(\bar{R}_2, \bar{j})$	$1 + R_5 G_6$	$.110 E+2$
$H(\bar{R}_2, j')$	$-B_1 B_2 G_3 R_5 G_6 R_9$	$-.100 E+5$

Table 22-10

## Problem Statement for Tuned Amplifier

A	B	C	D	E	F	G	H	Numerical Value
2	1	0	1	1	0	1	0	.400 E-1
3	1	1	1	2	0	1	0	.100 E+3
1	4	1	3	3	0	0	0	.250 E+2
3	4	0	4	4	1	1	0	.100 E-6
1	5	1	5	5	-1	0	0	.100 E+8
3	5	1	6	6	0	0	0	.100 E+13
2	1	0	6	7	0	0	1	.100 E+1

## Example 3

Example 3 shows a single-stage, tuned-amplifier (Figure 22-6A). The coded circuit (Figure 22-6B) and the problem statement matrices (Tables 22-10 and 22-11) for the flowgraph construction (Figure 22-6C) are displayed. Table 22-12 shows the flowgraph evaluation, and Table 22-13 shows the variables necessary for the sensitivity evaluations. The sensitivity to  $B$  is  $(2 - 1.00E5 \text{ S})/(2. - 1.00E5 \text{ S})$ , or 1. The sensitivity to  $R_L$  is  $(2. - 1.E5 \text{ S})/(2. + .25 \text{ E-5 s})$ , or approximately 10 at high

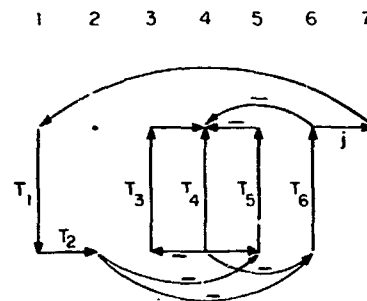
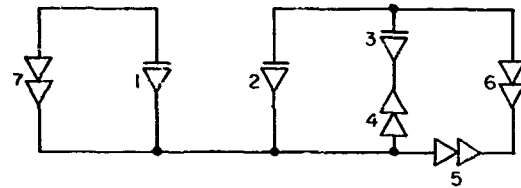
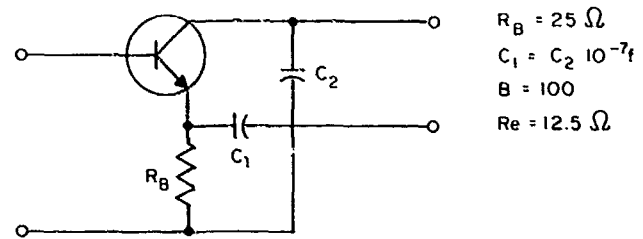


Figure 22-6—Tuned amplifier — A.—Electrical circuit  
B.—Coded circuit  
C.—Flowgraph.

Table 22-11

## V-W-T Matrices for Tuned Amplifier

V	1	2	3	4	5	6	7	W	1	2	3	4	5	6	7	T	1	2	3	4	5	6	7
1																-	Y	I					
2													+	-									
3				+															Z				
4											-	+							Y				
5		-		-																	Z		
6		+		+																		Z	E
7	+																						

Table 22-12

Flowgraph Evaluation for Tuned Amplifier

Loops	Transmittances	J	S	$\pm$	Numerical
L(i)	1 2 3 4 5 6 7				
1	1 2 4 5 6 7	1	0	-	.800E+12
2	1 2 6 7	1	0	+	.800E+12
3	3 4	0	1	+	.250E-5
4	4 5	0	0	+	.100E+1
5	4 6	0	1	-	.100E+6
6	1 2 3 4 6 7	1	1	+	.200E+7
7	1 2 4 5 6 7	1	0	+	.800E12

Table 22-13

Necessary Data for Sensitivity Evaluation - Example 3

$H(j')$	$G_e BR_b C_1 R_L S + G_e BR_L C_1 S/C_2 S$	8.00 E11 +2.00 E6 S
$H(\bar{j})$	$1.00 + C_1/C_1 + R_b C_1 S - R_L C_1 S$	2.00 -1.00 E5 S
$H(\bar{B})$	$1.00 + C_1/C_2 + R_b C_1 S - R_L C_1 S$	2.00 -1.00 E5 S
$H(\bar{R}_L)$	$1.00 + C_1/C_2 + R_b C_1 S$	2.00 +.250 E-5 S

Table 22-14

Problem Statement for Desensitized Amplifier

A	B	C	D	E	F	G	H	Numerical Value
1	2	0	1	1	0	1	0	.100E+5
3	2	0	2	2	0	1	0	.400E-1
3	2	0	3	3	1	1	0	.100E-8
1	3	1	4	4	0	0	0	.125E+2
4	3	1	4	5	0	1	0	.800E+1
5	1	1	6	6	0	0	0	.100E+5
5	4	1	7	7	0	0	0	.200E+3
1	2	0	7	8	0	0	1	.100E+1

frequencies, showing that the load of the tuned amplifier greatly affects the voltage gain of the circuit.

#### Example 4

The fourth example displays a single-stage, transistor amplifier that has been desensitized to changes in  $G_m$ . Figure 22-7A shows the actual circuit, while Figure 22-7B shows the coded equivalent circuit. Tables 22-14 and 22-15 show the problem statement and matrices necessary for the flowgraph (Figure 22-7C). Table 22-16 displays the flowgraph evaluation, while Table 22-17

Table 22-15

## V-W-T Matrices for Desensitized Amplifier

V	1	2	3	4	5	6	7	8	W	1	2	3	4	5	6	7	8	T	1	2	3	4	5	6	7	8
1																	-	Y								
2												+					-		Y							
3												+					-			Y						
4		-	-		+																Z	Y				
5													-		-	-										
6						+																	Z			
7						+		E																	Z	E
8	+	+	+																							

Table 22-16

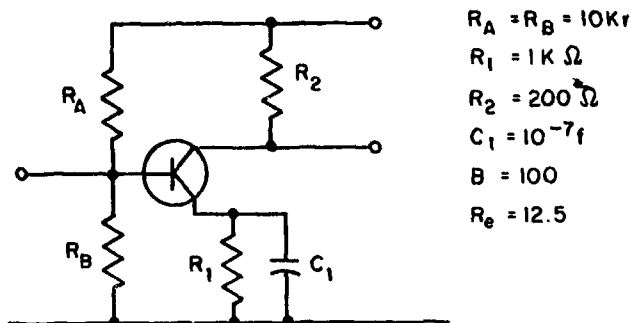
## Flowgraph Evaluation for Desensitized Amplifier

Loops	Transmittances	J	S	$\pm$	Numerical
L(i)	1 2 3 4 5 6 7 8				
1	2 4	0	0	+	.500E+0
2	2 4 5 7 8	1	0	-	.800E+3
3	3 4	0	1	+	.125E+9
4	3 4 5 7 8	1	1	-	.206E12
5	4 5	0	0	-	.100E+3

Table 22-17

## Necessary Data for Sensitivity Evaluation - Example 4

$H(j')$	$-G_1 R_e G_m R_L - C_1 R_e G_m R_L S$	$-.800E+3 \quad -.206E12 S$
$H(\bar{j})$	$1.00 + G_1 R_e - R_e G_m + C_1 R_e S$	$-98.5 \quad +.125E+9 S$
$H(\bar{R}_2)$	$1.00 + G_1 R_e - R_e G_m + C_1 R_e S$	$-98.5 \quad +.125E+9 S$
$H(\bar{G}_m)$	$1.00 + G_1 R_e + C_1 R_e S$	$1.50 \quad +.125E+9 S$



$R_A = R_B = 10K\Omega$   
 $R_1 = 1K\Omega$   
 $R_2 = 200\Omega$   
 $C_1 = 10^{-7}f$   
 $\beta = 100$   
 $R_e = 12.5$

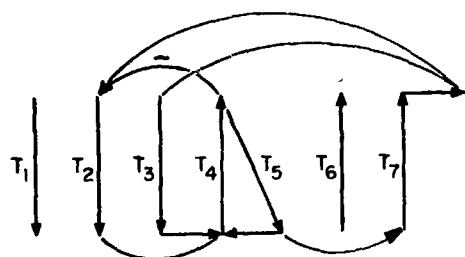
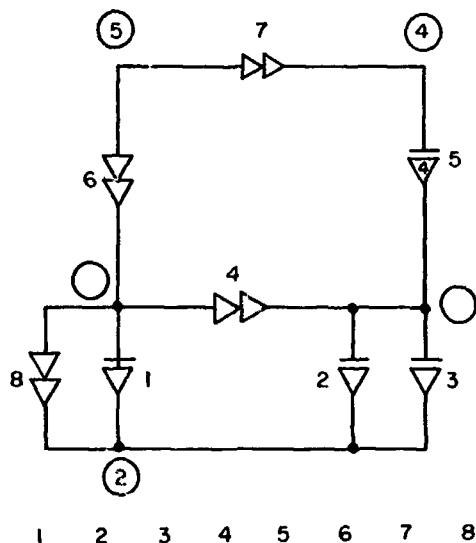


Figure 22-7—Desensitized amplifier —  
 A.—Electrical circuit  
 B.—Coded circuit  
 C.—Flowgraph.

$7S^{-2} + 3.96)/(.201E^{-7}S^{-2} + 3.98 + .199E^{-7}S^2)$ ; thus, the sensitivity to  $L_5$  is extremely frequency-dependent.

## CONCLUSION

A wide range of programs compatible with the present sensitivity analysis is now in use:

1. Flowgraph construction (Reference 19),

Table 22-18

Problem Statement for Band-Pass Filter

A	B	C	D	E	F	G	H	Numerical Value
2	3	0	1	1	-1	1	0	.100E+1
3	1	1	2	2	-1	0	0	.101E+7
3	4	0	3	3	1	1	0	.100E-7
4	1	0	4	4	1	1	0	.980E-6
4	1	1	5	5	1	0	0	.100E+1
4	5	0	6	6	1	1	0	.100E+7
5	1	1	7	7	-1	0	0	.101E+7
5	6	1	8	8	1	0	0	.100E+1
2	1	0	5	9	0	0	1	.100E+1

shows that the sensitivity of the gain  $P_2$  from Equation 2 is  $(-98.5 + .125E + 9)/(-98.5 + .125E + 9S)$ . Thus, at D.C., the gain of the amplifier is relatively insensitive to changes in  $G_m$ .

## Example 5

The last example displays a bandpass amplifier (Figure 22-8A). Figure 22-8B shows the coded equivalent circuit; Tables 22-18 and 22-19 show the problem statement and the matrices for the construction of the flowgraph (Figure 22-8C). Table 22-20 shows the flowgraph evaluation; Table 22-21 shows that the sensitivity of the voltage gain to  $L_5$  is  $(.201E^{-7}S^{-2} + 3.96)/(.201E^{-7}S^{-2} + 3.98 + .199E^{-7}S^2)$ ; thus, the sensitivity to  $L_5$  is extremely frequency-dependent.

Table 22-19

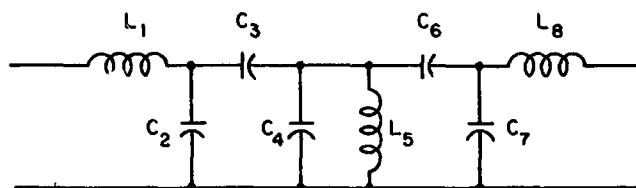
V-W-T Matrices for Band-Pass Filter

V	1	2	3	4	5	6	7	8	9	W	1	2	3	4	5	6	7	8	9	T	1	2	3	4	5	6	7	8	9
1												+							-		Y								
2	-		+																			Z							
3												-		+									Y						
4														-										Y					
5			-	+		+																		Z					E
6														+		-									Y				
7																										Z			
8																											Y		
9	+																												

Table 22-20

Flowgraph Evaluation for Band-Pass Filter

Loops	Transmittances	J	S	$\pm$	Numerical
L(i)	1 2 3 4 5 6 7 8 9				
1	1 2	-0	-2	+	.101E+7
2	1 2 3 5 9	1	0	-	.101E-1
3	2 3	0	0	+	.990E+0
4	3 5	0	2	+	.100E-7
5	4 5	0	2	+	.980E-6
6	5 6	0	2	+	.100E+7
7	6 7	0	0	+	.990E+0
8	1 2 3 5	0	0	+	.101E-1
9	1 2 4 5	0	0	+	.990E+0
10	1 2 5 6	0	0	+	.101E-1
11	1 2 6 7	0	-2	+	.100E+7
12	1 2 3 5 6 7 9	1	0	-	.100E-1
13	2 3 4 5	0	2	+	.970E-6
14	2 3 5 6	0	2	+	.990E+6
15	2 3 6 7	0	0	+	.980E+0
16	3 5 6 7	0	2	+	.990E-8
17	4 5 6 7	0	2	+	.970E-6
18	1 2 3 5 6 7	0	0	+	.100E-1
19	1 2 4 5 6 7	0	0	+	.980E+0
20	2 3 4 5 6 7	0	2	+	.960E-6



$$\begin{aligned}
 L_1 &= L_5 = L_8 = 1\text{h} \\
 C_2 &= C_7 = .99\ \mu\text{f} \\
 C_3 &= C_6 = .01\ \mu\text{f} \\
 C_4 &= .98\ \mu\text{f}
 \end{aligned}$$

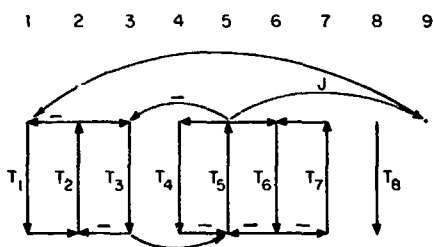
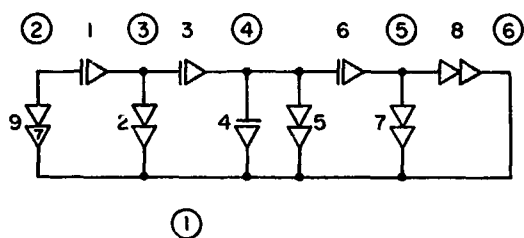


Figure 22-8—Band-pass filter — A.—Electrical circuit  
B.—Coded circuit  
C.—Flowgraph.

2. Transfer function, symbolic (Reference 20),
3. Transfer function, numerical (Reference 21),
4. Frequency analysis, numerical and display (Reference 22),
5. Monte Carlo analysis (Reference 23),
6. Transient response via state variables (Reference 24),
7. Stability analysis (Reference 25),
8. Model optimization (Reference 26),
9. Acoustic transducers (Reference 27),
10. Electromechanical transducers (Reference 28).

There are plans to undertake programs available to industry through the NASA Technology Utilization project, COSMIC, administered by NASA/MSFC.

Table 22-21

Necessary Data for Sensitivity Evaluation — Example 5

$H(j\omega)$	$C_6/C_2 + C_3 L_5/(L_1 C_2)$	.980
$H(\bar{j})$	$1/(L_1 C_2 S^2) + C_6/(L_1 C_2 C_7 S^2) + (C_3 L_5 + C_4 L_5$ $+ L_5 C_6)/(L_1 C_2) + C_3 C_6/(C_2 C_7) + C_3 L_5 C_6/L_1 C_2 C_7$ $+ C_4 L_5 C_6/L_1 C_2 C_7 + 1.00 + (C_3 L_5 + C_4 L_5 + L_5 C_6$ $+ C_3 C_4 L_5/C_2 + C_3 C_4 L_5/C_2 + C_6 C_3 L_5/C_2 + C_6 C_3 L_5/C_7$ $+ C_3 C_4 L_5 C_6/(C_2 C_7) S^2$	$.201\text{E}7\ S^{-2} + 3.98$ $.199\text{E}7\ S^2$
$H(\bar{L}_5)$	$1/(L_1 C_2 S^2) + C_3/C_2 + C_6/C_7 + C_6/(C_7 L_1 C_2 S^2)$ $+ C_3 C_6/(C_2 C_7) + 1.00$	$.201\text{E}7\ S^{-2} + 3.96$

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**1 N67 - 31585**

**23. DESENSITIZING OF MICROCIRCUITS TO VARIATIONS IN TEMPERATURE AND PRODUCTION SPREAD. PHASE IV -- TOLERANCE IN PERFORMANCE CRITERIA DUE TO PRODUCTION SPREAD OF PARAMETERS**

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A computer-program for tolerance analysis is established, which uses as input data:

1. The topology of the equivalent circuit.
2. Statistical distribution of each circuit parameter.
3. Desired performance criteria and desired sampling frequencies.

The program obtains first the sensitivity matrix for the network. Next, the sensitivity matrix is weighed in terms of the statistical distribution of each circuit parameter. The tolerance of the specified performance parameters of the circuit is then evaluated as a quadratic error due to the deviations by the weighed sensitivity matrix. The program provides:

1. Tolerance in performance criteria at specified frequencies.
2. Identification of components which most heavily contribute to fluctuations in performance.
3. A format for desirable specifications of component tolerances, which is essential to computer-oriented analysis.

Examples of increasing complexity serve to demonstrate that the technique can be effectively used by reliability engineers without specialized knowledge in circuit design.

## INTRODUCTION

An "in-house" NASA/ERC research task was completed, as part of a long-range effort to establish design procedures for microcircuits in which the sensitivity of performance parameters to temperature variations is minimized. Representative examples from design practice, one of which is stated in Table 23-1, were selected. From these was developed the following step-by-step procedure for design evaluation:

1. Selection of the equivalent circuit for computer-aided analysis, and coding of equivalent circuit for data processing.
2. Development of computer-oriented sensitivity criteria.
3. Determination of optimum desensitized design configurations.
4. Evaluation of tolerance in performance criteria due to production spread of parameters.
5. Comparison of performance of fabricated circuits with computer-predicted design specifications.

The tolerance evaluation, Phase (IV), is based upon the sensitivity criteria established in Phase (III).

## PROCEDURE

A previously-developed program (Reference 1) obtains the sensitivity function

$$S_A^B = - S(A)/S(B),$$

where

$$S(A) = a_0 + a_1 s^1 + \dots + a_n s^n = \sum_{k=1}^n a_k s^k$$

is a polynomial dependent on the circuit parameters, A, and

Table 23-1

Problem Statement for Transistor Circuit of Example One

A	B	C	D	E	F	G	H	Element Value
1	2	0	8	1	0	0	1	.100E+1
2	1	0	2	2	0	1	0	.025E-3
2	1	0	3	3	0	1	0	.020E-3
2	3	0	4	4	0	1	0	.100E+0
3	1	1	5	5	0	0	0	.100E+4
3	1	0	6	6	1	1	0	.100E-5
4	3	1	4	7	0	1	0	.100E+3
4	1	1	8	8	0	0	0	.100E+4

$$S(B) = b_0 + b_1 s^1 + \dots + b_n s^m = \sum_{k=1}^m b_k s^k$$

is a polynomial dependent on performance criterion B.

The computer subroutine discussed in Reference 1 is extended for use in this tolerance analysis. To illustrate, Figure 2 (Reference 1) shows the small signal ac equivalent circuit of the transistor circuit given in Figure 1 (Reference 1). Figure 3 (Reference 1) presents the "dichotomized" equivalent circuit coded for voltage gain, while Table 23-1 displays this as coded input to the computer program. The signal flowgraph of Figure 4 (Reference 1) is drawn from the computer output shown in Table 23-2. In Table 23-3, the coefficients  $a_k$  and  $b_k$  are evaluated, and the absolute value of sensitivity,  $|S(A)/S(B)|$ , is calculated at critical frequencies  $s_k$ , which include the break-frequencies of  $S(A)$  and  $S(B)$ . Next, the weighted sensitivity,  $T(B, A)$ , is computed in the parameter A, by multiplying the percentage spread,  $\frac{\Delta A}{A}$ , by the absolute value of sensitivity:

$$T(B, A) = \frac{\Delta A}{A} \left| \frac{S(A)}{S(B)} \right|.$$

This weighted sensitivity is listed in Tables 23-3 and 23-4.

The tolerance  $T^2(B)$  is then the sum over all N components,

$$T^2(B) = \sum_{A=1}^N T^2(B, A).$$

Table 23-2

V-W-T Matrices for Example 1

V	1	2	3	4	5	6	7	8	W	1	2	3	4	5	6	7	8	T	1	2	3	4	5	6	7	8
1		-	-	-					1									1								
2									2	+								2		Y						
3									3	+								3			Y					
4									4	+				+				4				Y				I
5				-		+	+		5									5					Z			
6									6					-				6						Y		
7									7								-	7								
8							-		8									8	E							Z

Table 23-3

Data for Reliability Calculation of Example 1

$$S_A^B = \frac{a_0 + a_1 s + \dots + a_n s^n}{b_0 + b_1 s + \dots + b_m s^m}$$

Expression or Equation	$\frac{V_G}{S_{R_N}}$	$\frac{V_G}{S_{R_E}}$	$\frac{V_G}{S_{C_E}}$	$\frac{V_G}{S_{\beta}}$	$\frac{V_G}{S_{R_L}}$	$\frac{V_G}{S_{R_1}}$	$\frac{V_G}{S_{R_2}}$
$a_0$	.100E+5	.101E+9	-	.101E+9	.100E+1	.000	.000
$a_1$	.200E+2	-	.101E+6	.102E+4	-	-	-
$a_2$	.100E-1	-	-	.100E-1	-	-	-
$b_0$	.101E+9	.101E+9	.101E+9	.100E+9	.100E+1	.100E+1	.100E+1
$b_1$	.101E+6	.101E+6	.101E+6	.101E+6	-	-	-
$b_2$	.101E-1	.101E-1	.101E-1	.101E-1	-	-	-
$ S(j\omega) $							
$\omega_0 = .000$	.100E-3	.100E+1	.000	.100E-1	.100E+1	.000	.000
$\omega_1 = .100E+4$	.200E-3	.707E-0	.707E-0	.100E-1	.100E+1	.000	.000
$\omega_2 = .100E+6$	.100E-1	.100E-1	.100E+1	.141E-1	.100E+1	.000	.000
$\omega_3 = .100E+7$	.100E+0	.100E-2	.100E+1	.100E+0	.100E+1	.000	.000
$\omega_\infty = \infty$	.100E+1	.000	.000	.100E+1	.100E+1	.000	.000
$\Delta P/P$	.01	.01	.01	.20	.01	.01	.01
$\omega_0 = .000$	.100E-5	.100E-1	.000	.200E-2	.100E-1	.000	.000
$\omega_1 = .100E+4$	.200E-5	.707E-2	.707E-2	.200E-2	.100E-1	.000	.000
$\omega_2 = .100E+6$	.100E-3	.100E-3	.100E-1	.282E-2	.100E-1	.000	.000
$\omega_3 = .100E+7$	.100E-2	.100E-4	.100E-1	.200E-1	.100E-1	.000	.000
$\omega_\infty = \infty$	.100E-1	.000	.000	.200E+0	.100E-1	.000	.000

These are listed in Table 23-5. The values refer to the  $\sigma = 1$  limits. If the component distribution is given as a matrix for various values of the standard deviation  $\sigma$ , a complete distribution of the performance criteria is obtained. See References 2 through 4 for additional information.

Table 23-4

Quantized Reliability Rating for Components of  
Example One

Equation	$R_N$	$R_E$	$C_E$	$\beta$	$R_L$	$R_1$	$R_2$
$\omega_0 = .000$	C	A	O	B	A	O	O
$\omega_1 = .100E+4$	C	A	A	B	A	O	O
$\omega_2 = .100E+6$	C	C	A	B	A	O	O
$\omega_3 = .100E+7$	B	C	A	A	A	O	O
$\omega_\infty = \infty$	B	O	O	A	B	O	O

A - Major source of uncertainty

B - Contributes less than 30 percent to uncertainty

C - Negligible contribution

O - Does not affect tolerance

flowgraph in Figure 7 (Reference 1) has been drawn from the computer output of Table 23-7. The data for reliability calculation, quantized reliability rating, and calculation of the variance in the input impedance are given in Tables 23-7 through 23-10 which proceed on the same order as previously cited Example 1.

## WORK IN PROGRESS

The following procedures are still in progress:

Table 23-5

Calculation of Variance in Voltage Gain for  
Example One

$\omega(i)$	radians/second	Type "A"	$T(\%)$
0	.000	$R_E, R_L$	1.41%
1	.100E+4	$R_E, C_E, R_L$	1.41%
2	.100E+6	$C_E, R_L$	1.44%
3	.100E+7	$C_E, \beta, R_2$	2.45%
$\infty$	$\infty$	$\beta$	20%

## WORST CASE DESIGN TECHNIQUES

The foregoing techniques can be extended with minimum modification to:

1. QPD: Quantized Probability Design (References 5, 6).
2. AWC: Absolute Worst Case Design (Reference 7).
3. TWC: Taylor Worst Case Design (Reference 8).

As an illustrative example, an application to QPD is shown in Tables 23-3, 23-4, and 23-5. A further illustration of the technique is given in Example 2 (Reference 1) which includes Figures 5 and 6 (Reference 1) and Table 23-6. The

1. Obtaining a data bank for circuit components for an appropriate range of sigma limits.
2. Ascertaining experimentally the validity of using the absolute value of sensitivity and of neglecting phase in the complex sensitivity calculations.
3. Ascertaining experimentally the validity of the quadratic error criterion and the feasibility of extending the technique to skew distributions.

4. Extending the technique to temperature induced fluctuations and verifying its appropriateness experimentally.

The effectiveness of this approach based on dichotomous techniques, has been compared with programs based on matrix techniques, such as ECAP and NET -2 (References 9 through 12).

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Table 23-6

Problem Statement for Passive R-C Circuit of Example Two

A	B	C	D	E	F	G	H	Element Value
2	3	1	1	1	0	0	0	$Z_1 = 100E+5$
3	4	0	2	2	0	1	0	$Y_2 = 500E-4$
4	5	0	3	3	0	1	0	$Y_3 = 100E-3$
5	1	1	4	4	0	0	0	$Z_4 = 300E+5$
4	1	1	5	5	-1	0	0	$Z_5 = 100E+7$
3	5	0	6	6	1	1	0	$Z_6 = 100E-5$
1	2	1	7	7	0	0	1	$E_7 = 100E+1$

Table 23-7

V-W-T Matrices for Example Two

V	1	2	3	4	5	6	7	W	1	2	3	4	5	6	7	T	1	2	3	4	5	6	7
1								1	-					-		1	Z						
2	+				+		+	2								2		Y					
3				+	-			3								3			3				
4								4		-				-		4			Z				
5								5	-	+						5				Z			
6	+			+			+	6								6					Y		
7								7	+					+		7							Z



Table 23-8

Data for Reliability Calculation of Example Two

$$S_A^B = \frac{a_0 + a_1 s + \dots + a_n s^n}{b_0 + b_1 s + \dots + b_m s^m}$$

Expression or Equation	$\frac{Z_i}{S R_1}$	$\frac{Z_i}{S R_2}$	$\frac{Z_i}{S R_3}$	$\frac{Z_i}{S R_4}$	$\frac{Z_i}{S C_5}$	$\frac{Z_i}{S C_6}$
$a_0$	.250E+0	.500E+0	.250E+0	.750E+0	.000	.000
$a_1$	.350E-1	.400E-1	.000	.450E-1	.400E-1	.225E-1
$a_2$	.178E-2	.110E-2	-.300E-3	.975E-3	.180E-2	.120E-2
$a_3$	.385E-4	.120E-4	-.133E-14	.900E-5	.203E-4	.160E-4
$a_4$	.303E-6	.450E-7	.900E-7	.300E-7	.000	.000
$b_0$	.175E+1	.175E+1	.175E+1	.175E+1	.175E+1	.175E+1
$b_1$	.183E+0	.183E+0	.183E+0	.183E+0	.183E+0	.183E+0
$b_2$	.655E-2	.655E-2	.655E-2	.655E-2	.655E-2	.655E-2
$b_3$	.958E-4	.958E-4	.958E-4	.958E-4	.958E-4	.958E-4
$b_4$	.468E-6	.468E-6	.468E-6	.468E-6	.468E-6	.468E-6
$ S(j\omega) $						
$\omega_0 = .000$	.143E+0	.286E+0	.143E+0	.429E+0	.000	.000
$\omega_1 = .100E+4$	.644E+0	.966E-1	.190E+0	.644E-1	.431E-1	.340E-1
$\omega_2 = .100E+6$	.647E+0	.961E-1	.192E+0	.641E-1	.433E-3	.342E-3
$\omega_3 = .100E+7$	.647E+0	.961E-1	.192E+0	.641E-1	.433E-3	.342E-3
$\omega_\infty = \infty$	.650E+0	.960E-1	.192E+0	.640E-1	.000	.000
$\Delta P/P$	.01	.01	.01	.01	.05	.05
$\omega_0 = .000$	.143E-2	.286E-2	.143E-2	.429E-2	.000	.000
$\omega_1 = .100E+4$	.644E-2	.966E-3	.190E-2	.644E-3	.215E-2	.169E-2
$\omega_2 = .100E+6$	.647E-2	.961E-3	.192E-2	.641E-3	.216E-4	.170E-4
$\omega_3 = .100E+7$	.647E-2	.961E-3	.192E-2	.641E-3	.216E-5	.170E-5
$\omega_\infty = \infty$	.650E-2	.960E-3	.192E-2	.640E-3	.000	.000

Table 23-9

Quantized Reliability Rating for Components of  
Example Two

Quantized Reliability Rating for Components						
Equation	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	R <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
$\omega_0 = .000$	A	A	A	A	O	O
$\omega_1 = .100E+4$	A	B	A	B	B	B
$\omega_2 = .100E+6$	A	B	A	B	C	C
$\omega_3 = .100E+7$	A	B	A	B	C	C
$\omega_\infty = \infty$	A	B	A	B	O	O

A - Major Source of Uncertainty

B - Contributes less than 30 percent to Uncertainty

C - Negligible Contribution

O - Does not affect Tolerance

Table 23-10

Calculation of Variance in Input Impedance for  
Example Two

$\omega$ (i)	radians/second	Type "A"	T(Z <sub>i</sub> )
0	.000	R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , R <sub>4</sub>	.55%
1	.100E+4	R <sub>1</sub> , R <sub>3</sub>	.73%
2	.100E+6	R <sub>1</sub> , R <sub>3</sub>	.68%
3	.100E+7	R <sub>1</sub> , R <sub>3</sub>	.68%
$\infty$	$\infty$	R <sub>1</sub> , R <sub>3</sub>	.65%

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**NO 7-51586**

**24. ADAPTATION OF MODELS FOR MINORITY-CARRIER DEVICES  
TO INTEGRATED CIRCUITS**

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Progress is reported on the initial phase of a continuing NASA/ERC in-house research effort to examine alternative models of minority-carrier devices for their usefulness in computer-aided design evaluation of integrated circuits. The minority-carrier parameters, often referred to as the Linvill diffusance model, are investigated with a view to extending this approach to represent networks containing microcircuit elements. This model is to be compared with the conventional model based on networks containing controlled sources. Corresponding design specifications such as frequency response and sensitivity analysis, are then to be compared, so that the region of validity and the limitation of each model may be identified. Guidelines are to be developed for the explicit formulation of circuit design problems in terms of algorithms upon which the computer programs are based. Discrepancies between experimental and computed results are to be examined.

The dual potential N and P type device, upon which the Linvill Model is based, requires re-examination as an extension of networks with a single type of potential. The strategy selected to accomplish this is the extension of dichotomous algorithms to bi-potential systems. To make this account self-contained, dichotomous techniques will be reviewed, and an outline will be presented describing how dichotomous algorithms may be extended.

**LINVILL MODEL**

**Necessity for Re-evaluation of Network Techniques**

Previous models of circuits based on the Linvill Model appear inaccurate or inadequate (References 1 and 2), for several reasons:

1. The unsubstantiated assumption is made that the complete model can be derived with only a single type of node representing each element, the former corresponding to the excess density of the P and N carrier concentrations (Reference 2).

2. Insufficient justification is given to account for the effect of driftance elements.
3. Evaluation techniques cannot be readily adapted to the present coding of the circuit.

It is desirable that additional qualifications be made.

#### Difficulties in Flowgraph Construction for Bi-potential Systems (Tables 24-1A and 24-1B).

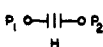
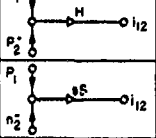
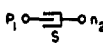
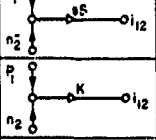
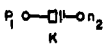
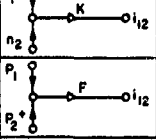
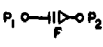
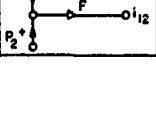
The usefulness of dichotomous techniques such as flowgraphs for networks with a single type of potential suggests the possibility of their extension to networks of the Linvill form. The elements to be considered, with their equations and symbols, are listed in Table 24-1A. The condition will be examined under which dichotomous techniques for passive circuits can be extended to define cut and tie sets of a bi-potential system. Difficulties result in constructing a corresponding flowgraph, because of the inability of Kirchhoff's laws to describe a driftance element. If conventional cuts and ties are used, this element produces an erroneous solution for network functions.

#### Approaches to Modelling Bi-potential Systems

The equivalent graph is drawn as before, except that care must be taken to assign direction corresponding to voltage sources from the N to the P area. All other directions can be arbitrarily selected. The flowgraph is then constructed, with the voltage nodes corresponding to the voltage sources having the excess density (N-P). All other voltage nodes are determined as the sum of the transmittances at a contributive node. If a driftance element is present, it connects either two P-type regions or two N-type regions. In the former case, an additional P node is present and will contribute a value of  $\pm 2P_1$  or  $\pm 2P_2$  depending on the topology of the system. No transmittances terminate at this node. A similar node is present in the case in which the driftance element connects two N-type nodes,  $N_1$  and  $N_2$ . The flowgraph can then be evaluated for the cut and tie sets of the bi-potential system, following the algorithms to be developed. Any driftance nodes are ignored.

Table 24-1A

FLOWGRAPH REPRESENTATIONS FOR LUMPED SEMICONDUCTOR REGIONS

LUMPED PARAMETER	$\longrightarrow i_{12}$	$i_{12}$	TRANSMITTANCE	DEFINITION
DIFFUSANCE		$(P_1 - P_2) H$		$H = \frac{ADq}{w}$
STORANCE		$(P_1 - P_2) S$		$S = \frac{Awd}{2}$
COMBINANCE		$(P_1 - P_2) K$		$K = \frac{ADq\mu^2}{2w}$
DRIFTANCE		$(P_1 + P_2) F$		$F = AqE\mu\phi$

#### The Closed System Approach

To develop a technique for modelling bi-potential circuits, the cut and tie sets of a graph of  $n$  elements of a single type will be developed from the "closed system" point of view. This approach can then be employed to calculate the driving point and sensitivity functions. This method consists of:

1. A coding procedure.

Table 24-1B  
Flowgraph Construction for Bi-Potential Systems

CIRCUIT	DICHOTOMOUS SYSTEM CODING	FLOWGRAPH

2. Computer-oriented algorithms.

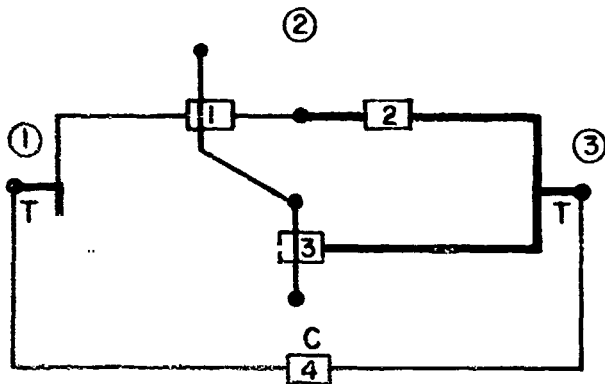
3. A computer program to perform the given operations.

The major effort is a strictly-ruled coding procedure to obtain algorithms for computations. The algorithms are used to develop a computer program. The signs of the cuts and ties are calculated to provide a parity check against coding errors. Most of the existing programs check every possible combination of elements and eliminate the improper ones. The technique to be described avoids this situation. The closed system approach brings to light the duality between cuts and ties and gives evidence of relationships based on the dichotomous procedures.

It is important to note the limitations of the method. The algorithms to be presented here apply only to graphs containing elements of a single type, all of which must be passive. These algorithms will then be extended.

#### Illustrative Example

Given the 3-element graph in Figure 24-1, the cut and tie sets are calculated, using the following procedures:



T: TERMINALS OF OPEN SYSTEM

C: CLOSING ELEMENT

1. The graph is closed and coded (Reference 4); the directed graph of Figure 24-2 is obtained. This graph is described in Table 24-1.
2. Figure 24-3, the flowgraph in coded form, is derived from Table 24-2.

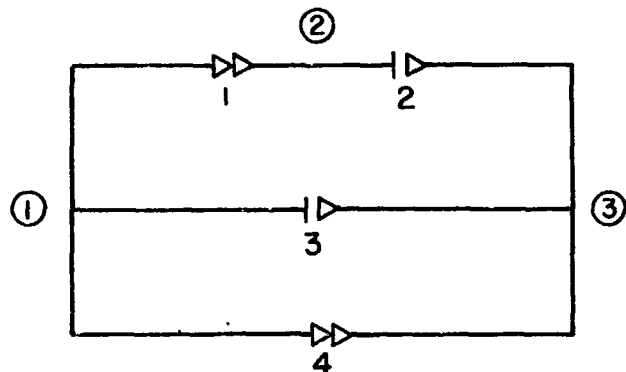


Figure 24-1—Closed system showing cut (1010) and tie (0110).

Figure 24-2—System coding (dichotomous).

3. The loops of the flowgraph are determined and listed in coded form in Table 24-3.
4. The  $K$  and  $\bar{K}$  operators are determined from the coding (Tables 24-4 and 24-5) and are used to transform the loops into the cut set and tie set.

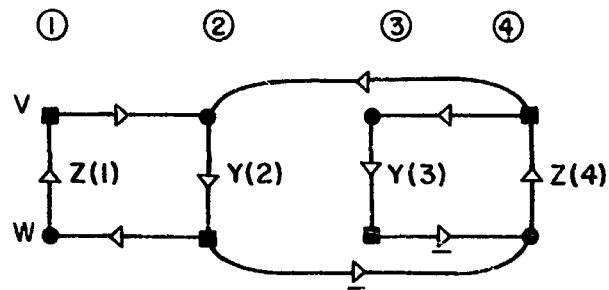


Figure 24-3—Flowgraph of dichotomous presentation of closed system.

# TERMINOLOGY

## Basic Terms and Concepts

1. Elements are topological quantities of a graph. Each element is associated with two vertices, and in some applications is interpreted as an obstruction to flow between them. Elements are numbered sequentially.
2. Vertices are the topologically distinguishable points of a graph. Any two may or may not be connected by an element. They are numbered sequentially.
3. A terminal is a preferred or accessible vertex. At least two terminals are required for an external measurement on the graph.
4. A graph is a sequence of numbered vertices, each of which is connected to at least one other vertex by an element.
5. A directed graph is a graph in which the type and direction of each element is specified.
6. A tie of a graph consists of a minimal sequence of elements which connect every vertex. A tie is also referred to as a tree. The tie set of a graph consists of all possible ties.

Table 24-2

Flowgraph Tables

V	1	2	3	4	W	1	2	3	4	T	1	2	3	4
1		-			1					1	Z			
2					2	+			-	2		Y		
3					3				-	3			Y	
4		+	+		4					4				Z

Table 24-3

Loops, K and  $\bar{K}$  Operators

No.	Loop				Order	Operator
1	0	0	0	0	0	K (0110)
2	1	1	0	0	1	
3	0	1	0	1	1	
4	0	0	1	1	1	$\bar{K}$ (1001)
5	1	1	1	1	2	

7. A cut for a graph with n elements and m vertices, is a sequence of n-(m-1) elements such that a line drawn through those elements will not form a closed path.
8. A closed graph is one in which the cut set and tie set have the same cardinality. This is equivalent to the statement that the cut set and tie set are duals; i.e. for each tie, the remaining elements form a cut, and vice versa. A closed system has no preferred vertices.
9. An open graph is one which is not closed. The addition of an element across two terminals to convert an open graph to a closed one is termed "closing the graph".

10. Dichotomy is defined as a technique determining and distinguishing between two types of elements, which, in a closed graph, are duals.

### Flowgraph Terminology

1. A node describes a topological property of the graph such that each element is associated with two nodes, the v-node and the w-node, each corresponding to the functional dependence of one of the characteristic variables determining the dichotomy.

Table 24-4

Cut Set

Operator	No.	Cut				Sign
K (0110)	1	0	1	1	0	+
	2	1	0	1	0	-
	3	0	0	1	1	-
	4	0	1	0	1	-
	5	1	0	0	1	+

Table 24-5

Tie Set

Operator	No.	Tie				
$\bar{K}$ (1001)	1	1	0	0	1	+
	2	0	1	0	1	-
	3	1	1	0	0	-
	4	1	0	1	0	-
	5	0	1	1	0	+



2. A distributive node describes a sampling procedure in which information is supplied by a single node and distributed to two or more nodes.
3. A contributive node describes a summing process which contributes to a single node — information supplied by two or more nodes.
4. A transmittance corresponds to a functional relationship between nodes and is represented by a directed line connecting a node of origin and a target node.
5. An intraconnection is a transmittance between two nodes of different elements.
6. An interconnection is a transmittance between the  $V$  and  $W$  nodes of an element.
7. A flowgraph is the dichotomous description associated with a graph. The topological properties can be a graphical representation, a matrix form, or a code. Neither graph properties nor the flowgraph properties depend on the type of description, but they are inherent in the physical phenomenon governing connections of vertices by elements.
8. Three dichotomized subgraphs (or partial graphs) can be defined in every flowgraph:
  - a. The  $V$ -graph is a description of that part of the flowgraph related to areas in the graph.
  - b. The  $W$ -graph is a description of that part of the flowgraph concerned with properties related to vertices in the graph.
  - c. The  $T$ -graph is that part of the flowgraph concerned with the dichotomous description of elements, i.e.,  $W = f(V)$  or  $V = f(W)$ .
9. The flowgraph of a closed passive graph contains one contributive and one distributive node for each element, and no other nodes. Since "known" quantities are sampled to obtain "unknown", if  $W = f(V)$ , then  $W$  nodes are distributive, and if  $V = f(W)$ , the  $V$ -nodes are distributive. The opposite follows for contributive nodes from the scrutiny of the summing property (Table 24-6). Transmittances must therefore be one of four possible types, relating  $W$  nodes and  $V$  nodes (Table 24-7).

Table 24-6

W-V Relationship

Constraint	W-nodes	V-nodes
$W=f(V)$	Distributive	Contributive
$V=f(W)$	Contributive	Distributive

10. A closed flowgraph is one in which every node is defined in terms of one or more other nodes. Hence all variables are mutually dependent, and a constraint between transmittances exists. This constraint is called the topology equation.

Table 24-7

Types of Transmittances

Transmittance	Type
W to W	W- transmittance: specifying properties or interrelations
V to V	V- transmittance: relating areaproperties or interrelations
V to W	Y - transmittance: for elements described by $W=f(V)$
W to V	Z- transmittance: for elements described by $V=f(W)$

## Solution Terminology

A loop is a selection of transmittances of a flowgraph such that for all transmittances, the target node of one transmittance coincides with the origin node of the next transmittance.

The order of a loop is defined as the number of sets of interconnected transmittances. A loop of order one is a singly connected set of transmittances and its associated nodes. A loop of order  $n$  is determined by the simultaneous presence of  $n$  disjoint first order loops. This definition includes the zero-order loop, which is present in every flowgraph.

## ALGORITHMS

## Construction of Closed Directed Graph

1. Given a graph with  $n$  elements and  $m$  nodes, apply the dichotomous technique and draw the closed directed graph.
2. To close the graph, add an element across each set of terminals. Choose an arbitrary tie containing this element.
3. In a code  $T$  of length  $n$ , each entry refers to one of  $n$  elements, and consists of positive integers, often binary. For the tree in step 2, consider each of the  $m - 1$  elements ( $j$ ) a Z element ( $v = f(w)$ ,  $D = 0$ ), and draw it " $\triangleright$ ", with arbitrary direction. The remaining  $n - (m - 1)$  elements are drawn " $\triangleright$ " and coded  $D = 1$ ,  $W = f(v)$ , also with arbitrary direction.

## Construction of Flowgraph

For each element  $i$  such that  $T(i) = 1$ , choose a sequence  $\{t_j\}$  of elements with  $T(t_j) = 0$ , such that  $\{i \cup \{t_j\}\}$  is a closed path (surface). Let the direction of  $i = D(i)$ . Moving along the path in the direction  $D(i)$ , for each  $t$ , let

$$V(i, t_j) = \begin{cases} +, & \text{if } D(t_j) = \sim D(i) \\ -, & \text{if } D(t_j) = D(i) \end{cases}$$

Also,  $v(i, i) = 0$ , and  $v(i, j) = 0$  if element  $j$  is not on the path. Finally,  $v(i) = [v(i, 1), v(i, 2), v(i, 3) \dots v(i, n)]$ . For each element  $j$  such that  $T(j) = 0$ , choose a sequence  $\{c_i\}$  of elements with  $T(c_i) = 1$ , such that a line drawn through all elements in  $\{c_i \cup j\}$  forms a circle. Let  $D(j)$  be the direction (inward or outward) of  $j$  with respect to the circle, and for each  $c_i$ , let

$$W(j, c_i) = \begin{cases} +, & \text{if } D(c_i) = -D(j) \\ -, & \text{if } D(c_i) = D(j) \end{cases}$$

Also,  $w(j, j) = 0$ , and  $w(j, i) = 0$  if element  $j$  is not on the circle. Finally,  $w(j) = [w(j, 1), w(j, 2), w(j, 3) \dots w(j, n)]$ .

To write the  $V$ -subgraph, draw an  $n \times n$  matrix and enter  $v(i)$  as the  $i^{\text{th}}$  column. Similarly, the  $W$ -subgraph is composed of an  $n \times n$  matrix with  $w(j)$  as the  $j^{\text{th}}$  column. Because the  $V$  and  $W$  matrices are composed on the basis of the dichotomous procedure and duality of the elements, we have the relationship

$$V = (-W)^*.$$

Consider now the duality of the flowgraph. We now have  $n$  vectors of dimension  $n$ . The expressions  $m - 1$  are  $W$  vectors of  $L = 0$  elements and  $n + 1 - m$  are  $V$  vectors of  $L = 1$  elements. These represent the distributive nodes ( $w$ -distributive and the  $v$  node contributive if  $w(i)$  appears in the above list and vice versa if  $v(i)$  appears). In Table 24-8, the distributive node vectors are listed as row vectors of an  $n \times n$  matrix, and their duals (contributive node vectors) are seen as column vectors. This single representation of the  $V$  and  $W$  matrices allows easy derivation of the interconnections of the flowgraph. They are read from column to row (i.e. the entry  $a_{ij}$  is directed from contributive node  $j$  to distributive node  $i$ ). In Table 24-9, the nodes are again listed, but the directional dependency is the opposite. Since these are the intraconnections, the only entries are

Table 24-8

Interconnections for Flowgraph (Figure 24-3)

Distributive Nodes	Contributive Nodes			
	V(1)	W(2)	W(3)	V(4)
W(1)		+		
V(2)	-			+
V(3)				+
W(4)		-	-	

Table 24-9

Intraconnections for Flowgraph (Figure 24-3)

Distributive Nodes	Contributive Nodes			
	V(1)	W(2)	W(3)	V(4)
W(1)	$Z_1$			
V(2)		$Y_2$		
V(3)			$Y_3$	
W(4)				$Z_4$

Table 24-10  
Summary of Constraints

Constraint	From	To
<u>Interconnections</u>	Distributive	Contributive
<u>Intraconnections</u>	Contributive	Distributive

on the diagonal, and the  $a_{ij}^{\text{th}}$  entry is directed from the distributive node at the left to the contributive node at the right. Table 24-10 is a summary of facts about contributive and distributive nodes.

In drawing the flowgraph, two nodes are constructed for each element, a V-node (corresponding to the loop or surface equations of the directed graph) and a W-node (corresponding to the vertex equation). The intraconnections are

drawn from Table 24-9 (equivalent to Table T of Table 24-2), and finally the directed, signed interconnections are drawn according to Table 24-8 (V and W of Table 24-2).

## EVALUATION OF FLOWGRAPH

The immediate objective is to obtain a complete and accurate list of loops and their orders. Starting at Table T in Table 24-2, examine the entry in the first row, first column. The letter Z indicates that the intraconnective transmittance is directed from W to V. Therefore, examine Table 24-2-V to discover if any interconnective transmittance leaves node V(1). A check of row 1 reveals that it does [Table 24-2 is read by columns, i.e.,  $V_2 = -V_1 + V_4$ ]. The check is continued at row 2 of Table 24-2-W and entry 2 of Table 24-2-T. Continuing in this manner, it is possible to list all first-order loops by writing the nodes through which they pass, in order of travel. It is necessary to list the loops in this manner at first to avoid duplicating loops; i.e., two loops are legal (and differentiable) if they pass through the same nodes in different cyclical order, but they are identifiable if they have identical nodes and order. Furthermore, it is perfectly legal for a loop of order greater than unity to pass through the same nodes as a loop of similar or lower order.

Once the complete list of loops is determined with order, it is convenient to present them in a code, which shall be called L. A code L for a closed directed flowgraph of  $n + 1$  elements is an  $(n + 1)$  dimensional row vector determined as follows: For each loop  $i$ , let

$$\ell(i) = \begin{cases} 1 & \text{if loop } i \text{ passes through node } j, \\ 0 & \text{otherwise,} \end{cases}$$

for  $j = 1, n + 1$ .

Then  $L'(i) = [\ell(i)(1), \ell(i)(2), \ell(i)(3), \dots, \ell(i)(n), \ell(i)(n + 1)]$ , and if loop  $i$  has order  $O_i$ , the sign of  $L(i)$  is defined by  $(-1)^{O_i}$ . Thus the L-code of loop  $i$  is

$$L(i) = (-1)^{O_i} L'(i).$$

In determining the cuts and ties, it is necessary to restrict the calculations to certain loops which are unique with respect to order; i.e., 2 loops  $i$  &  $j$  for which  $L(i) = L(j)$ , but  $\text{sign } L(i) = -\text{sign } L(j)$ , must be eliminated. This is most easily done by eliminating any two loops  $i$  and  $j$  for which  $L_N(i) + L_N(j) = 0$ , where,

$$L_N = (-1)^{0j} (\ell_i(n+1) \times 2^0 + \ell_i(n) \times 2^1 + \dots + \ell_i(2) \times 2^{n-1} + \ell_i(1) \times 2^n),$$

since each  $L$  code is a unique binary number.

The  $K$  operator is an  $n+1$  dimensional row vector defined as  $K = [T(1), T(2), \dots, T(n), T(n+1)]$ . Let  $\bar{0} = 1, \bar{1} = 0$ . Then, if  $T(i) = 0$ , then  $\bar{T}(i) = 1$ ; and if  $T(i) = 1$ , then  $\bar{T}(i) = 0$ .

The  $\bar{K}$  operator is a  $n+1$  dimensional row vector defined as  $\bar{K} = [T(1), \bar{T}(2), \dots, \bar{T}(n), \bar{T}(n+1)]$ . Also,  $\bar{K} = \overline{(K)}$ .

The symbol  $\circ$  refers to a matrix operation. Given a  $n$  dimensional row vector  $V = (v_i)$  and an  $m \times n$  dimensional matrix  $A = (a_{ij})$ ,  $V \circ A = B$ , where  $B = (b_{ij})$ ; element  $b_{ij}$  is determined by the sum (modulo 2) of  $v_j$  and  $a_{ij}$ .  $B$  is an  $m \times n$  matrix. The  $(L)$  matrix is the  $p(n+1)$  matrix in which the rows are the  $p(n+1)$ -dimensional row vectors  $L(i)$ .

The cut set of the closed directed graph (and thus of the closed undirected graph) is given by the  $p(n+1)$  matrix  $C$ , where

$$C = K \circ (L).$$

The cuts are the  $(n+1)$ -dimensional row vectors, and they are in  $L$ -coded form. The tie set of the closed directed graph is given by the  $p(n+1)$  matrix  $T$ , where

$$T = \bar{K} \circ (L).$$

The ties are the  $(n+1)$ -dimensional row vectors, and appear in  $L$ -coded form.

To determine the cut and tie sets of the open graph, it is necessary only to remove those cuts and ties in which a one appears in the  $L$  code under the column associated with the closing element. For this reason, it is most convenient to number the closing element with the highest number on the original graph, for then a simple ordering procedure will place the column corresponding to this element on the right side of the list. It is then easy to choose correctly.

## APPLICATIONS

### Impedance and Admittance

The most obvious application of this procedure is in the determination of impedances and admittances of passive electrical networks. If each element is given a value equivalent to its electrical impedance, the cuts and ties can be used to calculate the impedance of the network. Since the network is closed, it is necessary to eliminate those cuts and ties passing through the closing element. This can be done by the method stated in the section on algorithms. The only other prerequisite is that the closing element have a T code of "0".

The operator  $E_c$  is a transformation of a binary row vector into a product such that if  $R$  is a binary row vector with elements  $r_1, \dots, r_{n+1}$  either 0 or 1,

$$E_c(R) = Z_1^{(r_1)} Z_2^{(r_2)} \dots Z_{n+1}^{(r_{n+1})},$$

where  $Z_i$  is the value of the  $i^{\text{th}}$  element.

Example: if  $L(i) = (01101)$ , then  $E_c(L_i) = 1 \cdot Z_2 \cdot Z_3 \cdot 1 \cdot Z_5 = Z_2 Z_3 Z_5$ .

The operator  $E_t$  is also a transformation of a binary row vector into a product. It is defined as the dual operation of  $E_c$ ; if  $R$  is the previously defined row vector, then

$$E_t(R) = Z_1^{(\overline{r_1})} Z_2^{(\overline{r_2})} \dots Z_{n+1}^{(\overline{r_{n+1}})}$$

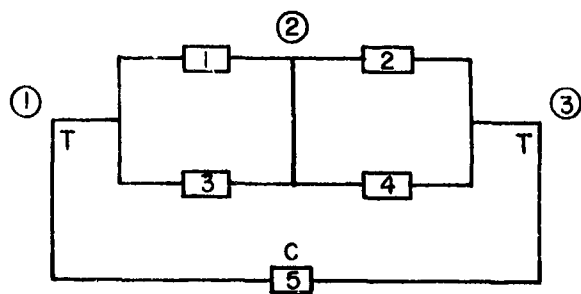
Example: if  $L(i) = (01101)$ , then  $E_t(L_i) = Z_1 \cdot 1 \cdot 1 \cdot Z_4 \cdot 1 = Z_1 Z_4$ .

If the binary code vectors of the cuts are given by  $L_{c_i}$  for  $i = 1, \dots, e$  cuts of the open system, and the coded ties are given by  $L_{t_i}$  for  $i = 1, \dots, f$  ties, then the impedance  $I$  is

$$I = \frac{\sum_{i=1}^e E_c(L_{c_i})}{\sum_{i=1}^f E_t(L_{t_i})}.$$

The admittance is found by taking the inverse of this quotient.

The impedance of a system with  $n$  ports is calculated similarly. The ports are closed with  $n$  elements by connecting the two terminals of each port with a  $T = 0$  element; the cuts and ties of the closed system are then calculated. The input impedance at any point is given by the previous formula, omitting the cuts and ties passing through the closing element of that port. Any port can be considered as being shorted by setting its impedance to 0, or as open by choosing a large enough value (approximately 100 times the value of the second largest element) for its impedance.



T: TERMINALS OF OPEN SYSTEM  
C: CLOSING ELEMENT

Figure 24-4—Closed system.

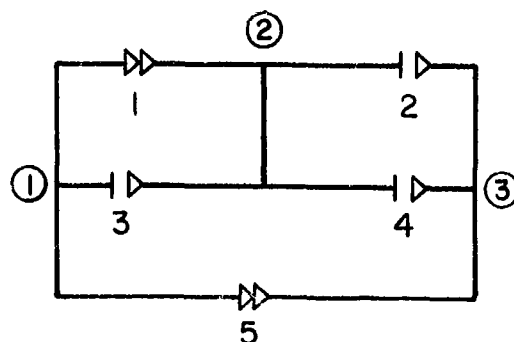


Figure 24-5—System coded dichotomously for flowgraph construction.

#### ADDITIONAL EXAMPLE

Figure 24-4 is the system to be solved for input impedance. Figure 24-5 is the system coded under the dichotomy and ready for flowgraph construction.

Figure 24-6 is the flowgraph of the closed system.

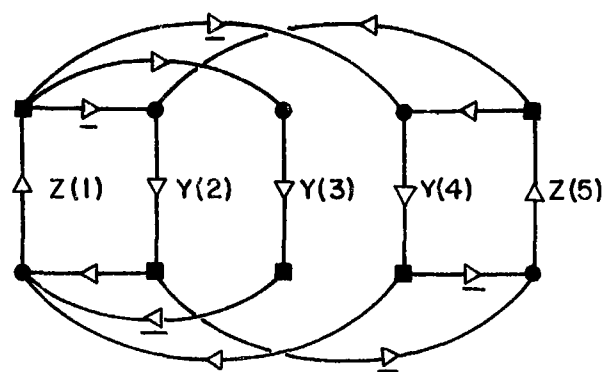


Figure 24-6—Flowgraph of the closed system.

Table 24-11

Description of Coded System

A	B	C	D
1	1	2	0
2	2	3	1
3	1	2	1
4	2	3	1
5	1	3	0
A: element number		C: terminal node	
B: node of origin		D: dichotomous code	

Table 24-12

Flowgraph Subtables

V	1	2	3	4	5	W	1	2	3	4	5	T	1	2	3	4	5
1	-	+	-			1						1	Z				
2						2	+			-		2	Y				
3						3	-					3		Y			
4						4	+			-		4			Y		
5	+		+			5						5				Z	

Table 24-13

## Loops of the Flowgraph

<u>No.</u>	<u>order</u>	<u>sign</u>	<u>loop description</u>	<u>L code</u>
1	0	+	0	0 0 0 0 0
2	1	-	1 2 1	1 1 0 0 0
3	1	-	1 4 5 2 1	1 1 0 1 1
4	1	-	1 3 1	1 0 1 0 0
5	1	-	1 4 1	0 0 1 0
6	1	-	2 5 2	0 1 0 0 1
7	1	-	4 5 4	0 0 0 1 1
8	2	+	1 3 1 - 2 5 2	1 1 1 0 1
9	2	+	1 3 1 - 4 5 4	1 0 1 1 1
10	2	+	1 2 1 - 4 5 4	1 1 0 1 1

Since their sum is zero, loops 3 and 10 are eliminated.

The K operator is ( 0 1 1 1 0 ). The  $\overline{K}$  operator is ( 1 0 0 0 1 )

The computation consists of:  $K \odot$  loops:

$$(0\ 1\ 1\ 1\ 0) \begin{pmatrix} 0\ 0\ 0\ 0\ 0 \\ 1\ 1\ 0\ 0\ 0 \\ 1\ 0\ 1\ 0\ 0 \\ 1\ 0\ 0\ 1\ 0 \\ 0\ 1\ 0\ 0\ 1 \\ 0\ 0\ 0\ 1\ 1 \\ 1\ 1\ 1\ 0\ 1 \\ 1\ 0\ 1\ 1\ 1 \end{pmatrix} = \begin{pmatrix} 0\ 1\ 1\ 1\ 0 \\ 1\ 0\ 1\ 1\ 0 \\ 1\ 1\ 0\ 1\ 0 \\ 1\ 1\ 1\ 0\ 0 \\ 0\ 0\ 1\ 1\ 1 \\ 0\ 1\ 1\ 0\ 1 \\ 1\ 0\ 0\ 1\ 1 \\ 1\ 1\ 0\ 0\ 1 \end{pmatrix}$$

and  $\overline{K} \odot$  loops:

$$(1\ 0\ 0\ 0\ 1) \begin{pmatrix} 0\ 0\ 0\ 0\ 0 \\ 1\ 1\ 0\ 0\ 0 \\ 1\ 0\ 1\ 0\ 0 \\ 1\ 0\ 0\ 1\ 0 \\ 0\ 1\ 0\ 0\ 1 \\ 0\ 0\ 0\ 1\ 1 \\ 1\ 1\ 1\ 0\ 1 \\ 1\ 0\ 1\ 1\ 1 \end{pmatrix} = \begin{pmatrix} 1\ 0\ 0\ 0\ 1 \\ 0\ 1\ 0\ 0\ 1 \\ 0\ 0\ 1\ 0\ 1 \\ 0\ 0\ 0\ 1\ 1 \\ 1\ 1\ 0\ 0\ 0 \\ 1\ 0\ 0\ 1\ 0 \\ 0\ 1\ 1\ 0\ 0 \\ 0\ 0\ 1\ 1\ 0 \end{pmatrix}$$



The row vectors of the resultant matrices are the cuts and ties. The cuts and ties of the open system are those with a 0 in column five.

For the open system:

Cut ( L code )	$E_c(\text{cut})$
0 1 1 1 0	$Z_2 Z_3 Z_4$
1 0 1 1 0	$Z_1 Z_3 Z_4$
1 1 0 1 0	$Z_1 Z_2 Z_4$
1 1 1 0 0	$Z_1 Z_2 Z_3$

Tie ( L code )	$E_t(\text{tie})$
1 1 0 0 0	$Z_1 Z_2$
1 0 0 1 0	$Z_1 Z_4$
0 1 1 0 0	$Z_2 Z_3$
0 0 1 1 0	$Z_3 Z_4$

$$I = \frac{\sum_{i=1}^4 E_c(L_{ci})}{\sum_{i=1}^4 E_t(L_{ti})} = \frac{Z_2 Z_3 Z_4 + Z_1 Z_3 Z_4 + Z_1 Z_2 Z_4 + Z_1 Z_2 Z_3}{Z_1 Z_2 + Z_1 Z_4 + Z_2 Z_3 + Z_3 Z_4}.$$

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**N67-31587**

**25. COMPLEMENTARY MOS-FET NAND GATE MODELLING FOR  
COMPUTER-AIDED TRANSIENT ANALYSIS**

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A nonlinear model of a field effect transistor is developed for performing a computer-aided transient analysis of a complementary MOS-FET, two input NAND gate. The model considers the source-to-substrate-offset voltage effect on the gate. The computer-predicted performance is compared to experimental results. The procedure derived here is applicable to more complex MOS-FET circuits in which variations in source-to-substrate voltage exist.

A device equivalent to the metal-oxide-semiconductor, field effect transistor (MOS-FET) is shown in Figure 25-1. The quantity  $\ell_d$  in this device is defined as follows:

$$= 0 \text{ for } V_g \leq |V_t + V_x|,$$

$$\begin{aligned} \ell_d = & -2P(V_g - V_t - V_x)V_d - \frac{1}{2}V_d^2 \text{ for } V_d \leq |V_g - V_t - V_x|, \\ & -P(V_g - V_t - V_x)^2 \text{ for } V_d \geq |V_g - V_t - V_x|, \end{aligned}$$

where

$V_t$  = threshold voltage,

$$V_x = \frac{C'V_b}{(1 + V_b)^{1/3}},$$

$V_b$  = substrate-to-source voltage, and

$C, P$  = constants.

The voltages given in the above definition are shown in Figure 25-2(a). Figure 25-2(b) shows the substrate-to-source voltage effect on the gating action of the MOS transistor. The equation describing  $V_x$  has been shown by RCA-Somerville to agree with experimental curves.

Using two N-type MOS-FET's, a NAND gate is formed (Figure 25-3). It can be seen that only the uppermost N-type MOS-FET exhibits the substrate effect, i.e., variation in source-to-substrate voltage. Substituting the device model of the MOS-FET (Figure 25-1) into the NAND gate (Figure 25-3) and adding the four stray circuit capacitances results in a general circuit model of the NAND gate (Figure 25-4(a)).

This circuit is redrawn in a symmetrical form, with individual elements labelled (Figure 25-4(b)). The circuit of Figure 25-4(b) can be simplified with the following reasonable approximations:

1. Gate-to-source capacitance of MOS-FET's is invariably small and can be neglected.

2. During switching, all DC values can be considered as ground. This enables one to consider all capacitors leading to  $V_0$  as ground capacitors. Figure 25-4(c) takes the simplifications into account, as well as lumping parallel elements to obtain

$$\frac{1}{2} C_1 = C_2 = C_3 = C_4 = C_5 = C_6,$$

and the numbering of six nodes.

Equations for current sources and other equivalents for Figure 28-4(c) are given in Table 25-1. The node equations of interest involve the output voltage and the substrate voltage, and arise from nodes 1 and 4:

$$\text{Node 1. } (C_1 + C_3) \dot{V}_{bn2} - I_{dn1} + I_{dn2} = C_1 \dot{V}_A + C_3 \dot{V}_B.$$

$$\begin{aligned} \text{Node 4. } (C_2 + C_4 + C_5 + C_6) \dot{V}_{out} - I_{dp1} - I_{dp2} - I_{dn2} \\ = C_6 \dot{V}_A + (C_4 + C_5) \dot{V}_B, \end{aligned}$$

where  $V_1 = V_{bn2} = V_4 = V_{out}$ .

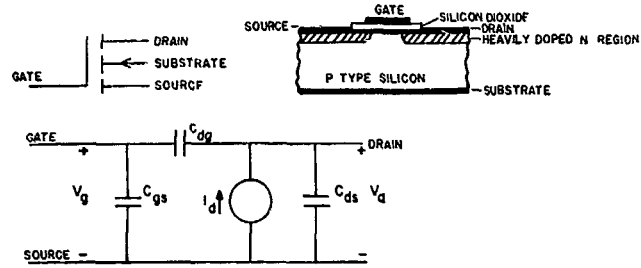


Figure 25-1—Metal oxide semiconductor-field effect transistor (MOS-FET).

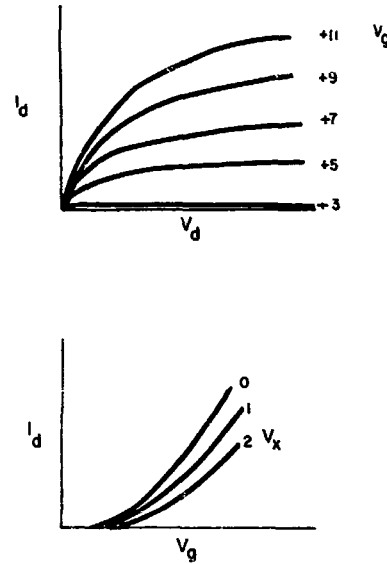


Figure 25-2—Characteristics of MOS transistors.  
(a) The  $V$ - $I$  characteristics of N-type MOS transistors.  
(b)  $V_g - I_d$  characteristic shift due to  $V_x$ .

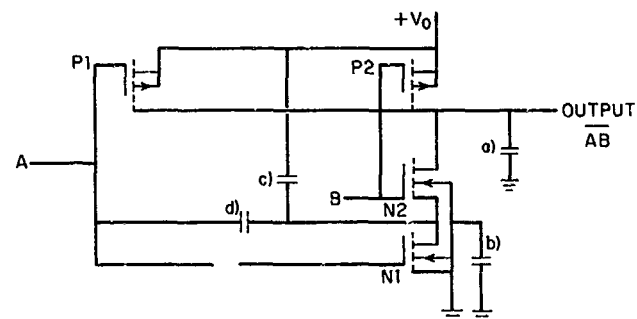
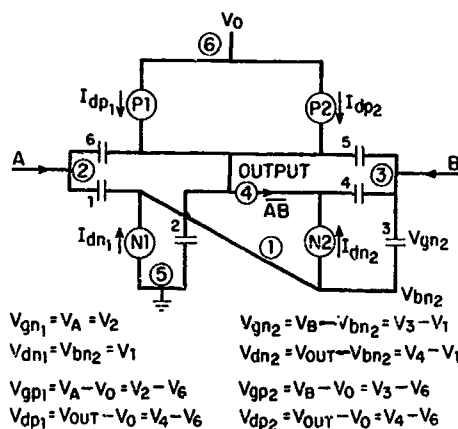
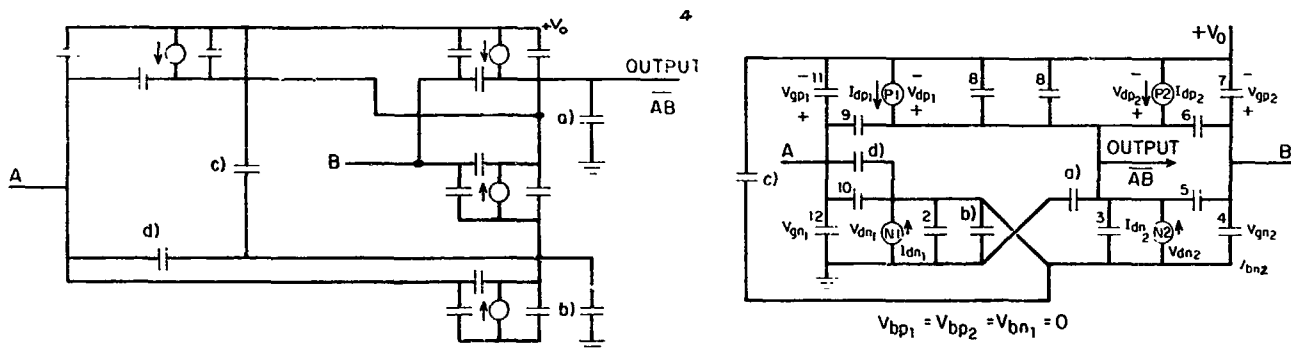


Figure 25-3—MOS-FET NAND gate.

$V_{gn1}$	$I_{dn1}$	Condition	$V_{dn1}$
$V_A$	0	$V_{gn1} \leq V_{tn1}$	$V_{bn2}$
	$-2P(V_{gn1} - V_{tn1})V_{dn1} + PV_{dn1}^2$	$V_{dn1} \leq V_{gn1} - V_{tn1}$	
	$-P(V_{gn1} - V_{tn1})^2$	$V_{dn1} \geq V_{gn1} - V_{tn1}$	
$V_{gn2}$	$I_{dn2}$	Condition	$V_{dn2}$
$V_B - V_{bn2}$	0	$V_{gn2} \leq V_{tn2} + V_{x2}$	$V_4 - V_{bn2}$
	$-2P(V_{gn2} - V_{tn2} - V_{x2})V_{dn2} + PV_{dn2}^2$	$V_{dn2} \leq V_{gn2} - V_{tn2} - V_{x2}$	
	$-P(V_{gn2} - V_{tn2} - V_{x2})^2$	$V_{dn2} \geq V_{gn2} - V_{tn2} - V_{x2}$	
$V_{gp1}$	$I_{dp1}$	Condition	$V_{dp1}$
$V_A - V_0$	0	$V_{gp1} \geq V_{tp1}$	$V_4 - V_0$
	$2P(V_{gp1} - V_{tp1})V_{dp1} - PV_{dp1}^2$	$V_{dp1} \geq V_{gp1} - V_{tp1}$	
	$P(V_{gp1} - V_{tp1})^2$	$V_{dp1} \leq V_{gp1} - V_{tp1}$	
$V_{gp2}$	$I_{dp2}$	Condition	$V_{dp2}$
$V_B - V_0$	0	$V_{gp2} \geq V_{tp2}$	$V_4 - V_0$
	$2P(V_{gp2} - V_{tp2})V_{dp2} - PV_{dp2}^2$	$V_{dp2} \geq V_{gp2} - V_{tp2}$	
	$P(V_{gp2} - V_{tp2})^2$	$V_{dp2} \leq V_{gp2} - V_{tp2}$	



**Figure 25-4—Circuit models.**

(a) NAND gate      (b) Labelled equivalent circuit      (c) Circuit model used for computer analysis.

By substituting the equivalents given in the smaller boxes of Table 25-1 into the equations of the current sources, a set of reduced equations is obtained. This set of reduced equations, which describe  $\ell_{dn1}$ ,  $\ell_{dn2}$ ,  $\ell_{dp1}$ ,  $\ell_{dp2}$ , are substituted into the Node 1 and Node 4 equations to obtain nonlinear equations of the form

$$y' = f(x, y, z),$$

$$z' = g(x, y, z).$$

A FORTRAN IV computer program solves these equations. The program uses a fourth-order Runge-Kutta scheme, and the step size in the integration can be adjusted for desired accuracy.

Results for a ramp input at one terminal are sketched in Figure 25-5. Experimental curves are drawn smoothly, and the output of the program is indicated by plus signs (+). The curves show that for a 10-nanosecond risetime in input, inverted delay switches in about 95-100 nanoseconds.

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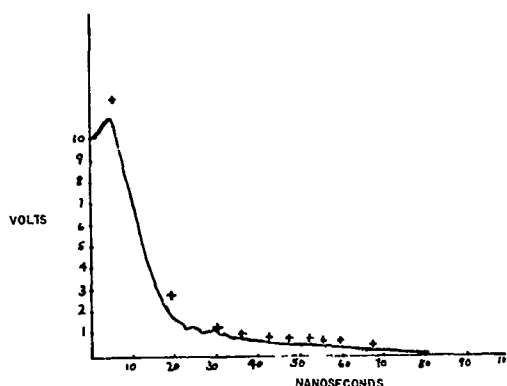
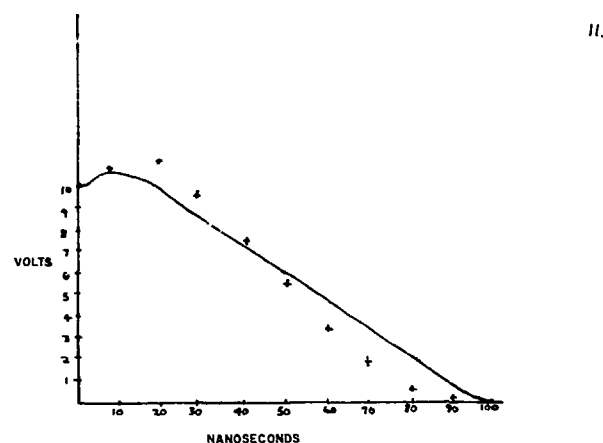
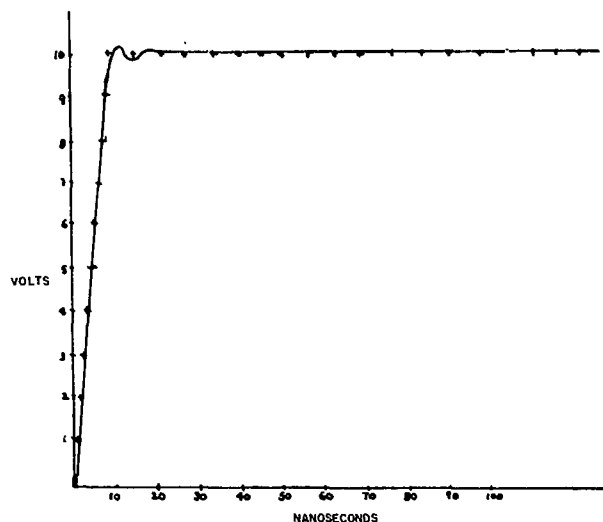


Figure 25-5—Results for ramp input at one terminal.  
(a) Input versus time  
(b) Output versus time  
(c) Substrate voltage versus time.

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N67-31588

26. FLOWGRAPHS: A DISPLAY TECHNIQUE FOR INTERACTIONS BETWEEN  
THERMAL AND ELECTRICAL DEVICE PARAMETERS

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This paper reports progress made on a continuing NASA/ERC in-house research effort to examine the complex relationships between variables and parameters in microcircuits. Flowgraph analysis is used to provide evidence of the interactions under investigation. Flowgraphs describe relationships between thermal and electrical parameters of devices and associated circuits. In addition, flowgraphs permit a systematic investigation of a wide range of device phenomena, such as thermal stability, and are applied to temperature dependent parameter variations in transistors. Flowgraph analysis is used to evaluate design criteria for compensation of thermal effects by associated circuits, and flowgraph models serve to justify design limitations and design approximations based on thermal dependence.

## INTRODUCTION

The relationships between component parameters and thermal behavior are investigated with the following objectives in mind:

1. To develop a physical and analytical explanation of the interaction between thermal and electrical effects.
2. To determine criteria which describe effectively thermal instability caused by positive feedback between the thermal circuit and the electrical circuit. This instability is often referred to as "thermal runaway."
3. To assess quantitatively the sensitivity of circuit parameters to temperature variations and develop a set of judicious approximations valid over suitably specified temperature ranges.

Although many technical publications reveal extensive work on thermal sensitivity, the approaches proposed fall short of the objectives stated above in several respects, specifically:

1. The limitations under which the approximations are valid are not known or not stated. (See References 2, 3, 6, 8.)
2. The concept of thermal feedback and the parameters used to describe it are defined in such a manner that ambiguity is possible, and frequently misapplication results. (See References 2, 3, 4, 6, 7, 8.)
3. The circuit sensitivity is calculated before the thermal runaway, and the temperature dependence of the transistor is evaluated. This approach entails making approximations without ascertaining their validity. (See References 3, 4, 6, 8, 9.)

This investigation aims at surmounting these shortcomings by employing recently developed techniques of flowgraph analysis (References 10 through 16). Flowgraphs are mathematical models establishing the interrelation between variables of systems with large numbers of components. By establishing a model for both the thermal circuit and the electrical circuit and by defining clearly the interactions; it is possible to describe the system accurately; then to make a well-defined set of approximations; and finally, to advance a design procedure based upon the approximate model.

Four distinct sets of assumptions are involved:

1. Approximations cannot be used since the transistor is operating in the nonlinear region; thus the design must resort to experimental data.
2. Approximations cannot be justified, but the designer suspects the linear assumptions to be valid. The linear approximation is useful as a trial solution subject to subsequent verification.
3. Approximations are valid but range of validity must be specified.
4. Small signal analysis applies; all approximations are valid.

The appropriate assumption should always be stated explicitly.

## OPERATION OF THE P-N DIODE

Analysis of dc bias, stability, and temperature sensitivity of transistor circuits involves the small-signal transistor parameters as well as temperature-dependent steady state (operating point or large signal) parameters. Temperature sensitivity of these parameters depends on semiconductor properties which are usually provided as empirical design data or derived from solid state physics.

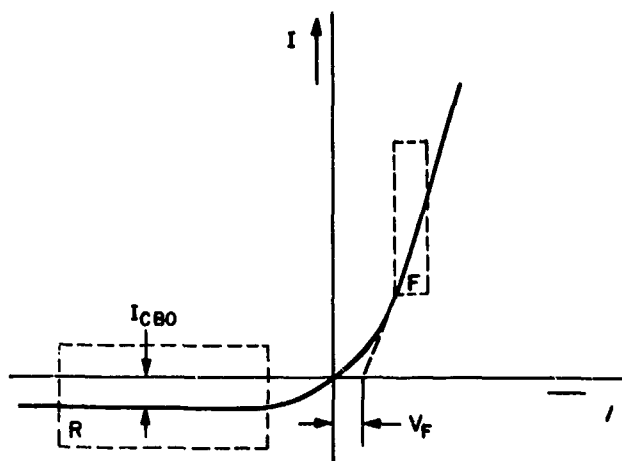


Figure 26-1—Regions of operation of biased diode.

point from small signal parameters such as  $h$  parameters. The  $H$  parameters can be obtained from the large signal curve noting that for  $\Delta V_{BE}$ ,  $\Delta I_E$ , etc., the entire linear region changes, while the  $h$  parameters are obtained from the small signal slope.

Consider the steady-state current flowing in a normally operated forward biased transistor, Figure 29-2. The base-to-emitter diode is forward biased and the collector diode is reverse biased. Only under these conditions, will  $I_{CBO}$  flow between collector and base. Definition:  $I_{CBO}$  is defined as the current flowing between the base and collector if the emitter is disconnected. Thus:  $I_C = -H_{FB} I_E + I_{CBO}$  and  $I_B = (1+H_{FB}) I_E - I_{CBO}$ . An increase in  $I_{CBO}$  decreases the base current and increases the collector current. This condition can be verified by the definition of  $I_{CBO}$  (Figure 26-2).

The temperature-induced changes of  $I_{CBO}$  and  $V_F$  are incorporated in the common base equivalent circuit (Figure 26-3) and in the corresponding flowgraph model (Figure 26-4).

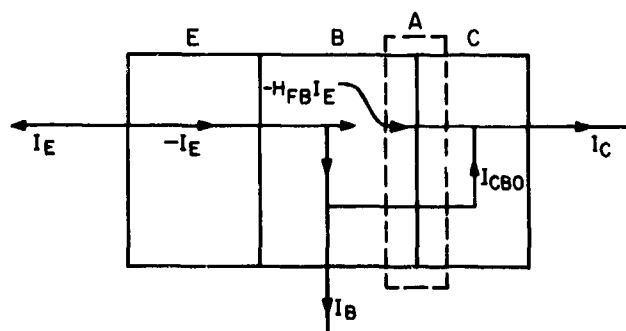


Figure 26-2—Definition of currents in transistor.

First in importance is the leakage current  $I_{CBO}$  in the backward biased diode and the voltage drop  $V_F$  in a forward biased diode (Figure 26-1). Both parameters are temperature-dependent. In silicon transistors an increase in temperature of  $10^\circ \text{C}$  causes  $I_{CBO}$  to double. As indicated in the introduction, small-signal analysis techniques are employed here for thermally dependent variations of the steady state current. A notation, such as  $H_{IB} = \frac{\Delta V_{BE}}{\Delta I_E}$ , will be used to denote thermally-dependent, two-port large signal parameters. Capital-letter  $H$  parameters are used to differentiate operating

## COMMON EMITTER CONFIGURATION

The sum of the currents entering and leaving the closed volume  $A$  in Figure 26-2 is described by the flowgraph of Figure 26-5. Path inversion gives a flowgraph appropriate for common-emitter configuration (Figure 26-6). Since  $(1 + H_{FE})$  is usually 50 times, the effect of  $I_{CBO}$  is much more significant in the common-base configuration.

The current  $I_{CBO}$  flowing across the emitter junction will be amplified as if it were a regular

base current. The amplified current  $H_{FE} I_B$  will be  $H_{FE} I_{CBO}$ . An addition of  $I_{CBO}$  and  $H_{FE} I_{CBO}$  gives the total current flowing from emitter to collector. Adding  $H_{RE}$ ,  $H_{IE}$ , and  $H_{OE}$  gives the temperature dependent common emitter circuit model (Figure 26-7) and the flowgraph model (Figure 26-8).

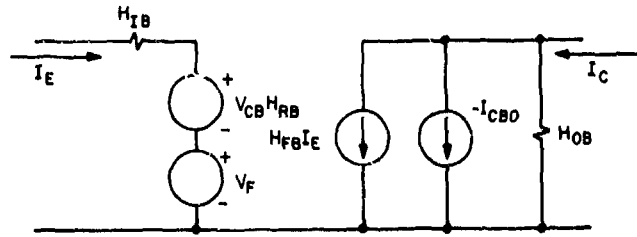


Figure 26-3—Common base circuit model.

### THERMAL CONSTRAINTS

For changes in temperature up to 75° C above the specified operating temperature of the transistor,  $I_{CBO}$  increases by a factor of 2 for an increase in temperature  $T_T = 10^\circ \text{C}$  in silicon transistors and of  $T_T = 7^\circ \text{C}$  in germanium transistors.

Thus

$$\frac{I_{CBO}}{I_{CBO}^*} = \frac{T}{T_T} (\ell n 2)$$

and

$$I_{CBO} = I_{CBO}^* 2^{(T-T_0)/T_T}$$

where  $I_{CBO}^*$  is the initial value at  $T = T_0$ .

To a first-order approximation

$$I_{CBO} = I_{CBO}^* J_T T$$

where

$$J_T = \frac{\ell n 2}{T_T}$$

yielding a transmittance in Figure 26-9(a), which does vary greatly with temperature.

The temperature will reach a steady-state value only when all the heat generated ( $P_g$ ) by the transistor is dissipated by the heat sink ( $P_d$ ), as Figure 26-9(b) shows. In turn the heat generated in the transistor is  $I_{CE} V_{CE}$ , modeled suitably in Figure 26-9(c).

The heat dissipated by the heat sink is proportional to the temperature difference ( $\Delta T$ )

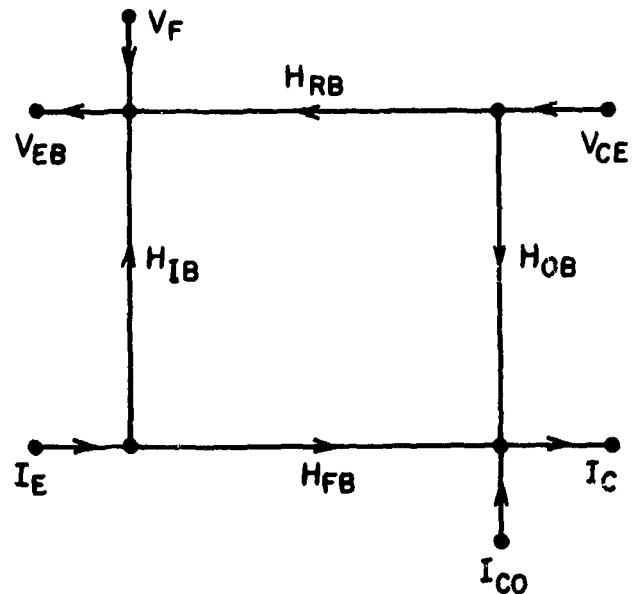


Figure 26-4—Common base flowgraph model.

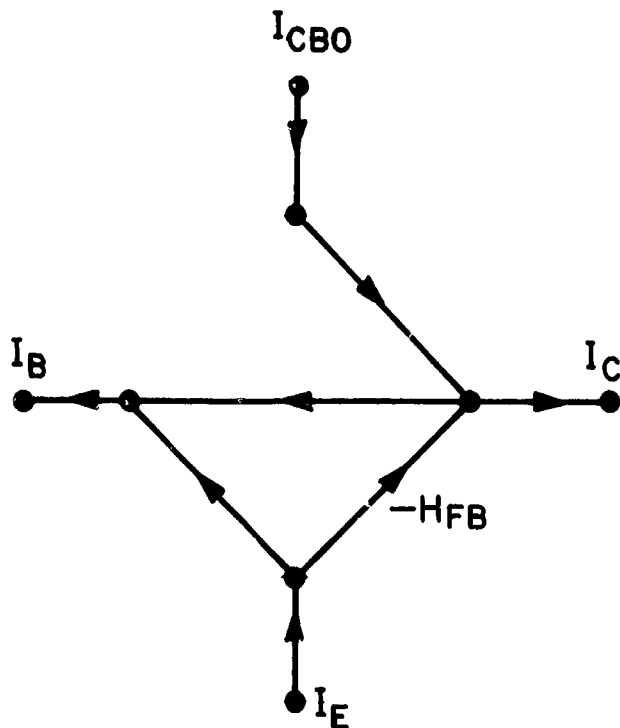


Figure 26-5—Common emitter flowgraph.

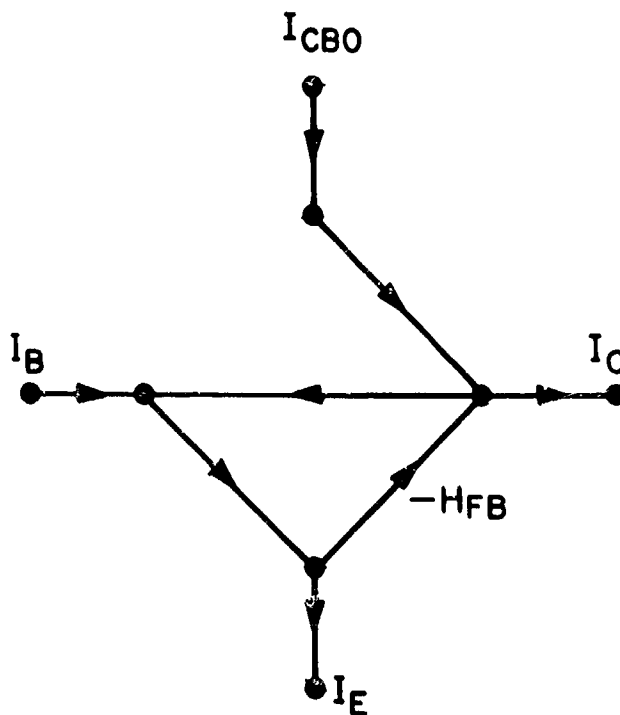


Figure 26-6—Path inversion for Figure 5.

between the transistor and the heat sink and to the heat-sink constant,  $C$  defined as the heat flow per unit temperature. Combining the flowgraphs in Figure 26-9 gives the relationship between  $I_{CBO}$  and  $T$  shown in Figure 26-10.

Combining the flowgraphs in Figure 26-8 and Figure 26-10 yields Figure 26-11 for calculating temperature biasing dependence and thermal runaway. Thus

$$I_C = \frac{I_B H_{FE}^* + I_{CBO}^* (1 + H_{FE}^*) + V_{CE} H_{OE}^*}{1 - (I_{CBO}/I_F)}$$

where  $I_F$  is the critical thermal feedback current

$$1/I_F = \frac{J_T V_{CE}}{C} (1 + H_{FE}^*)$$

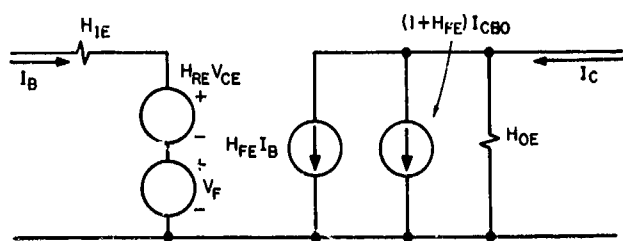


Figure 26-7—Common emitter flowgraph.

### RUNAWAY LIMIT

It is advantageous to define the thermal feedback loop  $F_T = \frac{I_{CBO}}{I_{F(Q)}}$  at the operating point of  $Q$  point when  $1/I_{F(Q)} = \frac{J_T V_{CE(Q)} (1 + H_{FE}^*)}{C}$

At the thermal run. way

$$I_{CBO}^* \approx I_F$$

and

$$1/I_{F(R)} \approx \frac{J_T E_{CE}}{C} (1 + H_{FE}^*)$$

$I_F$  is minimum when  $V_{CE}$  equals  $V_{CE} \text{ (max)}$ . Since  $V_{CE} \text{ (max)}$  usually equals the circuit dc supply voltage ( $E_{CC}$ ), the critical runaway cur-

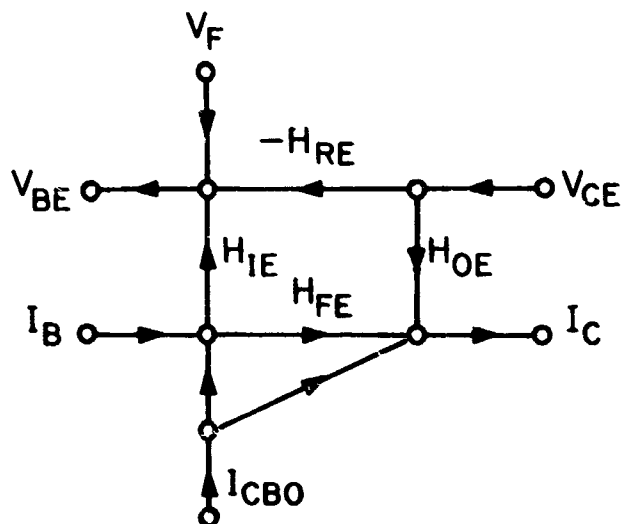


Figure 26-8--Common emitter flowgraph model.

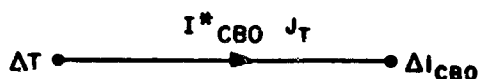


FIG. 9(a)



FIG. 9(b)

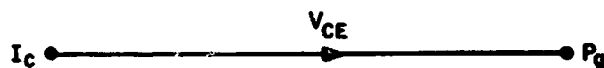


FIG. 9(c)

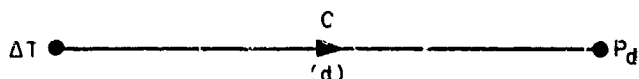


Figure 26-9--Functional relations for thermal dependence.

rent  $I_{F(R)}$  is calculated for  $V_{CE} = E_{CE}$ . Runaway will occur as  $I_{CBO}^*$  approaches  $I_{F(R)}$ . Hence, a large value of  $I_{F(R)}$  is desirable and represents an upper limit, which increases as the thermal circuit improves. Therefore,  $I_{F(R)}$  is a figure of merit of the cooling design. The response of the temperature feedback has a time constant in the 0.1- to 10-second range. It is slow relative to the small signal variations in electronic circuits. Therefore, it is justified to neglect the variations of  $T$  with respect to the small signal variation of the input.

## TEMPERATURE SENSITIVE PARAMETERS

The variation of transistor components depends of the  $I_F$  at the Q point. The value of  $I_{F(Q)}$  is about one-half of the value of  $I_{F(R)}$ . Thus

$$I_{C(Q)} = \frac{I_B H_{FE}^* + I_{CBO}^* (1 + H_{FE}^*) + V_{CE} H_{OE}^*}{1 - F_T}$$

Comparison with  $I_C$  calculated from Figure 26-8 yields the temperature-dependent parameters  $\frac{H_{FE}^*}{1 - F_T}$  and  $\frac{H_{OE}^*}{1 - F_T}$ .

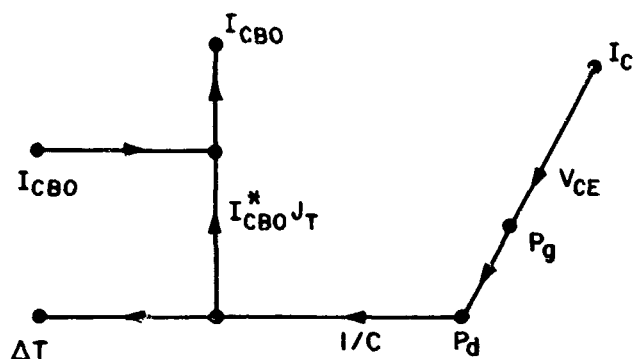


Figure 26-10—Relations between transistor currents and temperature.

### TEMPERATURE SENSITIVITY

In the design of a circuit, the possible occurrence of thermal runaway must first be examined; only then can thermal sensitivity be considered. The thermal sensitivity parameters  $S_1$ ,  $S_v$ , and  $S_2$  specify the changes in the large-signal currents and voltages with respect to the temperature-dependent parameters<sup>2</sup>. Thus,

$$S_1 = \frac{\Delta I_E}{\Delta I_{CBO}} \cdot S_2 = \frac{\Delta I_C}{\Delta I_{CBO}} \cdot \text{and } S_v = \frac{\Delta V_{CE}}{\Delta I_{CBO}}.$$

The supply voltage  $V_1$  is assumed to be constant. Similarly, voltage stability factors at constant  $I_{CBO}$  can be formulated.

### DESIGN EXAMPLES

A temperature feedback factor  $F_T$  of 0.2 or less is considered adequate in design. Furthermore, if the amplified base current  $I_B H_{FE}$  exceeds significantly the ohmic current  $V_{CE} H_{OE}$  in the collector port, the direct contribution of  $V_{CE}$  to  $I_{CE}$  can be neglected. Hence,

$$I_C = I_B H_{FE} + I_{CBO} (1 + H_{FE}).$$

It is only under these restrictions that this formula is justified, although it is frequently used, irrespective of the thermal circuit and frequently leads to erroneous results. Although the direct contribution of  $V_{CE}$  to  $I_C$  can be often neglected, the effect of  $V_{CE}$  through the thermal loop must remain as a factor of  $F_T$ . The transistor model used in sensitivity calculations is given in Figure 26-13.

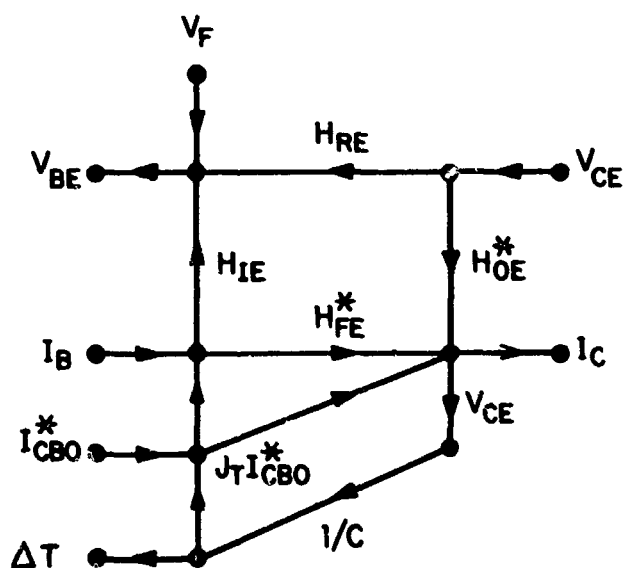


Figure 26-11—Temperature dependence for configuration.

The foregoing criteria for temperature-dependent transistor parameters will now be illustrated by examples. The temperature-dependent transistor model makes it possible to define a linear graph for the circuit using accepted flowgraph techniques (References 14 through 21). All voltage sources are represented as branches (heavy line), all current sources are represented as links (dashed line), and the branches form a connected but not closed structure (tree). A tree is achieved since passive elements of the circuit can be assigned to branches or links. The flowgraph is constructed from the equivalent circuit by assigning two nodes to each parameter, a voltage node and a current node. The nodes are then interconnected by defining:

1. Current nodes for the branches as function of current nodes for the links
2. Voltage nodes for the links as function of voltage nodes for the branches
3. The current node as function of the voltage node and impedance for passive parameters that were chosen to be links
4. The voltage node as function of the current node and resistance for passive parameters that were chosen to be branches
5. Active parameters in terms of conditions and controlled variables. Results are summarized in Table 26-1.

## CONCLUSION

Flowgraph models provide a useful technique to describe the interactions between thermal and electrical device parameters under temperature variation. Device performance is analyzed by first establishing a flowgraph model, which is systematically constructed on the basis of physical phenomena and of system constraints. Thermal and electrical performance characteristics of the device result from this model. The model is then examined to determine the presence of feedback and similar relationships

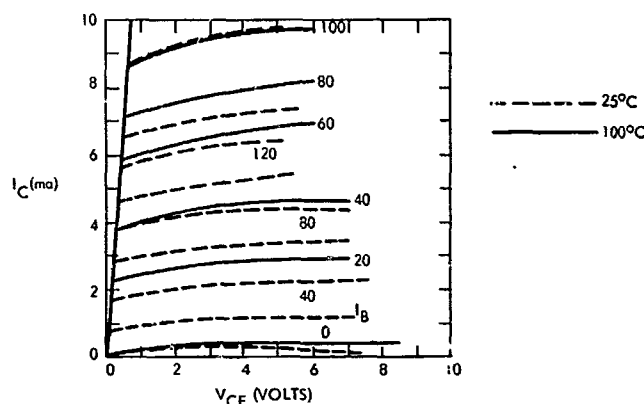


Figure 26-12—Transistor characteristics Texas Instruments 2N335 (redrawn from Reference 1).

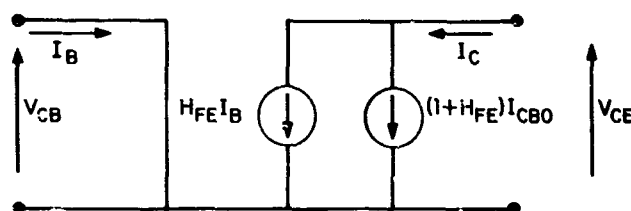


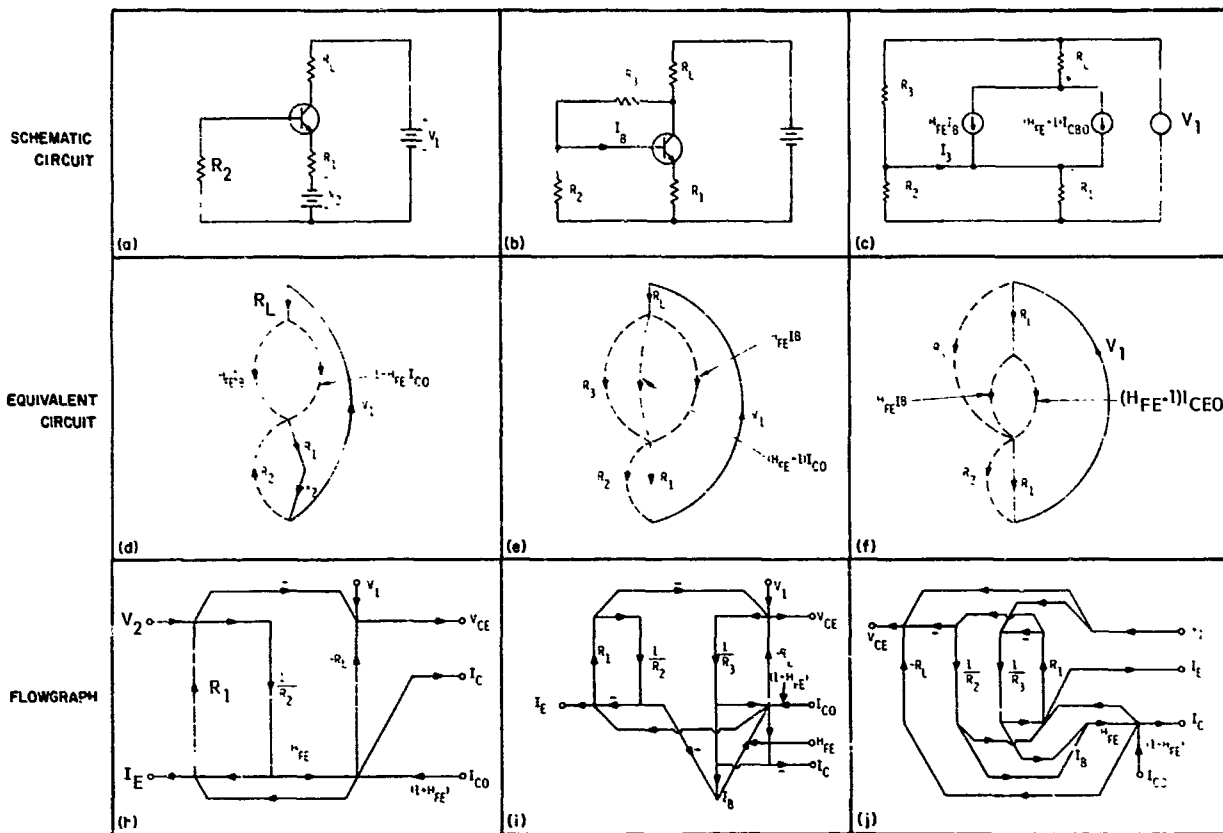
Figure 26-13—Transistor model for sensitivity calculations.

$$F_T < 0.2$$

$$V_{CE} H_{OE} \ll I_B H_{FE}$$

$$H_{FE} = \frac{H_{FE}^*}{1 - F_T}$$





$s_1$	$\frac{(1+H_{FE})}{1+(1+H_{FE}) \frac{R_1}{R_2}}$	$\frac{(1+H_{FE}) \frac{R_L}{R_3} (1+H_{FE} \frac{R_1}{R_2})}{1 + (1+H_{FE}) (\frac{R_L}{R_3} + \frac{R_1}{R_2} + \frac{R_1}{R_3} + \frac{R_L R_1}{R_2 R_3})}$	$\frac{1+H_{FE}}{1 + \frac{R_1}{R_3} + \frac{R_1}{R_2} + H_{FE} \frac{R_1}{R_3} + H_{FE} \frac{R_1}{R_2}}$
$s_2$	$\frac{(1+H_{FE}) (1 + \frac{R_1}{R_2})}{1+(1+H_{FE}) \frac{R_1}{R_2}}$	$\frac{(1+H_{FE})}{1 + (1+H_{FE}) (\frac{R_L}{R_3} + \frac{R_1}{R_2} + \frac{R_1}{R_3} + \frac{R_L R_1}{R_2 R_3})}$	$\frac{(1+H_{FE}) (1 + \frac{R_1}{R_2} + \frac{R_1}{R_3})}{1 + (\frac{R_1}{R_2} + \frac{R_1}{R_3}) (1+H_{FE})}$
$s_V$	$\frac{(1+H_{FE}) (-R_L) (1 + \frac{R_1}{R_2}) - R_1 (H_{FE}+1)}{1+(1+H_{FE}) \frac{R_1}{R_2}}$	$\frac{-(1+H_{FE}) (R_L) (1 + \frac{R_1}{R_2})}{1 + (1+H_{FE}) (\frac{R_L}{R_3} + \frac{R_1}{R_2} + \frac{R_1}{R_3} + \frac{R_L R_1}{R_2 R_3})}$	$\frac{-(1+H_{FE}) [R_L (1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}) + R_1]}{1 + (1+H_{FE}) (\frac{R_1}{R_2} + \frac{R_1}{R_3})}$
$I_E$	$s_1 I_{CBO} + \frac{V_2 (H_{FE} - 1)}{1+(1+H_{FE}) \frac{R_1}{R_2}}$	$s_1 (I_{CO} + V_1 R_3)$	$\frac{I_{CBO} (1+H_{FE}) + V_1 (\frac{1}{R_3} + \frac{1}{R_2} H_{FE})}{1+(1+H_{FE}) (\frac{R_1}{R_2} + \frac{R_1}{R_3})}$
$V_{CE}$	$s_V I_{CBO} + V_1 - V_2 \frac{\frac{R_L}{R_2} (H_{FE} + 1)}{1 + (1+H_{FE}) \frac{R_1}{R_2}}$	$s_V I_{CO} + s_1 V_1 \frac{R_1}{R_2}$	$V_1 \frac{[2 - (1+H_{FE}) \frac{R_1}{R_3} - R_L H_{FE} (1 - \frac{R_1}{R_2})]}{1 + (1+H_{FE}) (\frac{R_1}{R_2} + \frac{R_1}{R_3})}$

Table 26-1—Sensitivity criteria for stabilizing circuits.

between thermal and electrical parameters. Of particular interest are conditions for stability of the system.

The flowgraph model is utilized to determine other device properties as follows:

- Assumptions necessary to permit approximations in performance characteristics
- Procedure for evaluating temperature sensitivity of parameters
- Figures-of-merit for stability of a system against thermal "runaway".

Flowgraph techniques thereby provide a valid as well as practical design approach.

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27. COMPUTER-ORIENTED MODELLING OF INTEGRATED CIRCUITS:  
ALGORITHMS FOR THE DICHOTOMOUS PRESENTATION OF ACTIVE NETWORKS

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Progress is reported on a research effort aimed at developing standardization and qualification procedures for integrated circuits through computer-aided design evaluation. A compatible series of computer programs is developed for circuits with many components, typically 30-100. The programs are based on theorems for oriented, weighted graphs, and are intended to meet circuit design requirements which exceed the memory capacity of medium-size computers when programs based on node or mesh analysis are employed. Since these limitations become more severe as worst-case design, Monte-Carlo routines, and similar reliability techniques are introduced, the procedure developed is particularly useful to designers and analysts with access to a medium or desk size computer, or to a time-sharing outlet. The approach is based on the dichotomy entailed in the flowgraph associated with any active network. Algorithms are established for three purposes: To dichotomize the network into voltage and current generators; To examine separately each set and the associated system of controls interrelating both sets; and To establish a flowgraph in terms of a unique dichotomous presentation for a given equivalent circuit. While the algorithms were developed for linear networks, the dichotomous procedures provide a less restricted approach.

## INTRODUCTION

The evaluation of network functions, by matrix operations such as mesh or nodal analysis, has inherent limitations associated with partial or complete inversion of matrices. Typical limitations are necessity for substantial memory, inaccuracies due to round-off error, and large running time.

The complexity of a matrix-based evaluation routine increases with the number of trees inherent in the network topology, which in turn appears to increase factorially with the number of network elements. As a consequence, networks with 20 to 50 components are now considered beyond the capabilities of small computers such as the IBM 1620. To overcome these limitations,

the following alternatives are being explored:

1. Increase in computer memory from  $10^7$  bits to  $10^{10}$  bits.
2. Decreases in computer operation times from  $10^{-5}$  to  $10^{-10}$  seconds.
3. Utilization of relaxation techniques for matrix operations.
4. Utilization of dichotomous procedures in place of matrix procedures.

"Dichotomy" is derived from the Greek "dich" (in two) and "temnein" (to cut), and refers to a separation of the system by appropriate cuts into two or more subsystems, followed by an analysis of each subsystem and of the relationships between the subsystems. Networks seem to be ideally suited for dichotomy into separate subsystems such as the following, which appear more amenable to computer-oriented methods of analysis:

1. Subsystems relating through-variables, such as Kirchhoff's current law.
2. Subsystems relating across-variables, such as Kirchhoff's voltage law.
3. Interrelations between the above subsystems, such as Ohm's law.

The dichotomous representation of lumped parameter systems is based on analysis of the functional dependence between the two variables associated with each parameter, and forms the foundation of flowgraph and similar network descriptions. It is essential to distinguish between the concept of subsystem based on dichotomy, which separately analyzes two or more properties of each parameter of the system, and the concept of subsystem resulting from dicoptics, an approach employed by Kron and Happ (Reference 5), which involves tearing the system into parts and analyzing properties identical to those used before tearing. Dicoptics is essentially a search for judiciously selected subsystems to minimize interconnections and maximize intraconnections; its purpose is to reduce significantly the number of variables to be evaluated. Conversely, in the dichotomy entailed in flowgraphs the number of variables is doubled, thus increasing the size of the associated matrix. This dichotomy, therefore aims at reducing the complexity of algorithms, not the size of the matrix associated with the system.

#### Equivalent Circuit Description

A network with active and passive elements which may be nonlinear consists of:

1. A set of vertices; each vertex is defined as an electrically distinct point.
2. A set of elements; each element is defined by direction from A, the origin vertex, to B, the target vertex.

3. The network topology, which is defined by associating with each element a set of vertices, A and B. Similarly, other network properties are defined by associating with each element other properties, described by the symbols C, D, E, F, G and H.
4. With each element E is associated a control function, C, a control element, D, and a generator function, G. In controlled sources  $D \neq E$ , and in passive elements  $D = E$ . There are also associated a frequency dependent indicator F and a tagging variable H.
5. For independent sources, D is absent; this case does not occur in computer-oriented calculations, and is only of academic interest.
6. The dichotomy of a network is accomplished by requiring that the properties D and E be split into two mutual categories, denoted by the binary symbols 1 and 0. The dichotomy in control function D is described by property C, and the dichotomy in generator element E is described by property G.

This network can be represented graphically by an equivalent circuit (Figure 27-1). The information needed to code the circuit in Figure 27-1 is found in the equivalent circuit (Figure 27-2).

### Review of Dichotomous Techniques

The dichotomy is based on constraints imposed by laws of physics, and implemented by assigning each function a binary code 0 or 1. Cross-variables or voltages are coded by "0." Through-variables or currents are coded by "1." No two voltage generators may be in parallel. No two current generators may be in series. The topology of voltage generators forms a tree, or Z structure. The topology of current generators forms a link, or Y structure.

Guidelines, algorithms, and resulting programs for selection of an equivalent circuit from a schematic circuit diagram are excluded from the scope of this investigation. It is assumed that sufficient information is given to construct the equivalent circuit in Figure 27-1. The objective of

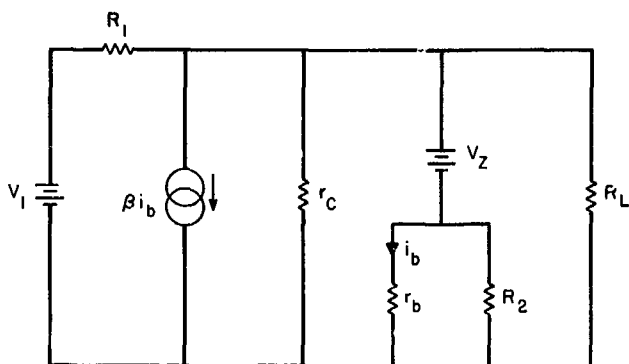


Figure 27-1—Equivalent circuit for voltage regulator.

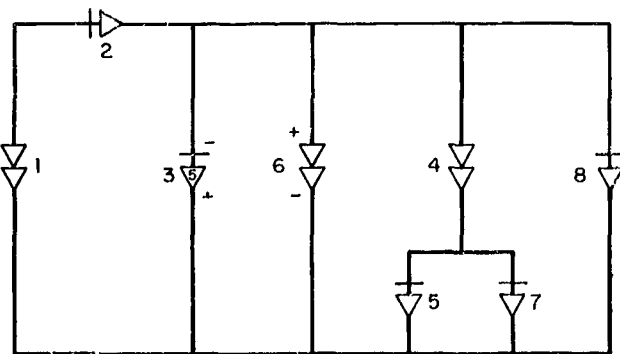


Figure 27-2—Coded equivalent circuit, exhibiting dichotomy.

this investigation is to construct a dichotomous presentation of the network. A flowgraph is defined here as a network description in which an element is identified by:

1. Two variables, such as current and voltage.
2. A functional relationship specifying the direction of functional dependence between the variables.
3. A symbol or numerical relationship denoting this functional relationship.

The flowgraph is, therefore, a dichotomous network description: its specific form — matrix, directed graph, or code — is immaterial.

Since the usage of the terms "block diagram" and "flowgraph" as synonyms has led to much confusion, it seems appropriate to define block diagram by the following properties:

1. An oriented, weighted graph with two distinct types of nodes: contributive, or summing point, and distributive, or sampling point.
2. A functional relationship between nodes, specifying the direction of functional dependence between the variables.
3. A description of the functional relationship between variables.

The flowgraph, therefore, has distinct features which distinguish it from the block diagram. A flowgraph is a unique description of a network, while a block diagram description entails arbitrary and subjective decisions. The functional dependence describing any network element always expresses a distributive node as a function of a contributive node, but never otherwise. The functional relationships governing interconnections between elements are dependent only on the network topology and are restricted to three values, 0, +1, and -1. The functional dependence always expresses a contributive node in terms of a distributive node, and never otherwise.

From a draftsman's vantage point, a flowgraph as defined here may be drawn as a block diagram, without violating the foregoing definition of a flowgraph or block diagram.

#### Unique Features of Dichotomous Approach

The dichotomous approach presented here entails several original and unique features of primary interest to the systems analyst:

1. A systematic procedure of problem formulation in terms of a closed system. This implies that the unknown to be evaluated forms an integral part in setting up the problem.



2. An approach to circuit evaluation and design based on algorithms. This implies that the engineer is to formulate his problem so that it is understandable to a computer programmer, who is not expected to acquire an understanding of the engineering aspect of the problem.
3. A splitting-up of a large system of equations into several "simpler" systems which can be analyzed with greater facility. If the system is linear, the functional relationships describing the overall system are separated into two sets of algebraic relationships (Kirchhoff's current and voltage laws) and a set of first order differential operators relating them. In nonlinear systems, the linear operator is replaced by an appropriate subroutine.

These features are best understood by examining an illustrative example. A set of algorithms will then be presented.

## TERMINOLOGY

### Coding of Network Topology

The sample problem of Figures 27-1 and 27-2 for the computer program is illustrated in Table 27-1. Input data for each element of the circuit consisting of:

1. Code A B C D E F G for the equivalent circuit.
2. A numerical value of the element in terms of a real or a complex number.
3. Tagging variables, such as H, which define the desired solution.

Table 27-1

Problem Statement for Voltage Regulator  
(Figure 27-1)

A	B	C	D	E	F	G	H	Numerical
2	1	0	0	1	0	0	0	.500 E+2
2	3	0	2	2	0	1	0	.400 E-1
3	1	1	6	3	0	1	0	100 E+3
3	4	0	0	4	0	0	0	.250 E+2
4	1	0	5	5	0	1	0	.100 E-1
3	1	1	6	6	0	0	0	.100 E+6
4	1	0	7	7	0	1	0	.200 E-1
3	1	1	8	8	0	1	1	.100 E+1

The coding procedure is implemented as follows:

1. All elements and distinct electrical points are numbered consecutively. Entries A, B, and E describe the network topology. The origin and termination vertex of each element are A and B, while E is the element number.
2. The direction of positive current through element E is specified by vertices A and B to be from A to B, and defines a voltage rise in active elements and a voltage drop in passive elements.

3. Frequency dependence is specified by code  $F$  as  $s^F$ . For example, an entry "0" denotes no dependence, while 1 denotes linear dependence on frequency.

#### Coding of Network Dichotomy

The dichotomy of the network elements is described by entries  $C$  and  $G$ . Entry  $G$  indicates whether the element is a current generator or a voltage generator. Similarly, each element is controlled by either a current or a voltage; this control is denoted by entry  $C$ . The two permissible values for each  $C$  and  $G$  are defined in terms of a binary code: "0" for voltage and "1" for current. Table 27-2 outlines the dichotomous criteria. Four possible combinations of  $C$  and  $G$  specify the circuit element and unknown transmittance desired:

1.  $C = 0, G = 0$ : Amplification - a voltage controlled voltage generator. (V)
2.  $C = 1, G = 1$ : Amplification - a current controlled current generator. (W)
3.  $C = 0, G = 1$ : Admittance - a voltage controlled current generator. (Y)
4.  $C = 1, G = 0$ : Impedance - a current controlled voltage generator. (Z)

Controlled sources in the network may be linear elements, but the coding and construction procedure is equally valid for nonlinear elements. For nonlinear elements, the numerical values are replaced by subroutines.

#### Elements as Sources

For components of the equivalent circuit consisting of active elements, dependence is specified by entry  $D$ .  $D = 0$  denotes an independent source.  $D = E$  denotes a passive element; that is, an element controlled only by itself.  $D \neq E$  and  $D \neq 0$  denotes that  $E$  is a source controlled by element  $D$ .

Table 27-2

Criteria for Dichotomous Assignment of  $C$  and  $G$

G or C	Variable	Example
0	Across	Voltage
1	Through	Current
G	No elements	
0	In parallel	
1	In series	
C	Function	Node
	Control	Contributive
G	Generator	Distributive
Z	Impedance	$C = 1, G = 0$
Y	Admittance	$C = 0, G = 1$
W	Amplification	$C = 1, G = 1$
V	Amplification	$C = 0, G = 0$

To evaluate a network function, it is instructive to consider the following:

1. For a driving point function, the unknown voltage-current relationship is coded as an element with  $D = E$ , that is, as an active source with generator and control of the same cardinality.
2. For a transfer-function in which the unknown function is a voltage-current relationship, the generator and control have different cardinality,  $D \neq E$ . The unknown is therefore coded as a transfer immittance (Z or Y).
3. If the transfer function to be evaluated is a voltage amplification or a current amplification, then the unknown element is also coded an amplifier (V or W).

Controlled sources which are amplifiers contain:

1. A contributive node, which is the controlling variable and which has usually only a single input from another variable.
2. A distributive node, which acts as generator.
3. A transmittance from control to generator, which may be a symbol, a function or a subroutine.

### The Equivalent Circuit in Code

In Figure 27-2, a voltage generator is represented schematically by a double arrow, and a current generator by an arrow and a bar. The direction of positive current flow specifies the direction of the arrow. Positive current flow through an active source yields a voltage rise, while positive flow through a passive element corresponds to voltage drop.

The definition of positive current flow is needed to interpret the numerical value of current flow, which may be positive or negative. In practical design problems, it is convenient, and always possible, to make this value positive.

### The Closed System Formulation

The H tag relates the quantities to be determined by the equivalent circuit, and thus defines the problem uniquely. This is essential for the construction of a unique dichotomous solution.

For a desired circuit response, such as transfer function, current gain, or output impedance, all entries except one will be coded "0" for a "real" network element, with an unknown "virtual" element coded "1." For conversion of the open network to a closed network by inserting a fictitious element, the system is viewed as a "black box," with input and output terminals, and an unknown element connecting the two terminals. The element to be determined is usually coded  $E = 1$ . The artifice of setting  $E(1) = 0 + j1$  is often used for computation of the unknown response.

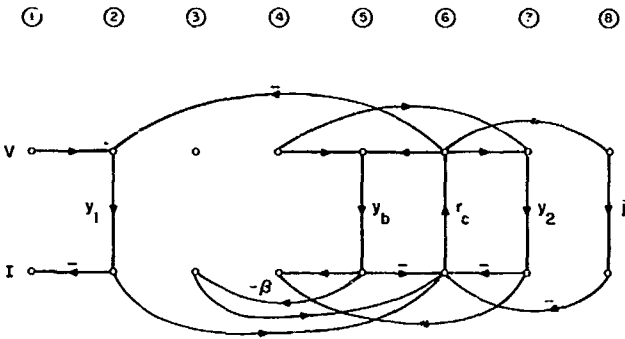


Figure 27-3—Flowgraph constructed from  $V$ ,  $W$ , and  $T$  matrices.

For a closed system, a constraint always exists which relates the network parameters,  $H \neq 0$ . If the unknown is  $E(1) = j$ , then  $H$  can be expanded as

$$H(j) = H(\bar{j}) + jH(j'),$$

where

$$H(\bar{j}) = \text{Re}(H) \quad \text{and} \quad H(j') = \text{Im}(H).$$

in practice,  $H$  is computed as a complex number, the  $j$  is redefined as an unknown, and  $H(j) = 0$  is solved for the unknown  $j = -H(\bar{j})/H(j')$ .

### Illustrative Example of Network Code

The voltage regulator in Figure 27-1 is coded in Table 27-1. The controlled source,  $E = 3$ , specifies the direction of positive current flow from node 3 to node 1. A frequency-independent current source is controlled by the current through element  $E = 6$ , thus is coded by  $C = 1$ ,  $D = 6$ ,  $F = 0$ , and  $G = 0$ . The transmittance  $E = 8$ , with value  $E(8) = j1$ , is the unknown.

Table 27-3

Problem Solution — Flowgraph Construction

V	1	2	3	4	5	6	7	8	W	1	2	3	4	5	6	7	8	T	1	2	3	4	5	6	7	8
1		+							1									1	E							
2									2	-					+			2		Y						
3									3						-			3								
4					+		+		4									4			E					
5									5		I	+		-				5		I		Y				
6		-	-		+		+	+	6									6					Z			
7									7			+		-				7							Y	
8									8						-			8								Z

The problem solution is presented in coded form in Table 27-3. Thus, algorithms are to be developed to produce a computer print-out from the coded network. The computer readout, Table 27-3, is equivalent to the flowgraph in Figure 27-3.

### Flowgraph Construction

The dichotomous presentation consists of three basic flowgraph regions: the strictly algebraic relationships  $V$  and  $W$ , for voltage and current, and  $T$ , which contains differential equations or sub-routines, referred to as transmittances. The procedure used to derive these relationships from the problem statement by the algorithms is as follows:

1. The  $V$  matrix must contain voltage relationships; hence, the tree branches, or  $G = 1$  elements, are determined in terms of the link branches, or  $G = 0$  elements.
2. The  $W$  matrix contains current relationships of the link branches, or  $G = 0$  elements, where the tree branches, or  $G = 1$  elements are treated as knowns.
3. The  $T$  matrix contains the transmittances relating the  $W$  matrix and the  $V$  matrix; the known and unknown variables are determined from code  $G$  in the problem statement.
4. The assignment of known and unknown variables in the  $V$  and  $W$  subsystems is the opposite of that in the  $T$  subsystem.

The  $V$ ,  $W$  and  $T$  matrices then form a closed flowgraph.

### Coding Convention for Flowgraph

The  $V$  and  $W$  matrices denote interconnections between elements or Kirchhoff constraints, and the  $T$  matrix describes the intraconnections within each element or transmittance. The flowgraph is interpreted in terms of signal flow. The  $T$ ,  $W$  and  $V$  matrices denote signal flow from column to row entry. Signal flow in interconnections occurs from distributive to contributive nodes. Signal flow in intraconnections from contributive to distributive nodes. Entries are finite: infinity is not admissible. Entries "+" or "-" imply +1 or -1; blanks imply zero.

## ALGORITHMS

### Properties of $V$ -matrix

The number of columns with entries is equal to the number of  $G = 1$  elements in the equivalent circuit. Each  $G = 1$  element is associated with one or more  $G = 0$  elements to form a tie set, or

closed sequence of adjoining elements. The algorithm must therefore examine the vertex origins and terminations of successive elements, to determine, for each given  $G = 0$  element, which  $G = 1$  element must be selected to form a tie set. From the network topology and the directions specified by A and B in the problem statement, the entries of V, shown in Table 27-3 result.

#### Construction of V-Matrix

Necessary data for construction are:

1. Entries A, B and G in the problem statement (Table 27-1).
2. A definition of the tie associated with each  $G = 0$  element.
3. A definition for the sign associated with each  $G = 1$  element in a given tie.

There exists a set of unknown voltages  $\bar{V}$ , consisting of elements  $E(i)$  for which  $G = 1$ ,

$$\bar{V} = (i | G(i) = 1),$$

and a conjugate set,

$$V = (i | G(i) = 0).$$

The set  $\bar{V}$  contains only elements which are current generators, while the set V contains only voltage generators. The algorithm expresses the unknown voltages in terms of the known voltages, as

$$\bar{V} = f(V).$$

There will be an entry 0, +1 or -1 in the  $V(j, k)$  position of the V-matrix if  $j \in V$  and  $k \in V$ . The entry will be  $\pm 1$  if  $E(j)$  occurs in a tie containing the  $E(k)$ . The entry will be -1 if  $E(j)$  and  $E(k)$  are directed in equal directions in the tie and +1 if in the opposite direction.

Select a tie of N elements with one element in  $\bar{V}(j)$  and  $(N - 1)$  elements in  $V(k)$  for each element in  $\bar{V}(j)$ . To illustrate, in Figure 27-1 for the tie  $E(4), E(5), E(6)$  clearly:

$$\bar{V}(j) = \bar{V}(5),$$

$$V(k) = (00010100),$$

$$\bar{V}(5) = V(4) + V(6).$$

This may be written as a code:

$$\bar{V}(5) = (000+0+00).$$

This result can usually be read off immediately from the equivalent circuit and is then entered as column 5 of the V-matrix. The entry +1 or -1 in  $\bar{V}(j)$  is best expressed as an algorithm in terms of vertices A and B.

Table 27-4

Choice of Entries for V-Matrix

E(i)	A(i)	B(i)	Is A in A(c)?	Is B in B(C)?	$\pm$
2	2	3	No	No	+
3	3	1	Yes	Yes	-
5	4	1	Yes	Yes	-
7	4	1	Yes	Yes	-
8	3	1	Yes	Yes	-

### Properties and Construction of W-Matrix

The number of columns with entries is equal to the number of  $G = 0$  elements in the equivalent circuit. Necessary data for construction are:

1. Entries A, B, and G in the problem statement (Table 27-1).
2. A definition of a cut-set as a single unknown  $G = 0$  element which can be expressed in terms of one or more  $G = 1$  elements on the basis of flow conservation through an imaginary closed surface.

3. An assignment of sign based on the direction of flow.

Analogous to the  $\bar{W}$ -matrix, two complementary sets exist:

1. Unknown currents:  $\bar{W} = (i | G(i) = 0)$ .
2. Known currents:  $W = (i | G(i) = 1)$ .

The set  $W$  will contain only current generators, while the set  $\bar{W}$  contains only voltage generators. A set of binary coded vectors is required to express the unknown currents in terms of only the knowns, as

$$\bar{W} = f(W)$$

To illustrate, consider column 9 in Table 27-1, which yields  $W(k) = (01101011)$ ,  $\bar{W}(j) = (10010100)$ , and the entries into the  $W$ -matrix  $W(j, k) = \bar{W}(j)$ , as listed.

### Sign Determinator in $W(j, k)$

Let  $A(\bar{W})$  be the set of vertex origins of the  $G = 0$  elements, and  $B(\bar{W})$  be the set of vertex terminations of these elements. In coded form from Table 27-1,  $A(\bar{W}) = (20030300)$  and  $B(\bar{W}) = (10040100)$ , where a "0" indicates a  $G = 0$  element. To reduce the length of the code, rewrite  $A(\bar{W}) = N(0110)$  and  $B(\bar{W}) = N(1001$  where  $N(0110)$

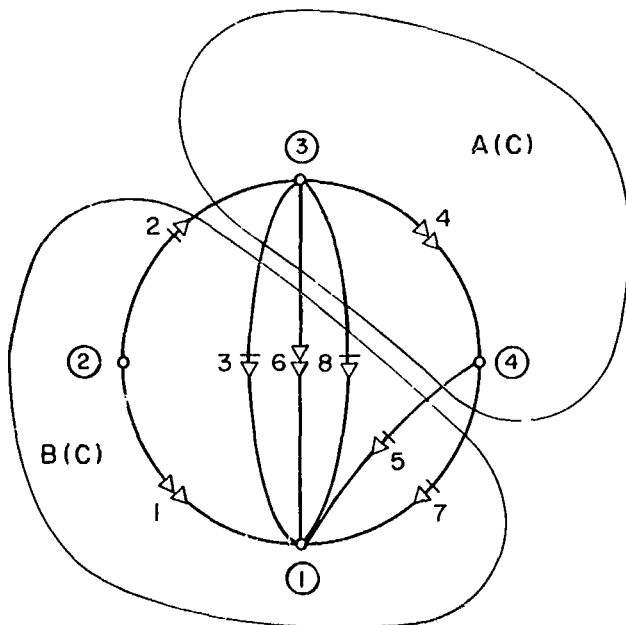


Figure 27-4—Separation of equivalent circuit into cut-set for the evaluation of  $I(6)$ .

is understood to be a set containing only vertices 2 and 3 of the four vertices in the equivalent circuit.

To determine the sign in  $W(6)$ , separate the vertices of the equivalent circuit, (Figure 27-4) into two complexes. Define complexes  $A(C)$  and  $B(C)$  as sets of vertices connected by  $\bar{W}$  elements, such that  $E(6)$  is the only  $\bar{W}$  element connecting the two complexes. From the problem statement Table 27-1  $A(6) = N(0010)$  and  $B(6) = N(1000)$ . Algorithms are formulated to identify all  $G = 0$  elements which are connected to  $A(6)$ : these are

$$A(C) = N(0011).$$

Similarly,

$$B(C) = N(1100).$$

To find all  $G = 1$  elements connecting  $A(C)$  and  $B(C)$ , connect vertex 3 or 4 in  $A(C)$  to vertex 1 or 2 in  $B(C)$ . The elements  $E(2)$ ,  $E(3)$ ,  $E(5)$ ,  $E(7)$  and  $E(8)$  meet this requirement and are listed in Table 27-4, with data on  $A$  and  $B$  from Table 27-1. It is then determined if  $A(1)$  is in  $A(C)$  for each  $E(i)$  and  $B(i)$  in  $B(C)$  as shown in Table 27-4. The result in code for  $E(6)$  is  $W(6) = (0+-0-0--)$  as entered in the  $W$ -matrix in Table 27-3.

Table 27-3 can be interpreted as:

$$I(6) = I(2) - I(3) - I(5) - I(7) - I(8).$$

The signs are then interpreted as the positive direction of current into  $A(C)$ , the reference direction for the unknown current  $I(6)$  being specified from  $A(C)$  to  $B(C)$ , or vertex  $A(6) = 3$  to vertex  $B(6) = 1$ . Similarly for  $W(4)$  from Table 27-1;

$$A(4) = N(0010) \quad \text{and} \quad B(4) = N(0001).$$

Thus

$$A(C) = N(1110) \quad \text{and} \quad B(C) = N(0001)$$

To find all  $G = 1$  elements connecting vertices 1, 2, or 3 in  $A(C)$ , to vertex 4 in  $B(C)$ , note that  $E(5)$  and  $E(7)$  meet this requirement; hence,  $W(4) = (0000+0+0)$ .

### T-Matrix

The  $T$  matrix describes the transmittances between the dichotomous variables current and voltage, as shown in Table 27-3.

If  $D \neq E$ , then  $E$  is a dependent source; if  $D = E$ , then  $E$  is a passive element. Four special cases occur:



1.  $C = 1, G = 0$  - the transmittance is an impedance  $Z$  or a current-controlled voltage generator.
2.  $C = 0, G = 1$  - the transmittance is an admittance  $Y$  or a voltage-controlled current generator.
3.  $C = 0, G = 0$  - the transmittance is a dimensionless quantity  $V$  relating the control and generator, or a voltage-controlled voltage generator.
4.  $C = 1, G = 1$  - the transmittance is a dimensionless quantity  $W$  relating the control and generator or a current-controlled current generator.

The case  $D = 0$  denotes that  $E$  is an independent source and is not considered here.

#### Closure of Open Graphs

An open system, Figure 27-5, contains strictly dependent and strictly independent variables. The flowgraph relates the variables  $X$  and  $Y$  by  $Y = GX$ , where  $G$  is the equivalent transmittance of the system. Closing the system by a "dummy" transmittance,  $T$ , the "independent" variable becomes  $G = 1/T$ , a function of the "dependent" variable  $X = TY$ . Assuming that any closed system is governed by a constraint,  $H = 0$ , which is dependent on the network topology and is referred to as the topology equation,  $H$  can be expanded in terms of any parameter,

$$H(T) = H(\bar{T}) + TH(T').$$

where  $H(\bar{T})$  is the part of  $H$  devoid of  $T$ , and  $H(T')$  is the part of  $H$  which contains  $T$ . We then solve this equation to obtain

$$T = -H(\bar{T})/H(T') = 1/G.$$

The variables  $X$  and  $Y$  are judiciously chosen. For example, to obtain current gain  $I_{out}/I_{in}$ , let  $Y = I_{out}$  and  $X = I_{in}$ , so that  $I_{out} = GI_{in}$ , where  $G$  represents the current gain.

Since present techniques of flowgraph evaluation are based on closed systems, it is necessary

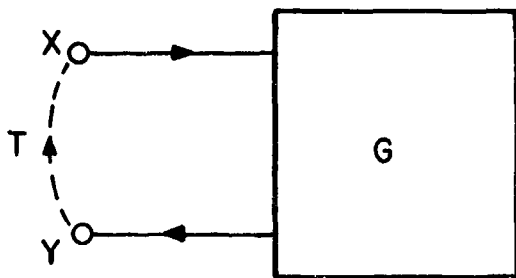


Figure 27-5—Closed system representation,  
 $Y = GX, X = TY$ .

to specify the problem in terms of an unknown parameter,  $T = X/Y$ , flagged by the  $H$  tag in the problem formulation. For example, from Table 27-1,  $H(8) = 1$ , while  $H(i) = 0$  for  $i \neq 8$ . The unknown tagged parameter is included in the flowgraph. No special algorithms are needed for processing it, provided the unknown is always treated as a transmittance associated with an element, and not as a transmittance associated with a constraint due to interconnections.

## Examples of Computer Runs

Two further examples are presented, to illustrate the problem statement, including tagging of the unknown parameter; construction of flowgraph, including the closing parameter; numerical value in appropriate form for future processing.

Figure 27-6 shows the equivalent circuit of a transistorized band-pass amplifier coded for  $1/T = V_{(out)} / I_{(in)}$ , with Figure 27-7 the coded equivalent circuit. Table 27-5 gives the problem statement and Table 27-6, the computer printout, from which the flowgraph in Figure 27-8 is constructed.

The band-pass lossy ladder in Figures 27-9 and 27-10 and Table 27-7 is coded for  $V_{(out)} / I_{(in)}$ . Table 27-8 and Figure 27-11 exhibit the computer printout of the associated flowgraph.

Copies of this computer program have been qualified and are available at a nominal charge through project COSMIC, University of Georgia (Reference 7).

## CONCLUSIONS

The algorithms presented provide a firm interface between the circuit designer and the mathematician for computer-oriented modelling of integrated circuits. Although the algorithms were written for linear networks, the approach is completely general and can easily be extended to nonlinear networks.

## REFERENCES

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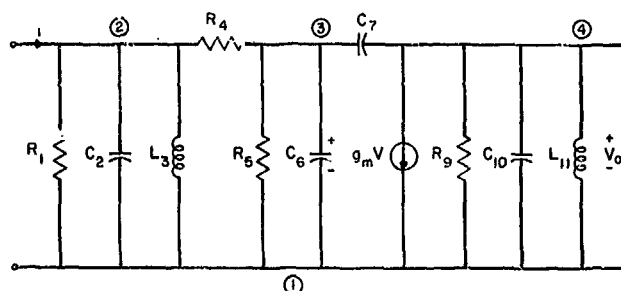


Figure 27-6—Band-pass amplifier equivalent circuit.

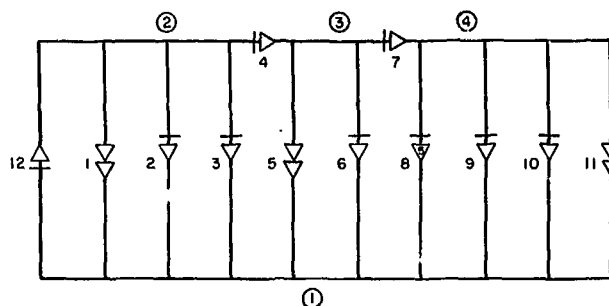


Figure 27-7—Coded equivalent circuit showing dichotomy.

Table 27-5

Problem Statement for Band-Pass Amplifier  
(Figure 27-6)

A	B	C	D	E	F	G	H	Numerical
2	1	1	1	1	0	0	0	.500 E+2
2	1	0	2	2	1	1	0	.400 E-5
2	1	0	3	3	2	1	0	.250 E-4
2	3	0	4	4	0	1	0	.500 E+2
3	1	1	5	5	0	0	0	.500 E+2
3	1	0	6	6	1	1	0	.200 E-8
3	4	0	7	7	1	1	0	.500 E-11
4	1	0	8	8	0	1	0	.500 E+2
4	1	0	9	9	0	1	0	.400 E+4
4	1	0	10	10	1	1	0	.100 E-8
4	1	1	11	11	2	0	0	.100 E-2
1	2	0	11	12	0	1	0	.100 E+1

Table 27-6

Computer Output for Flowgraph Construction

V	1	2	3	4	5	6	7	8	9	10	11	12	W	1	2	3	4	5	6	7	8	9	10	11	12	T	1	2	3	4	5	6	7	8	9	10	11	12			
1	+	+	+									+	1													1	Z														
2													2	-												2	Y														
3													3	-												3		Y													
4													4	-			+									4			Y												
5				-		+	+						5													5				Z				Z							
6													6				-									6					Y										
7													7				-						+			7						Y									
8													8										-			8															
9													9										-			9									Y						
10													10										-			10										Y					
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12													12	+												12															

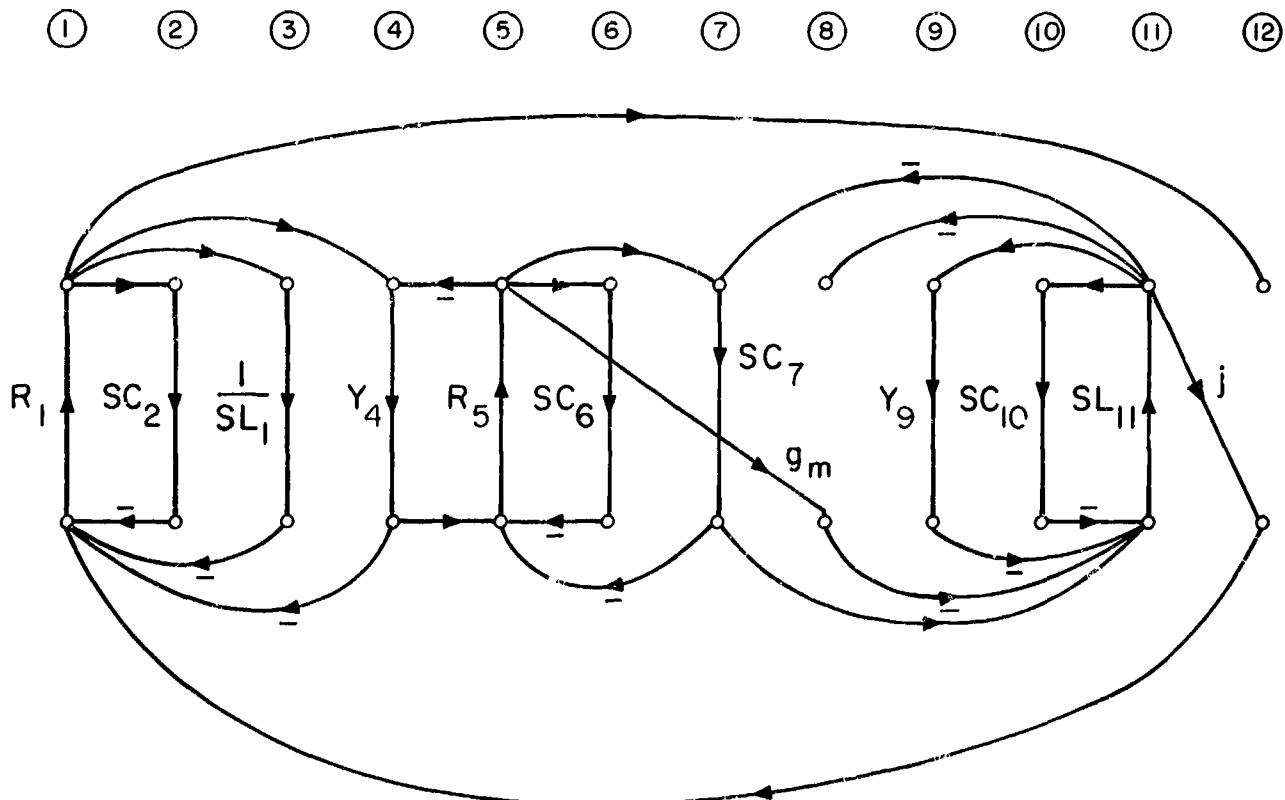
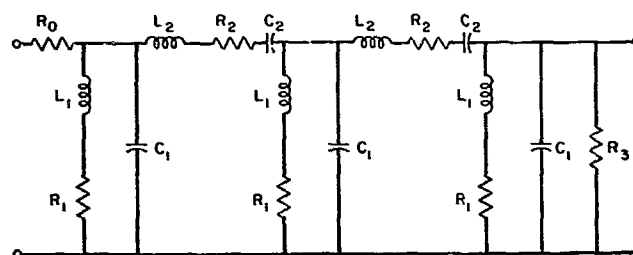


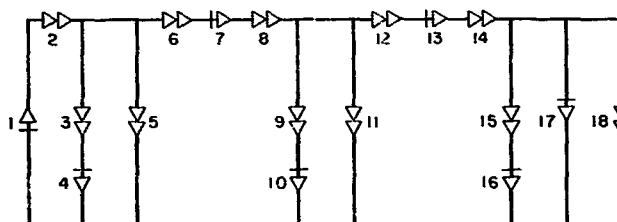
Figure 27-8—Flowgraph constructed from computer output V, W, and T matrices.

### Problem Statement for Band-Pass Lossy Ladder (Figure 27-9)

A	B	C	D	E	F	G	H	K	Numerical
1	2	0	18	1	0	1	1	1	.000 E+0
2	3	1	2	2	0	0	0	0	.500 E+2
3	12	1	3	3	1	0	0	0	.500 E-1
12	1	0	4	4	0	1	0	0	.100 E+2
3	1	1	5	5	2	0	0	0	.250 E-4
3	5	1	6	6	1	0	0	0	.250 E-1
5	6	0	7	7	0	1	0	0	.250 E+2
6	7	1	8	8	2	0	0	0	.100 E-4
7	13	1	9	9	1	0	0	0	.500 E-4
13	1	0	10	10	0	1	0	0	.100 E+2
7	1	1	11	11	2	0	0	0	.250 E-4
7	9	1	12	12	1	0	0	0	.250 E-1
9	10	0	13	13	0	1	0	0	.250 E+2
10	11	1	14	14	2	0	0	0	.100 E-4
11	14	1	15	15	1	0	0	0	.500 E-1
14	1	0	16	16	0	1	0	0	.100 E+2
11	1	0	17	17	1	1	0	0	.250 E-4
11	1	1	18	18	0	0	0	0	.100 E+2



**Figure 27-9—Band-pass lossy ladder.**



**Figure 27-10—Equivalent circuit coded for flowgraph construction.**

### Computer Printout for Flowgraph Construction

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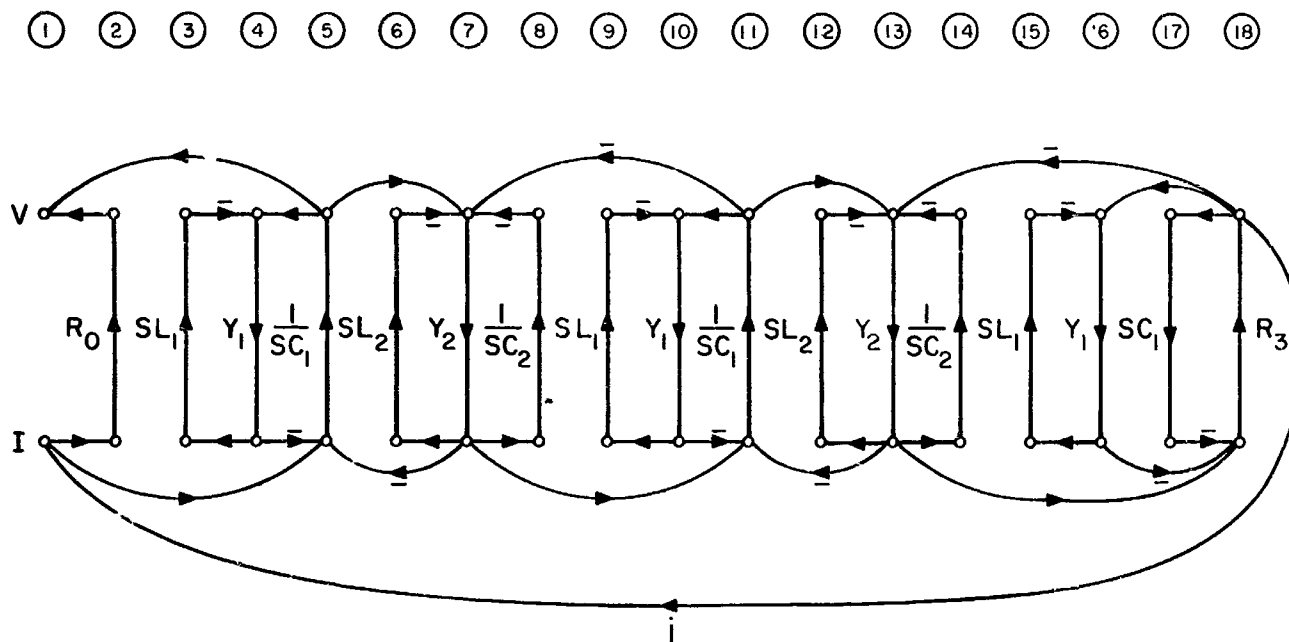


Figure 27-11—Flowgraph constructed from computer output.

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## **28. MICROCIRCUIT APPLICATIONS IN THE APOLLO TV CAMERA**

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Circuit design approaches to obtain 80 percent utilization of microcircuits in the Apollo TV Camera are presented. A universal microcircuit breadboard functional block is described. Application problems are indicated along with final microcircuit design details. Certain aspects of the Quality Control and Reliability Programs, as applied to new microcircuit designs used in the camera, are discussed with emphasis on practical considerations.

### **INTRODUCTION**

The Apollo TV camera is to be utilized throughout the Apollo mission, including operation on the Lunar surface. Requirements include: minimum weight, size, power, and maximum reliability. Because of these requirements, a maximum utilization of microcircuits was directed. The approaches taken in microminiaturizing the camera, the resulting circuits, problem areas, and some aspects of the Reliability and Quality Control Program are presented.

### **DEVELOPMENTAL CYCLE**

The development cycle included breadboarding the system in discrete component form and determining which functional blocks could be placed in microcircuit form. Some microcircuit blocks could be obtained as "off the shelf" items and some would have to be custom designed blocks. Since a large number of custom blocks was required, a universal block microcircuit breadboard approach was utilized. This approach analyzed the circuit parameters of each functional area. The analysis establishes the requirements for a general purpose functional block.

The block developed for this program is known as CLEM (Composite for Lunar Excursion Module). CLEM is a monolithic chip, fabricated with the planar epitaxial process. It is composed of ten transistors of four types, six diode clusters, and 18 tapped diffused resistors ranging in value from 110 kohms to 50 ohms. In the microcircuit breadboard form, different circuits are obtained by various arrangements of flying lead interconnections. Twenty-three circuits of the TV

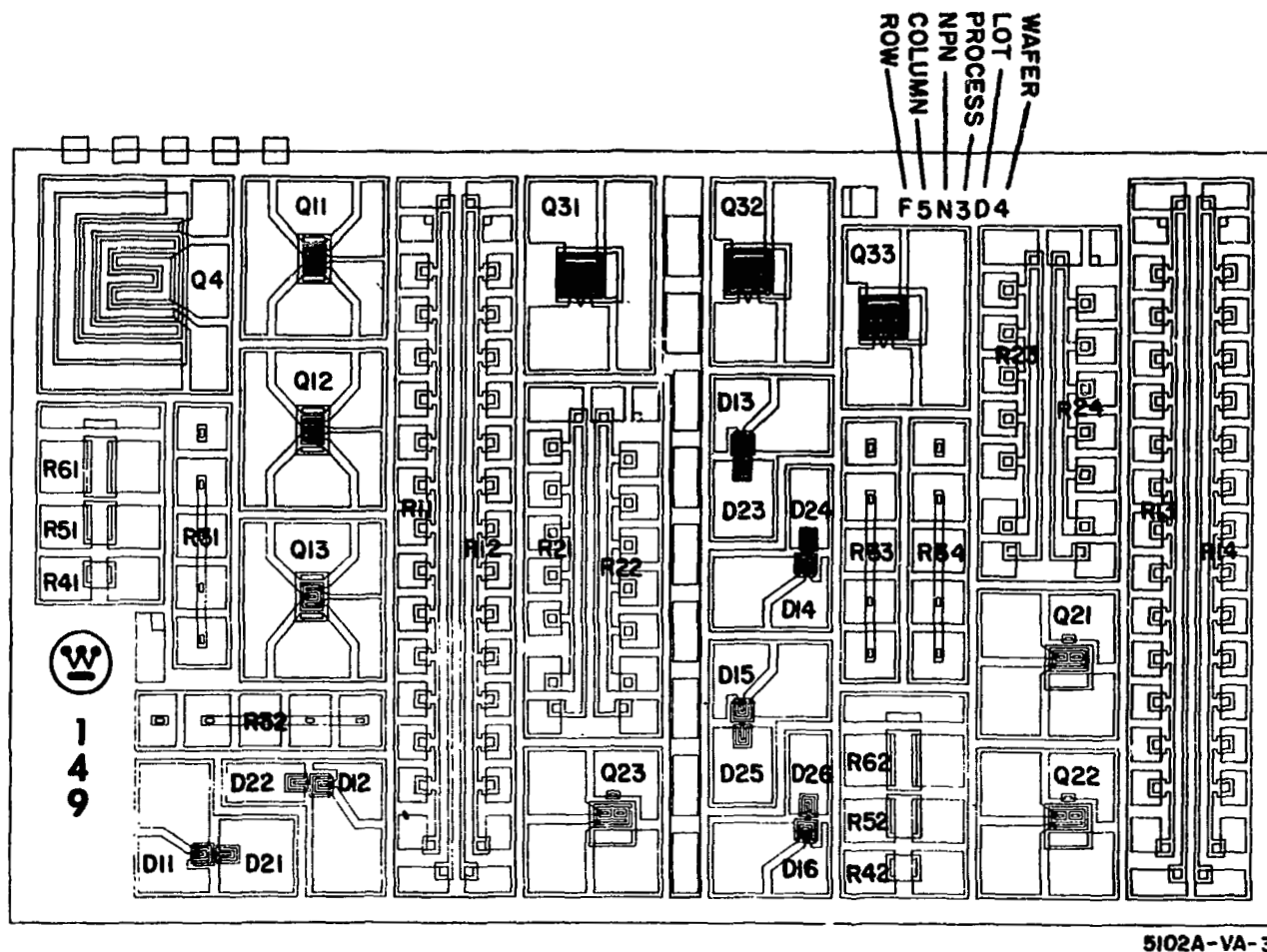


Figure 28-1— General purpose CLEM breadboard topology indicating various regions on the block.

camera are breadboarded using CLEM. This block is detailed in References 1 and 2 and Figures 28-1 and 28-2.

CLEM was used to develop a complete microcircuit breadboard for the camera. This development cycle phase was a set of specifications defining the required microcircuit blocks. Following the development of the breadboard, surveys of industry were conducted to obtain suppliers. This was necessary due to the lack of capacity at Westinghouse Solid State Laboratory where the CLEM's were developed. The problem of obtaining suppliers resulted for the following reasons:

1. A small quantity was required.
2. Quality Control and Reliability provisions and practices of many suppliers were deficient; if not throughout their facility, at least in the areas where the item would be fabricated.
3. Technological capability in the silicon monolithic block was not adequate.

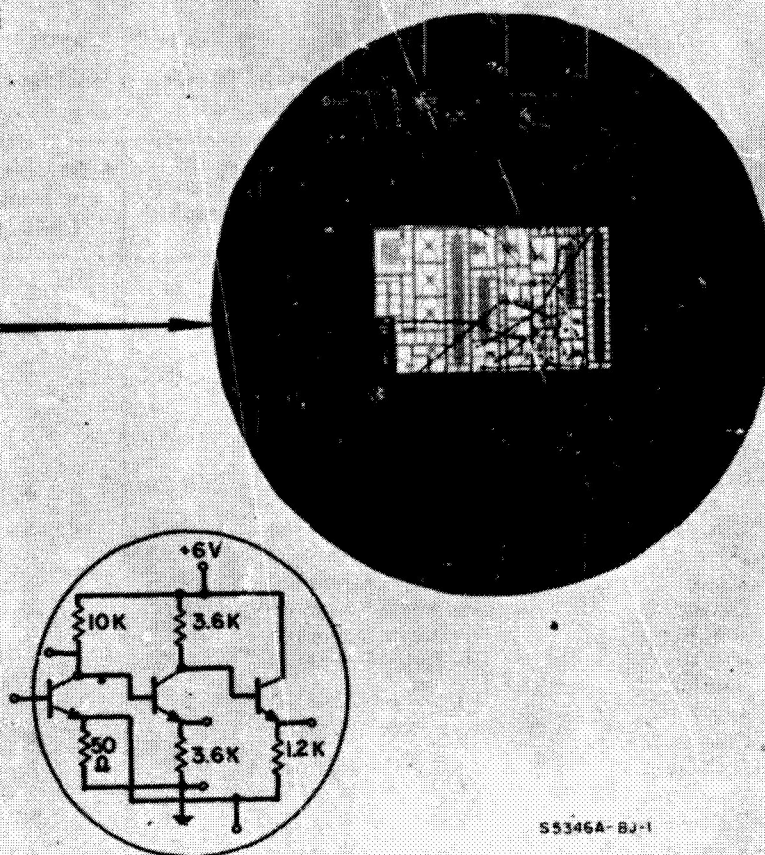


## LEM TV CAMERA CIRCUITS BREADBOARDED WITH CLEM

OPERATING ON POWER SUPPLIES  
-8 V, +6V, +25 V

ALC DETECTOR  
ALC DRIVER  
CORRECTION NETWORKS  
AGC ATTENUATOR  
LINEAR PRE-AMPLIFIER  
POST AMPLIFIER NO. 1  
POST AMPLIFIER NO. 2  
OSCILLATOR-AMPLIFIER  
BLANK DRIVER  
MIXER  
SAW TOOTH GENERATORS  
DIFFERENTIAL AMPLIFIERS  
OUTPUT DRIVERS  
MULTIVIBRATORS  
INVERTER DRIVERS  
LINE REGULATORS  
LINE SWITCHES  
VOLTAGE REGULATORS

## TYPICAL CLEM BREADBOARD



SS346A-BJ-1

Figure 28-2—Lem TV camera circuits breadboarded with CLEM.

Utilization of "off the shelf" operational amplifiers was not successful due to specifications of the various blocks. The design includes one standard operational amplifier. Utilization of many outboard components would have enabled the use of standard operational amplifiers; however, volume restrictions prevented this.

As a result of these problems, a determination of functional blocks suitable for implementation in the thin film hybrid form was made. This enlarged the availability of suppliers. The final selection of suppliers was based on technological capability, Reliability and Quality Control programs and practices, and management attitude. The suppliers are indicated in Table 28-1. Considerable and conscientious effort in selecting suppliers was not infallible, as indicated by the following problem. Amelco was the supplier of nine thin film hybrid circuits using sputtered tantalum thin film technology. The determination of technological capability was based on products of the engineering development laboratory. When this technology was transferred to a production line to obtain the desired quantity, many of the process skills were lost. Consequently, a serious cost and schedule impact was experienced.

Delivery of production microcircuits enabled completion of five TV cameras to date. Micro-miniaturizing the camera is considered successful in that only two transistors originally in micro-circuit form are now discrete.

Table 28-1

Lunar TV Camera  
Microelectronic Devices -- Testing Schedule Summary

Circuit description	Camera subsystem	Manuf.	Fab. (1) tech.	Safety margin verification tests (2)	Preconditioning, power age and screening (3)	Group A tests (4)	Group B tests (5)
Flip-flop	Sync	Signetics	M	X	X	X	X
Triple nand gate	Sync	Signetics	M	X	X	X	
Quad nand gate	Sync	Raytheon	M	X	X	X	X
Schmitt trigger	Sync	WMED	M	X	X	X	
Sawtooth gen	Sweep	Amelco	TFH	X	X	X	
Diff amp.	Sweep	Amelco	TFH	X	X	X	X
Driver	Sweep	Amelco	TFH	X	X	X	
Mixer	Video	Amelco	TFH	X	X	X	
Driver/inv.	Pwr.sup.	Amelco	TFH	X	X	X	
+6V Reg.	Pwr.sup.	Amelco	TFH	X	X	X	
-8V Reg.	Pwr.sup.	Amelco	TFH	X	X	X	
Astable multi	Pwr.sup.	Amelco	TFH	X	X	X	
Line reg.	Pwr.sup.	Amelco	TFH	X	X	X	X
D.C. amp.	ALC	Fairchild	M	X	X	X	X
Video amp. #1	Video	W AERO	M	X	X	X	
Video amp. #2	Video	W AERO	M	X	X	X	
Video amp. #3	Video	W AERO	M	X	X	X	
Amplifier-OSC.	Sync	W AERO	M	X	X	X	
Detector	ALC	W AERO	M	X	X	X	X
ALC/BLNK driver	Video/ Sync	W AERO	M	X	X	X	
Corr. net #1	ALC	W AERO	M	X	X	X	
Corr. net #2	ALC	W AERO	M	X	X	X	
Volt. att.	AGC	W AERO	HM	X	X	X	X

## NOTES:

- (1) M -- monolithic; TFH -- thin film hybrid  
HM -- hybrid monolithic
- (2) Safety Margin Verification Tests consist of sample testing select devices to the preconditioning, power aging and screening requirements, plus the following environmental stress tests: shock, vibration, centrifuge, temperature cycling, and power age step stress.
- (3) Preconditioning, Power Age, and Screening consists of the 100% processing of the integrated circuits to double pre-seal visual inspection, high temperature bake, temperature cycling, centrifuge, hermetic seal tests, x-ray, electrical screening, pre-power age electrical tests, power aging, and post-power age electrical tests.
- (4) Group A Electrical Tests consists of the 100% testing of I/C's to the electrical performance tests over the temperature range -55°C to +125°C.
- (5) Group B Environmental Inspection and Stress Testing consist of sample testing to various mechanical and thermal stress levels in addition to long term (1500 hour) high temperature operation life.

## TYPES OF CIRCUITS

The TV camera requires a wide range of circuits, digital and analog. Referring to the Block Diagram, Figure 28-3, the functional blocks are sectionalized as follows:

## Video Section

The video section contains three video amplification blocks, having similar characteristics, utilizing three transistors of the 2N2484 type ( $h_{fe} = 300$  min) and resistor values ranging from 100 ohms  $\pm$  20 percent to 68 kohms  $\pm$  20 percent. Resistor ratios are held to nominal value  $\pm$  7.5 percent. See Figure 28-4. Also included is a mixer required to mix picture video and sync signals. This block is characterized by resistor values ranging from 100 ohms  $\pm$  2 percent to 2.7 kohms  $\pm$  10 percent and the use of transistors of the 2N2907 and 2N2369A type as well as a FET, 2N3436. This block was implemented in the thin film hybrid form using thin film resistor networks and chip transistors. See Figure 28-5.

## AGC/ALC Section

The AGC/ALC section, providing automatic gain and light level control for the camera, contains a dc amplifier detector, ALC blank driver, correction networks, and a voltage controlled

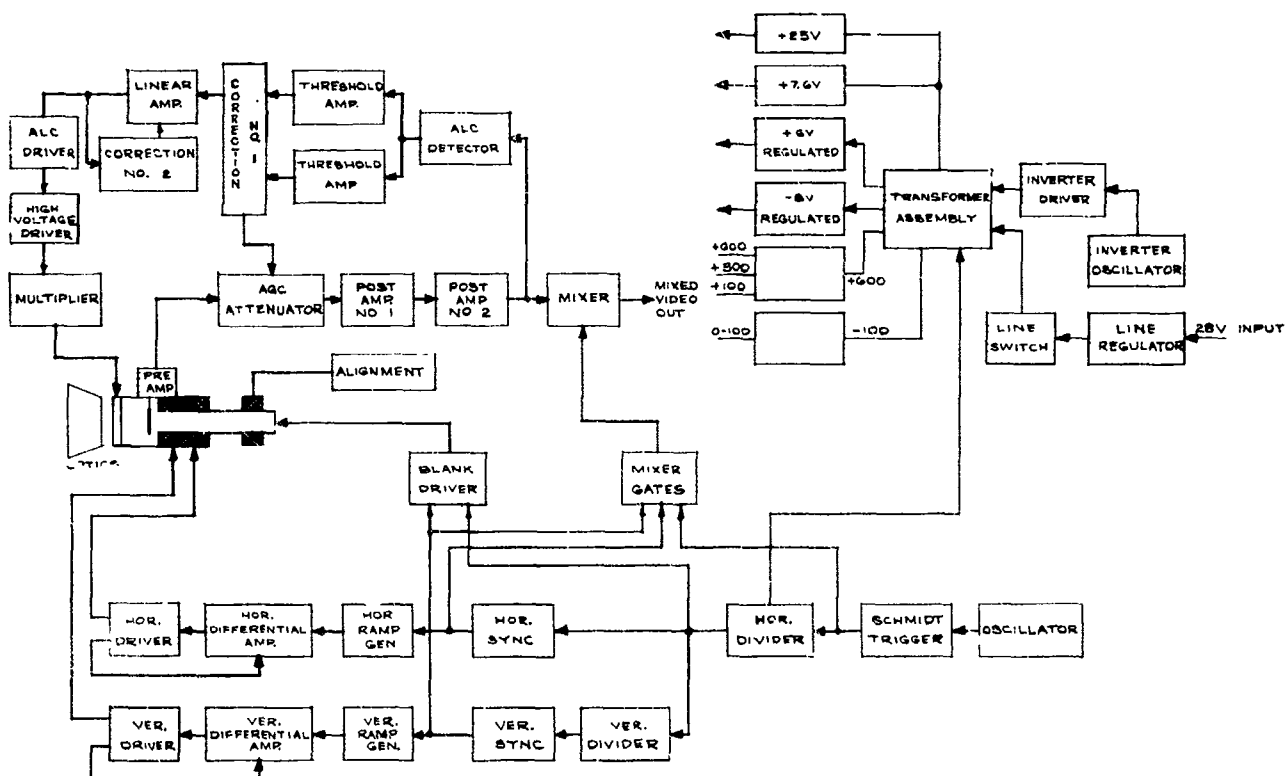


Figure 28-3—Block diagram.

Power rating = 200 mw  
 Supply voltage = +10 or +20 VDC  
 Output DC levels = 0.0 to 4.5 VDC  
 Output swing = 0.5 to 6.0 VPP  
 Voltage gain = 7.4 to 12.9  
 Frequency response = 1.5 cps to 700 KCPS

$Q_1, Q_2, Q_3 = 2N2484$

	Pre Amp	Post Amp #1	Post Amp #2
$R_1$	30K ohms	10K ohms	10K ohms
$R_2$	1.8K ohms	3.6K ohms	3.6K ohms
$R_3$	700 ohms	1.2K ohms	1.2K ohms
$R_4$	100 ohms	100 ohms	100 ohms
$R_5$	3.6K ohms	3.6K ohms	1.8K ohms
$R_6$			68K ohms
$R_7$			51K ohms
$D_1$			1N914

$R_2/R_5, R_3/R_4, R_6/R_7 = \text{nominal} \pm 7.5\%$   
 All resistors  $\pm 20\%$

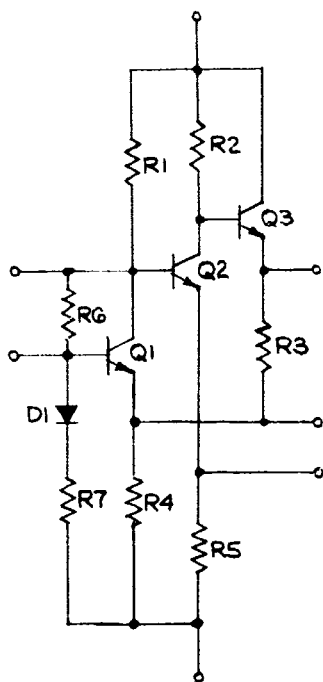


Figure 28-4—Video amplifier.

attenuator. The dc amplifier is a 702A type Fairchild operational amplifier. The detector has resistor values ranging from 1 kohm to 62 kohms, utilizing six diodes of the 1N914 type and two transistors of the 2N708 type. The correction networks are resistor-diode networks with 13 resistors ranging from 110 ohms to 68 kohms and nine diodes of the 1N914 type.

Power rating = 1.36 w  
 Supply voltage =  $\pm 20$  VDC, + 10 VDC  
 Input/Output current = 20 MADC  
 Voltage gain @  $f = 500$  KCPS = 0.5 min  
 Output voltage swing = 2.5 VPP  
 Amplitude distortion =  $\pm 2.0\%$

$Q_1, Q_3, Q_5 = 2N2907$   
 $Q_2 = 2N3436$   
 $Q_4 = 2N2369A$   
 $R_1 = 860 \text{ ohms} \pm 10\%$   
 $R_2 = 1.4K \pm 10\%$   
 $R_3 = 3.2K \pm 10\%$   
 $R_4, R_8 = 910 \text{ ohms} \pm 10\%$   
 $R_5 = 5.1K \pm 10\%$   
 $R_6, R_9 = 1K \pm 10\%$   
 $R_7 = 2.7K \pm 10\%$   
 $R_{10} = 100 \text{ ohms} \pm 2\%$   
 $D_1 = 1N914$

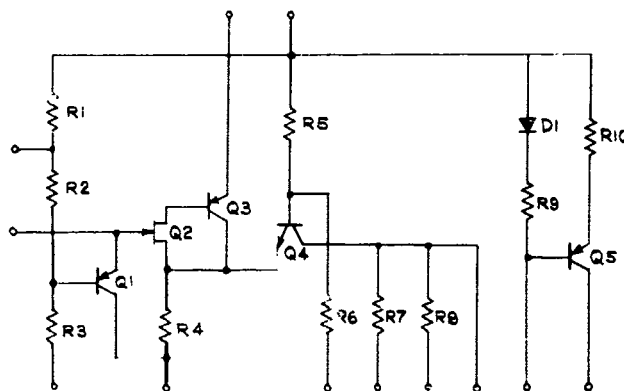


Figure 28-5—Mixer.

Power rating = 400 mw  
 Supply voltage =  $\pm 10$  VDC  
 Input voltage =  $\pm 10$  VDC  
 Output voltage = +10 to -0.5 VDC

DC Voltage Levels ( $V_{in}$ )

$V_{in}$					2VPP	2.5VPP	3VPP	4VPP
Point	$V_1$	$V_4$	$V_5$	$V_8$	$V_5$	$V_5$	$V_5$	$V_5$
Min	0.8	0.8	0.4	2.0	+0.44	-0.11	-0.39	-0.4
Max	1.1	1.1	0.5	2.5	+0.46	-0.44	-0.42	-0.44
$R_1, R_7 = 2K$				$R_5 = 2.4K$				
$R_2 = 7.5K$				$R_6 = 1K$				
$R_3 = 62K$				$D_1$ through $D_7 = 1N914$				
$R_4 = 2.5K$				$Q_1, Q_2 = 2N708$				

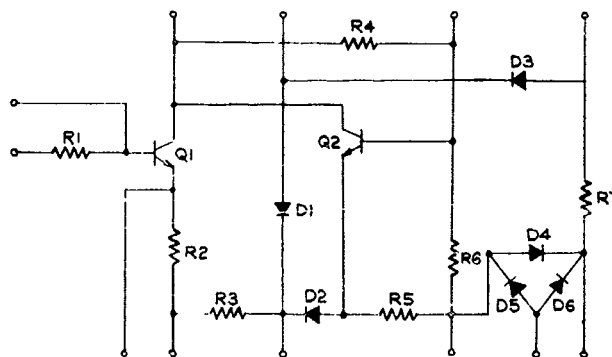


Figure 28-6—ALC detector.

Power rating = 400 mw  
 Output current vs. input voltage = 1.8 to 3.0  $\mu$ ADC @ 0.5 VDC,  
 7.0 to 9.0  $\mu$ ADC @ 2.0 VDC, 10.0 to 14.0  $\mu$ ADC @ +2.5 VDC

$R_1$ = 62K	$R_{10}$ = 620 ohms
$R_2$ = 12K	$R_{11}$ = 220 ohms
$R_3$ = 2.2K	$R_{12}$ = 110 ohms
$R_4, R_9$ = 7.5K	$R_{13}$ = 680 ohms
$R_5, R_8$ = 5.6K	$D_1$ through $D_9$ = 1N914
$R_6, R_7$ = 3.9K	

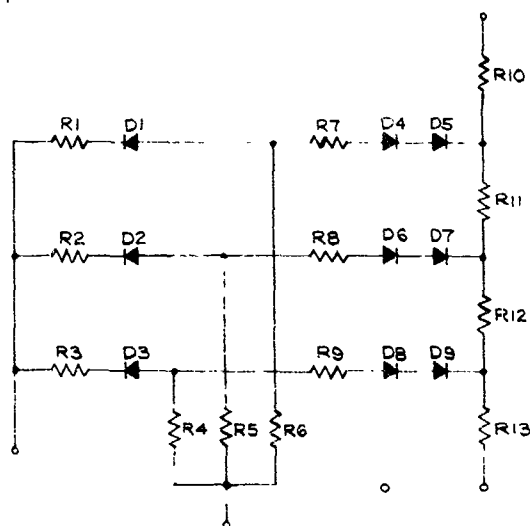


Figure 28-7—Correction network.

Power rating = 400 mw  
 Supply voltage = +30 VDC  
 Input voltage =  $\pm 10$  VDC  
 Output voltage levels = 0 to 17 VDC  
 Output voltage swing = 0.2 to 20.2 VPP  
 Switching times =  $T_r$  = 400 NS,  $T_f$  = 300 NS

$R_1$ = 20K	$D_1$ = 1N914
$R_2$ = 8.2K	$Q_1, Q_2$ = 2N3043
$R_3$ = 3.9K	
$R_4$ = 10K	
$R_5$ = 13K	
$R_6$ = 47 ohms	
$R_7$ = 27	

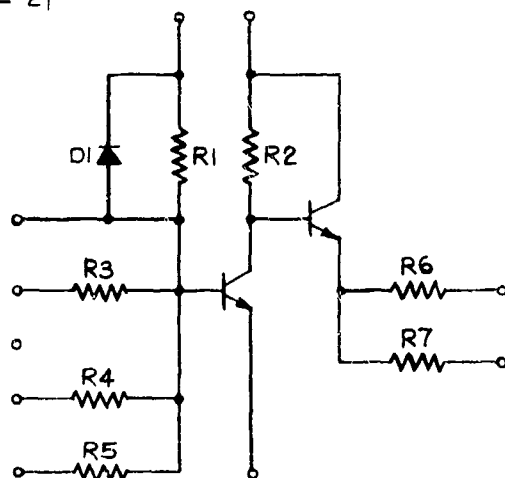


Figure 28-8—ALC/blank driver.

The voltage controlled attenuator is a planar epitaxial silicon monolith composed of four resistors, two transistors of the 2N2906 type, and two diodes of the 1N914 type. The ALC blank driver contains seven resistors ranging from 47 ohms to 20 kohms, one diode, and two transistors of the 2N3043 type. These circuits are fabricated as planar epitaxial silicon monoliths. See Figures 28-6, 28-7 and 28-8.

### Power Supply Section

The power supply section contains a driver/inverter, +6 volt and -8 volt regulators, a stable multi, and a line regulator which are fabricated in the thin film hybrid form using thin film passive networks and discrete transistor chips. The line regulator is most complex, requiring 24 components. Resistor values are held to  $\pm 3$  percent and resistor ratio tracking to  $\pm 0.5$  percent over the temperature range. See Figures 28-9 through 28-12.

### Sweep Section

The sweep section contains a sawtooth generator, differential amplifier, and deflection driver. These circuits are fabricated in thin film hybrid form. The deflection driver has resistors ranging down to 10 ohms. Two of the 10-ohm resistors are matched within  $\pm 2$  percent. See Figures 28-13, 28-14, and 28-15.

### Sync Section

The sync section utilizes the Signetics line of logic with the exception of the oscillator amplifier which is a portion of the crystal controlled clock, a NAND gate from Raytheon, and a Schmitt trigger from Westinghouse MED.

The oscillator amplifier is a planar epitaxial silicon monolith detailed in Figure 28-16.

Of the custom circuits mentioned above, those fabricated in planar epitaxial silicon monolithic form were converted to final production form maintaining the basic layout and characteristics of the CLEM block. While conversion from microcircuit breadboard to final configuration required new artwork and masks, many process parameters were retained. Electrical characteristics of the breadboard were easily duplicated resulting in time and cost savings. A further cost and schedule reduction was obtained in reduced specification preparation. A more detailed and explicit specification was required for circuits converted from CLEM to thin film hybrid form.

Power rating = 1.36 w  
 Supply voltage = 50 VDC  
 Input voltages = +10,  $\pm 15$ , +10 VDC  
 Output voltages = 0.3 to 35.8 VDC  
 Switching times =  $T_r$ ,  $T_f$  = 1.0  $\mu$ s  
 Input current = 0.62 to 0.96 mADC  
 $R_1, R_2, R_7, R_8$  =  $4K \pm 20\%$   
 $R_3, R_6$  =  $9K \pm 20\%$   
 $R_4, R_5$  =  $6K \pm 20\%$   
 $C_1$  =  $25pf \pm 20\%$ , 50 VDC  
 $D_1$  through  $D_8$  = 1N914  
 $Q_1, Q_2$  = 2N915

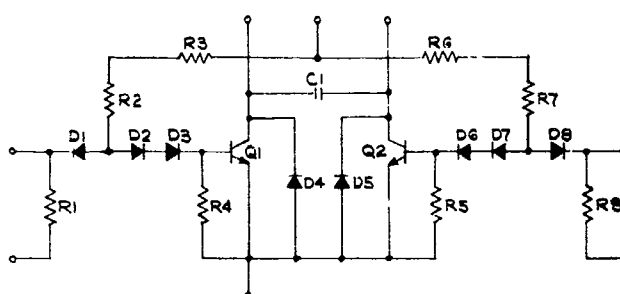


Figure 28-9—Driver inverter gate.

## RELIABILITY AND QUALITY CONTROL

The design, manufacture, and test of the microcircuits are marked by a comprehensive Reliability and Quality Control Program. Design is characterized by proper circuit operation over the temperature range from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Manufacture is marked by a complete specification, tight control of each process step, numerous test and inspection points throughout the fabrication cycle, and complete documentation of each step. A testing program assuring quality and reliability is summarized by Table 28-1. While detailed specifications screened out defective parts to a large extent, the reliability and quality indoctrination program has been effective also. This is noticeable in inspection areas of subjective judgement. An attitude has been developed which is "When in doubt, reject."

## CONCLUSION

The most significant aspect of this program was the development and utilization of the CLEM. This microcircuit breadboard was useful in the developmental and production stages of the program. In addition, at least one other program has been able to make use of this microcircuit. This was an Air Force development of a multichannel personal communications system which utilized CLEM. The technique appears to be the most economical way to microminiaturize a system requiring a variety of analog functional blocks.

Power rating = 1.36 W

Supply voltage = +36 VDC

Output voltages = 12.15 to 13.45, 8.07 to 8.93 and 3.7 VDC

Switching times = ( $t_r = 0.5$  to  $2.5 \mu s$ ) ( $t_f = 0.5$  to  $1.4 \mu s$ )

$C_1 = 82 \text{ pf}$   
 $C_2 = 270 \text{ pf} \quad \pm 10\% @ 50 \text{ V}$   
 $C_3 = 47 \text{ pf}$

$D_1 = \text{1r 4868}$

$R_1 = 10 \text{ ohms} \quad \pm 5\%$

$R_2 = 33 \text{ ohms}$

$R_4 = 1K$

$R_5, R_{10} = 14K \quad \pm 3\%$

$R_6 = 50K$

$R_7 = 5K \pm 10\%$

$R_{11} = 23.2K \pm 5\%$

$R_{14} = 13K$

$R_{15} = 20K \quad \pm 5\%$

$Q_1 = 2N2907A \quad Q_2, Q_3, Q_4, Q_5 = 2N2903$

$R_3 = 24K \pm 10\%$

$$\frac{R_5 + R_6}{R_5 + R_6 + R_{10}} = 0.821 \pm 0.017 (\pm 1\% \text{ tracking})$$

$$\frac{R_5}{R_5 + R_6 + R_{10}} = 0.042 \pm 0.013 (\pm 1\% \text{ tracking})$$

$R_8 = 50.4K \pm 5\% \quad R_9 = 28.7K \pm 3\%$

$R_{12} = 20K \pm 3\% \quad R_{13} = 12K \pm 5\%$

$$\frac{R_{14}}{R_{14} + R_{15}} = 0.394 \pm .008 (\pm 0.5\% \text{ tracking})$$

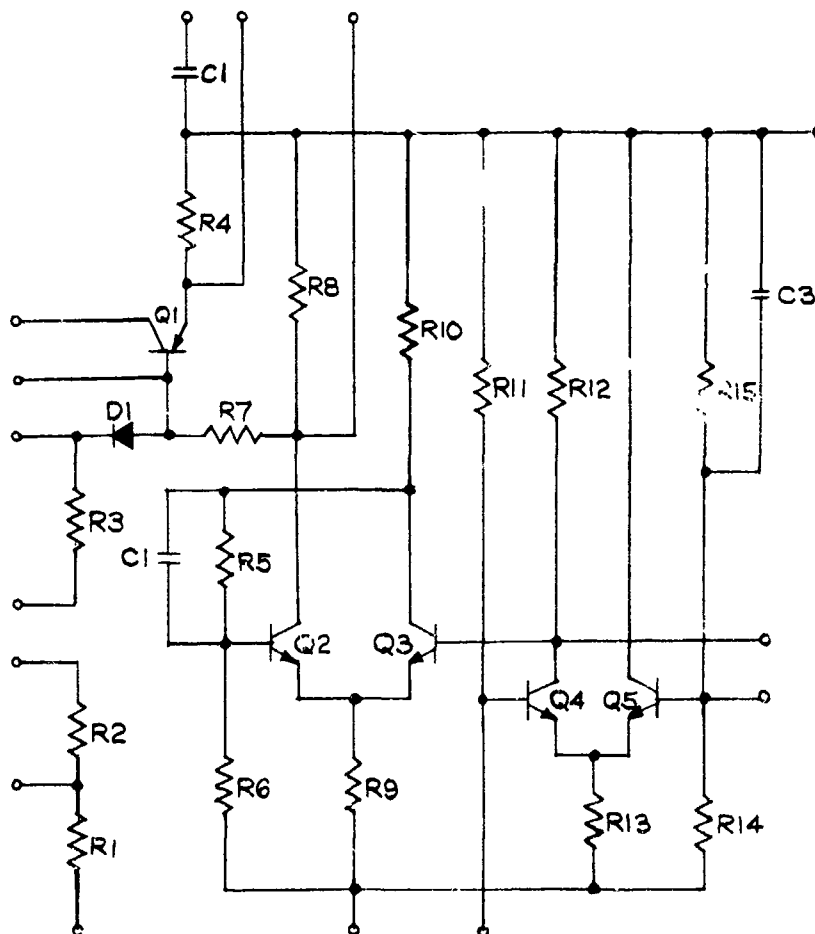


Figure 28-10—Line regulator.

Power rating = 1.36 w  
 Load current = 140 MADC  
 Differential voltage = 20 MVDC max.  
 Input voltage = 7.87 to 8.13 VDC  
 Load regulation = 0.13%  
 Line regulation = 0.15%  
 Ripple rejection = 0.05  
 $Q_1 = 2N2906A$   $Q_2, Q_3 = 2N2903$   
 $R_1 = 1.2K \pm 5\%$  track to  $\pm 100$  PPM/°C  
 $R_2 = 91\Omega$  ohms  $\pm 5\%$   
 $R_3 = 5K$   $R_4 = 10K$   
 $R_5, R_6 = 3K \pm 5\%$  track to  $\pm 100$  PPM/°C  
 $R_7 = 1K$   $R_8 = 680$  ohms  
 $R_9 = 82K$   $R_{10} = 160$  ohms  
 $D_1 = 1N753$   $C_1 = 100pf$

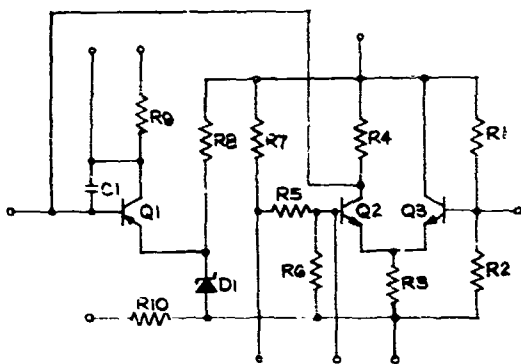


Figure 28-11— -8 volt regulator.

Power rating = 1.36 w  
 Sawtooth amplitude = 0. VPP to 2.5 VPP/Varies with sweep rate  
 Linearity =  $\pm 1\%$  maximum  
 $C_1, C_2 = 200$  p  $\pm 20\%$   
 $D_1$  through  $D_4 = 1N914$   
 $R_1, R_3 = 5.1K$  ohms  $Q_1 = 2N2904$   
 $R_2 = 1.5K$  ohms  $Q_2 = 2N2219$   
 $R_4 = 30K$  ohms  $Q_3 = 2N2484$   
 $R_5 = 2.4K$  ohms  
 $R_6 = 20K$  ohms  $TC \approx -200$  PPM/°C  
 $R_7 = 14.4K$  ohms  $\pm 3\%$   
 $R_8 = 4.7K$  ohms  $\pm 5\%$

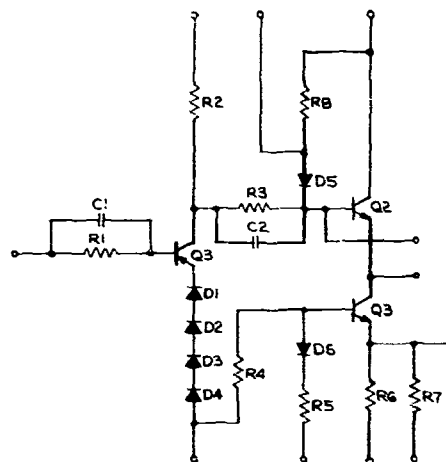


Figure 28-13—Sawtooth generator.

Power rating = 1.3 w  
 Power supply voltage = +40, -15VDC  
 Load current = 1.5 MADC  
 Zener voltage  $V_Z = 13.5$  to 18.5 VDC  
 No load output voltage = 5.94 to 6.00 VDC  
 Load regulation =  $\pm 0.20\%$   
 Line regulation =  $\pm 0.10\%$  and  $\pm 1.2\%$   
 Ripple rejection = 0.002  
 $Q_1 = 2N2822A$   $Q_2, Q_3 = 2N2903$   
 $R_1 = 2K \pm 5\%$   
 $R_2 = 18K$   
 $R_3, R_5 = 6K$   
 $R_4 = 4K$   
 $R_6 = 3.4K$   
 $R_7, R_8 = 50$   
 $R_9 = 7.5K$   
 $R_{10} = 14K$   
 $D_1 = 1N966B$   
 $D_2 = 1N914$

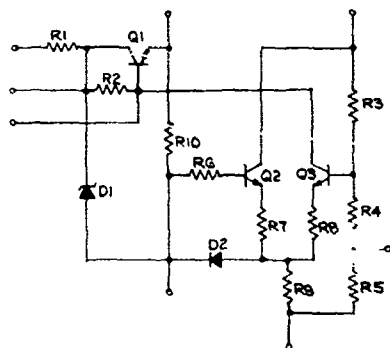


Figure 28-12— +6 volt regulator.

Power rating = 1.36 w  
 Voltage gain = 15 to 120  
 Voltage gain ratio = 0.75  
 Frequency response = 250K CPS  
 Undistorted output voltage = 1.4 VPP  
 on voltage  $Q_p = 0.15$  to 0.35 VDC,  $h_{fe}$ ,  $Q_{10}$  = 100 min.  
 $C_1 = 27$  pf  
 $C_2 = 600$  pf  
 $R_1 = 120$  K  $\pm 10\%$   
 $R_2 = 82K$   
 $R_3, R_4 = 3K \pm 5\%$   
 $R_5, R_6 = 10K \pm 5\%$   
 $Q_1, Q_2 = 2N2907$   
 $Q_3 = 2N2219$   
 $Q_4 = 2N2484$

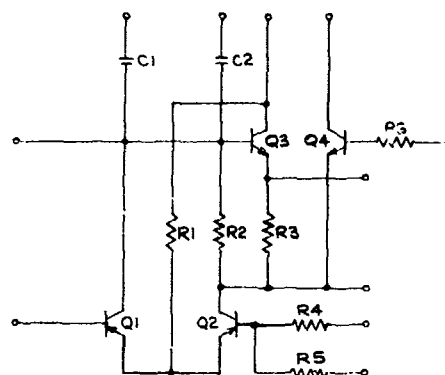


Figure 28-14—Swcen section differential amplifier.



Power rating = 1.36 w  
 Undistorted output voltage = 4 to 8 VPP @  $R_L = 2$  to 50 ohms  
 Average voltage gain = 5 to 9 VPP @  $R_L = 2$  to 50 ohms  
 $D_1, D_2 = 1N914$   
 $R_1, R_2 = 95$  ohms  
 $R_1 = 1.2K$  ohms  $\pm 5\%$   
 $R_3, R_4 = 10$  ohms --- matched within  $\pm 2\%$   
 $R_5 = 10$  ohms  
 $R_6 = 750$  ohms  
 $R_7 = 9K$  ohms  $+ 5, -10\%$   
 $R_8 = 150$  ohms  
 $R_9 = 2.7$  ohms  
 $R_{10} = 10K$  ohms  
 $Q_1, Q_2 = 2N2219$   
 $Q_3, Q_4 = 2N2907$

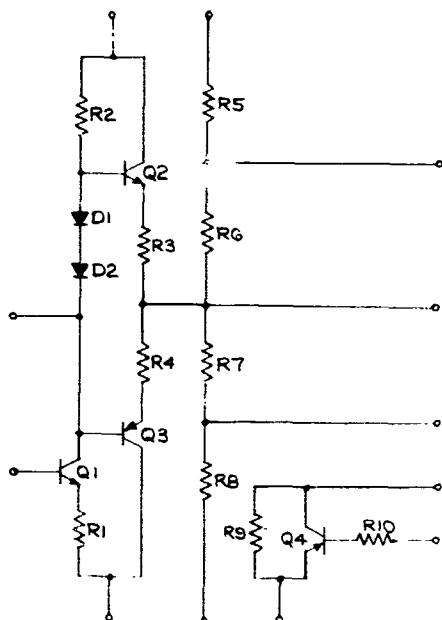


Figure 28-15—Deflection driver.

Power rating = 200 mw  
 Supply voltage =  $\pm 10$  VDC  
 DC level range = 2.5 to 5.6 VDC  
 Output voltage = 1.9 to 2.3 VPP  
 Frequency stability =  $\pm 70$  cps  
 $Q_1, Q_2, Q_3 = 2N2484$   
 $R_1, R_4 = 10K$  ohms  
 $R_2 = 100K$  ohms  
 $R_3 = 110K$  ohms  
 $R_5 = 82$  ohms  
 $R_6 = 50$  ohms  
 $R_7 = 3.6K$  ohms  
 $R_8 = 1.2K$  ohms  
 $R_9 = 1.8K$  ohms  
 $D_1, D_2, D_3 = 1N914$

Resistor ratios:  
 $R_7/R_9 = 2.0 \pm 7.5\%$   
 $R_8/R_6 = 24 \pm 7.5\%$

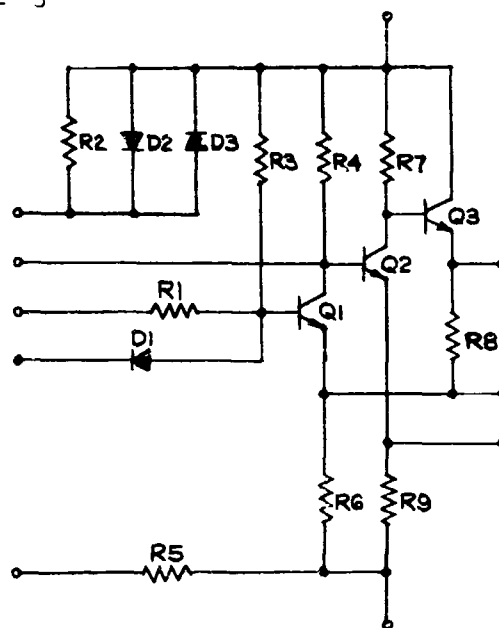


Figure 28-16—Oscillator amplifier.

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2. "Development of a Prototype Molecular System using the CLEM Functional Electronic Block", 12th East Coast Conference on Aerospace and Navigational Electronics, Baltimore, Maryland, October 22 - 29, 1965.

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## 29. DEVELOPMENT OF ELECTRONIC VISUAL INSTRUMENTATION

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This paper presents the history and reasons for development of television by Marshall Space Flight Center (MSFC) for use on space vehicles. A discussion of the theory of systems used includes single and multiple camera use with a common transmitter. Component problems and their solution to meet launch as well as orbital operation requirements are discussed. Microminiaturization and development of new image devices have reduced power required, size, and weight so that a palm-size camera that will meet vibration and other requirements for launch and orbit operation is possible. Also discussed is a new imaging theory approach which replaces the vacuum type imaging tube with a solid state image converter working in a solid state camera.

### HISTORY

During the development of the Redstone and Jupiter missiles from 1951 to 1959, the designer and engineer relied on the measurement devices and telemetry system then available for information on the performance of all parts of the vehicle. These devices measured vibration, acceleration, temperature, stress and strain, etc. In spite of the excellent job these devices did, there were times when the exact nature of a malfunction could not be determined by interpolation of their measurements.

By 1958, it was concluded that a picture would give the most useful information about these malfunctions. Television appeared more valuable than film cameras with their ejection and recovery problems. Since 1958, the Astrionics Laboratory has been developing TV systems for use between space vehicles and earth to gain information for developing the Saturn systems and to monitor the operation of post-developmental vehicles. A continuous study was made of the various instrumentation problems that arose in the development of the Redstone, Jupiter, and Pershing missiles as they were related to vehicle systems development and to space navigation.

In the early programs, flight times and operational ranges were relatively short, requiring a high picture rate with good resolution. Commercially available TV subsystems were then providing a capability of 30 pictures per second with the desired resolution. The decision was made

to concentrate, at least in the beginning, on a small extremely rugged camera capable of withstanding environmental extremes expected during power and coasting flight.

The first flight system consisted of a wideband FM transmitter and a miniaturized camera chain capable of withstanding the least favorable launch environment expected (at that time the Redstone booster). The ground system consisted of a laboratory-fabricated receiver, a broadband amplifier, and a specially built kinescope recorder. This system was the first to transmit real-time high-resolution TV at 30 pictures per second compatible with commercial TV systems from a ballistic missile operating outside the earth's atmosphere. It operated satisfactorily from liftoff to the optical horizon, a distance of more than 320 km, on the Mercury/Redstone vehicle, January 31, 1961.

The next flight was two years later on Saturn I (SA-5), where the system had to be further ruggedized to withstand the  $6.7 \times 10^6$  N thrust of the Saturn during launch and to transmit pictures of various operational parts of the vehicle.

## PROBLEMS AND SOLUTIONS

Investigation showed the following shortcomings of television camera systems used at that time:

1. They were too large.
2. They required too much power and were generally not battery-operated.
3. They were too weak structurally for launch environment.
4. No imaging tube was able to produce a picture while subjected to launch vibration.

Items 1, 2, and 3 appeared to be feasible with present technology.

It was decided to divide the first camera into the following sections:

1. Power supply.
2. Camera head consisting of pickup tube, preamplifiers, and line driver.
3. Camera control containing the remaining circuitry such as crystal-controlled clock, sweep circuits, line drivers, and video output amplifier.

The camera was sectioned to allow the camera head to be made as small as possible so that it could be located where space was limited. The power supply was, and still is, a solid-state

oscillator-type DC-to-DC converter operating from 28 volts DC and supplying the necessary voltage for the camera head and camera control. The camera control was all solid-state, using discrete components and handwired circuit boards. This part is now all microminiature solid-state modules.

The major problem area was the crystal used in the clock timer. Existing crystals could not survive the 20g random vibration required for flight qualification because of the support structure for the crystal. Considerable work was done in this area, and now the crystals will stand 35g random noise (20 to 2000 Hz) rigidly mounted to the container case. To accomplish the first flights, the crystals were "floated" in a silastic compound which served as an adequate vibration isolator.

In the camera head lay the weakest link in the system — the image pickup tube. A vidicon had been chosen because of its size and rugged design. The first tubes could not produce a picture under 5g vibration if the tube was mounted in the case in the conventional manner. To operate at the 20g level required that the socket be removed and the tube connected by flexible wires to the circuit board. The entire camera-head case was then filled with a clear inert silastic compound which floated the tube with respect to the case. This gave the needed isolation to the tube so that the camera head could be attached directly to the mounting position without use of vibration isolators.

During this time, intensive work was being done by Astrionics Laboratory and General Electrodynamics Corporation who supplied the vidicon. Among the major changes in tube design were:

1. Redesign of the electron gun assembly to reduce sliding of the tube in the glass envelope.
2. Redesign of the target mesh to raise the resonant frequency well above the highest expected frequency.
3. Changing the connectors between gun assembly and pins in tube base from solid wire to flexible wire mesh.

Out of this program came a camera that would withstand launch conditions of the Redstone and Jupiter missiles while producing good pictures. Further work was done between 1961 and 1963 to refine the camera head assembly by improving the gain and bandwidth of the video preamplifier and the general camera ruggedness.

The rest of the flight system consisted of a transmitter with its power supply and an antenna system. The assembly was mounted on a single plate except for the camera and looked similar to the assembly shown in Figure 29-1. The camera head alone is shown in Figure 29-2.

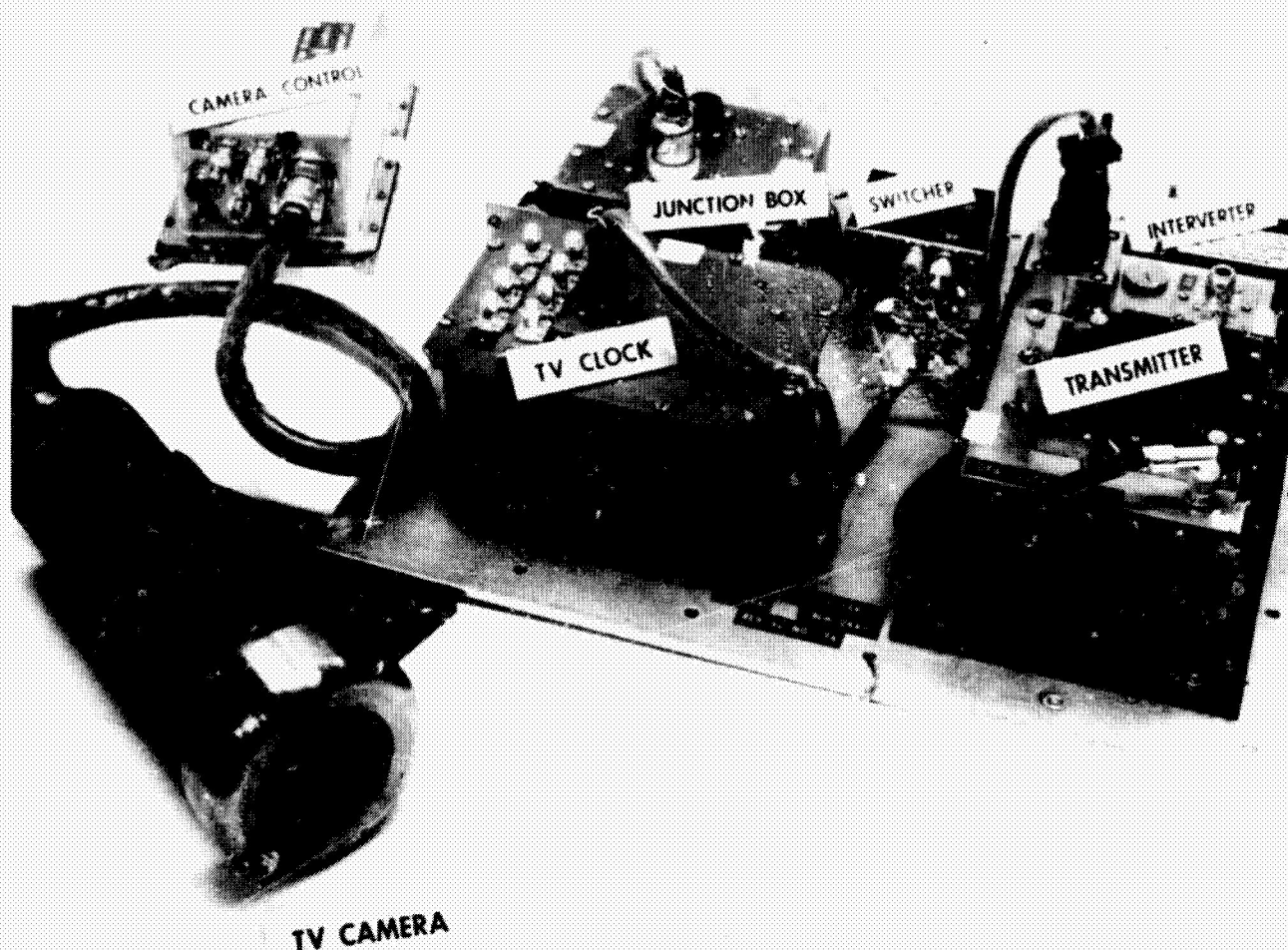


Figure 29-1—Flight TV system for Saturn SA series.

#### SYSTEMS DESCRIPTION

For reasons already given, the following parameters for the TV camera were chosen:

Frames per second	30
Interlace	2:1
Aspect ratio	4:3
Resolution (horizontal)	300 to 500 lines
Scan lines per frame	525
Signal-to-noise ratio (camera only)	30 db
Sync format	Modified EIA

This system is generally compatible with existing commercial television viewing, recording, editing, and playback equipment. The

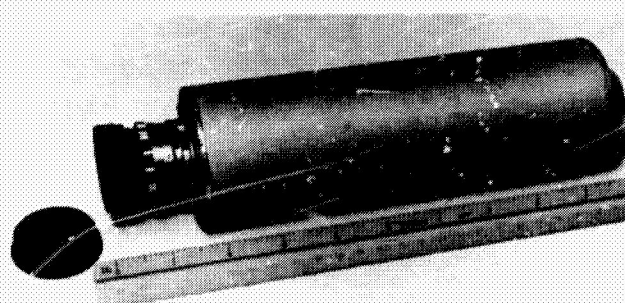


Figure 29-2—Flight camera head for Saturn SA series.

ratio of development-to-information-gained was believed to be the highest. The first system in 1961 used a laboratory modification of a straight FM transmitter. The video baseband from the camera system was 2.5 MHz so that the transmitter had to be essentially flat over a 10-MHz band and produce 5 watts RF. The receiver used a 70-MHz IF with a bandwidth of about 16 MHz and a discriminator of 24-MHz bandwidth. Using a tube-type preamplifier at the 5.8-meter parabolic antenna, the system had a 6-db noise figure at 860 MHz.

By the time SA-5 was ready, the transmitter had been widened to an 18-MHz bandwidth with an output of approximately 5 watts. This has since been raised to 20 watts by making the transmitter a two-package device. The driver is all solid-state and delivers 250 milliwatts to a traveling-wave tube amplifier which puts out 20 watts at 2210 MHz. The receiver was improved by the addition of a phase lock loop discriminator resulting in an overall system gain of better than -100 dbm.

Realizing the advantages of having more than one camera on a vehicle, the author proposed a system which was developed, whereby a number of cameras could be accommodated by the same transmitter. This system uses a device called a video register which times all the cameras in the system to maintain synchronization and transmits one frame from each camera in sequence. These pictures come at submultiples of 30 per second depending on the number of cameras. For example, a single 1/30-second frame picture will be sent every 1/15 second for two camera systems and every 1/10 second for three camera systems. These pictures are all film-recorded on the earth for single-frame study and are also tape-recorded.

The video register is all solid-state, using binary logic with a crystal clock to perform all the selection and switching functions. It may also be operated by ground command through the command system to keep any camera in the system locked to the transmitter for a required period. The companion to this in the ground receiving system is an all solid-state decoder that locks to the receiver output signal and separates the various camera signals to their respective outputs for viewing. The companion to the decoder is a sync processing device using solid-state binary logic. It recognizes the leading edge of each sync interval, both horizontal and vertical, and gates off the flight signal, inserts ground-generated standard commercial sync, and then gates on the flight signal for the video information. This allows in each sync interval the insertion of bursts of telemetry or other information which can be recovered on the ground to provide additional use of the transmitted power from the vehicle.

A final part of the system design is the retrieval technique. As the information is recorded during flight, a special counter counts the frames and records on one of the auxiliary tracks of the video tape machine a serial binary number for each frame so that the numbering is consecutive and each frame has its own number. When the tape is played back the observer can push a store button at any time and capture the next frame on a storage tube as a still picture for study along with its frame number which appears on a Nixie tube display.

By the use of a comparator and coincidence circuit, any frame number can be selected by a set of rotary switches, and the frame with this number can be captured on the storage tube. Thus rapid analysis of post flight tapes can be made with Polaroid prints of these frames available in 5 minutes after the flight.

A system patterned after this under the name of "Video File" is being marketed by the Ampex Corporation. The ITT Federal Laboratory is making available just the frame selection storage portion.

### MINIATURE TV CAMERA

The devices discussed thus far have used the latest solid-state technology available at the time of construction. It was concluded, however, that if the size, weight, and power consumption of the camera could be reduced even further, it could be used in places still inaccessible in the launch vehicle and also find possible use in the orbital experiments in connection with men and animals. In 1964, a "shrink the camera" program was started. As a result, a camera has been built using microelectronics which has reduced the size by 5:1, weight by 7:1, and the power greater than 2:1. The completed operational camera is in one package which measures  $3.8 \times 8.9 \times 15.2$  cm. It uses a 1.27-cm vidicon with electrostatic focus and electromagnetic deflection. The electronics consist of 26 blocks measuring  $1.27 \text{ cm}^2$  and 0.32 cm thick. These blocks do all the work of the electronics of the present flight camera which weighs 3.53 kilograms and measures  $10.2 \times 12.7 \times 15.2$  cm.

The camera, when space-qualified, will weigh 0.68 kilogram, measure  $5.08 \times 7.62 \times 16.5$  cm, and use 7 watts of power. It is resolution-limited by the 1.27-cm vidicon at 500 lines horizontal. It has a commercial format of sync, frame rate, aspect ratio, and interlace, so that it could be put to certain commercial uses immediately such as field use by broadcasting companies for sports and convention coverage. The medical profession can use it to monitor operations and patient activities.

The camera can be readily adapted to a lower frame rate so that it could be used in operations beyond ranges set by power limitations at 30 frames per second.

Figure 29-3 shows the camera, and Figure 29-4 shows some various versions of microelectronic packaging. The small block below the quarter is the size block used in this camera.

### SOLID STATE CONVERTER

In real-time recovery of pictorial information, there is still the proverbial weak link -- the image tube, which is made of glass. It has an electron gun that must shoot its beam of electrons over a target area less than 6.45 square cm and trace 450 or more lines all straight and evenly



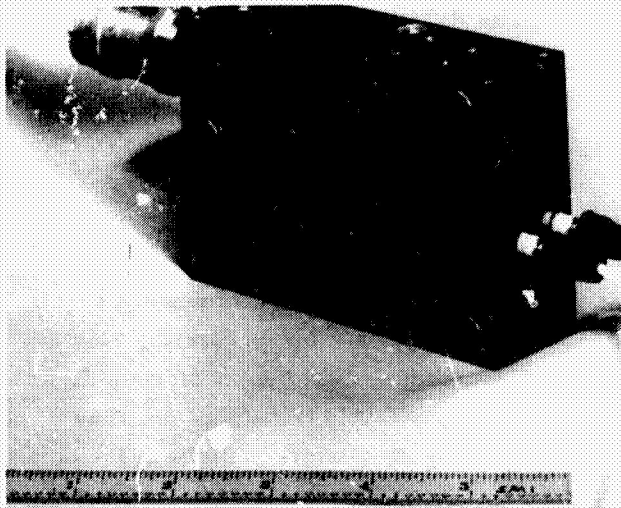


Figure 29-3—Microminiature television camera.

spaced for a good picture while the camera is being subjected to vibration and shock levels unbelievable 30 years ago. The state-of-the-art is apparently approaching the ultimate limit in this type of imaging device. With environmental requirements expected to continue to increase, the next move would be to eliminate the tube so that (in the sense of the electron beam being a moving part) there would be no moving parts.

During the intense tube development of 1960 and following, it became evident to the author that pictorial information obtained by the use of conventional television imaging tubes was not the best electronic means. It was felt

that a solid-state device could obtain this pictorial information without having most of the objectional features associated with standard or experimental cameras.

A system was envisioned whereby the imaging device could be replaced by a solid-state image converter operating on the basis of photoelectric effects, and operated by associated circuitry using the most minute solid-state technology available at the time it was needed. A program was outlined for development beginning in 1962 with Westinghouse Electric Corporation to produce, as the ultimate goal, a solid-state television camera compatible with standard TV resolution and data rates. The program philosophy behind this development was that this system would be

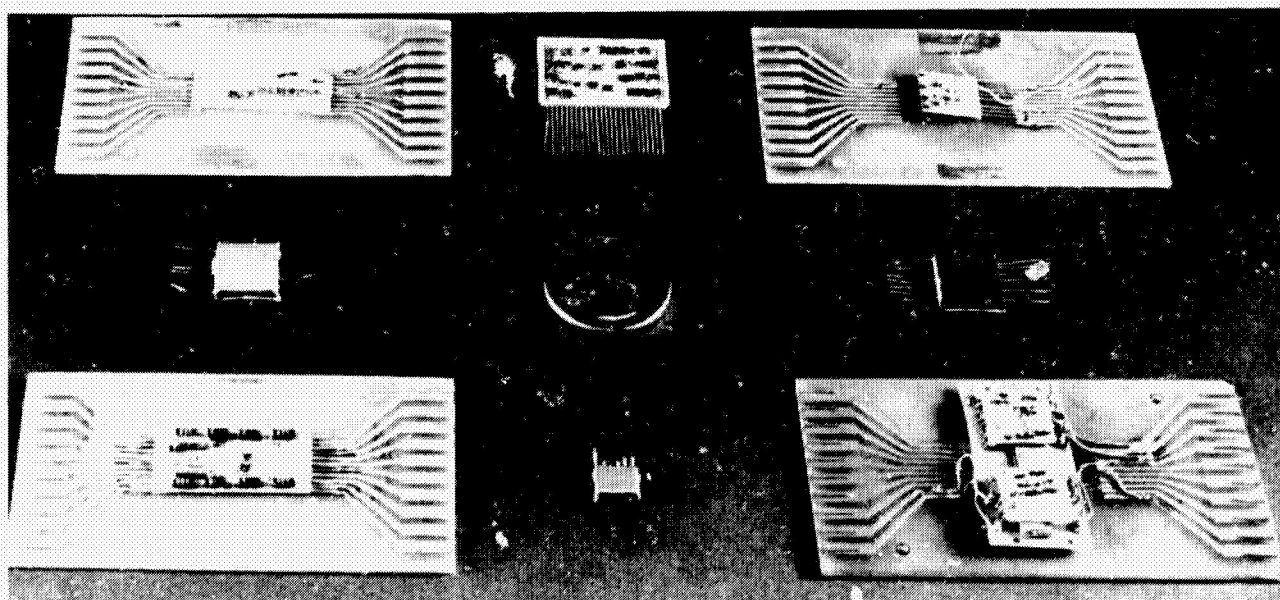


Figure 29-4—Microelectronic packaging examples.

developed in such a time frame within the technological limits so that when the need for imaging devices had exceeded the environmental capability of the best standard flight cameras with tubes as the imaging source, this system would be in operation and either replace or back up the current cameras in use at that time.

Ultimately this type of camera may be best suited for the extended space environment encountered on interplanetary missions. Because of the small size of the solid-state imaging device, a number of them could be used in a craft in the same space as one standard flight TV camera and would require equal or less power. Therefore, it is felt that this is directly related to the future planning of orbital, lunar, and planetary missions. Because this camera uses digital logic in extracting information, it is applicable to any rate of readout, and the output could be transmitted over extremely narrow bandwidths with the same resolution as it could be transmitted over a wide bandwidth system. The only difference would be that the number of pictures per second would be higher for the wideband system, but the circuit alterations necessary for this are extremely minor.

## SYSTEM DESCRIPTION

Figure 29-5 shows the general layout of the parts of this camera: the monolithic  $50 \times 50$  phototransistor mosaic, the molecular digital logic, the molecular readout amplifier, and the field effect transistor (FET) readout switches. These parts will be discussed to demonstrate the use of molecular techniques in a complete imaging system which has practical applications in aerospace systems. Prospects for further improvement to approach the performance capability of the vidicon appear excellent.

The mosaic sensor is the solid-state equivalent of the vidicon and can image radiation in the visible and near infrared regions of the spectrum. It is read out by a combination of metallized interconnections, bonded leads, and a printed circuit board rather than by beam-scan techniques.

Selection of the material for the sensor was based on considerations of both reliable fabrication techniques and material spectral response. Silicon satisfies both conditions: first, the planar diffused processing methods are well developed; and, second, silicon is sensitive to radiation from the near IR to the long wavelength cutoff above  $11,000 \text{ \AA}$ . To minimize crosstalk while maintaining high resolution, imaging is accomplished by conversion within discrete sensor regions, all of which are contained in a single monolith. The mosaic concept was introduced to achieve this large number of discrete isolated elements interconnected in a configuration such that each photo element could be sequentially interrogated as an isolated device without necessitating an unwieldy number of individual leads. The concept of XY interconnections was introduced to provide a structure both manageable in its number of leads and compatible with conventional viewing systems that accept XY data.

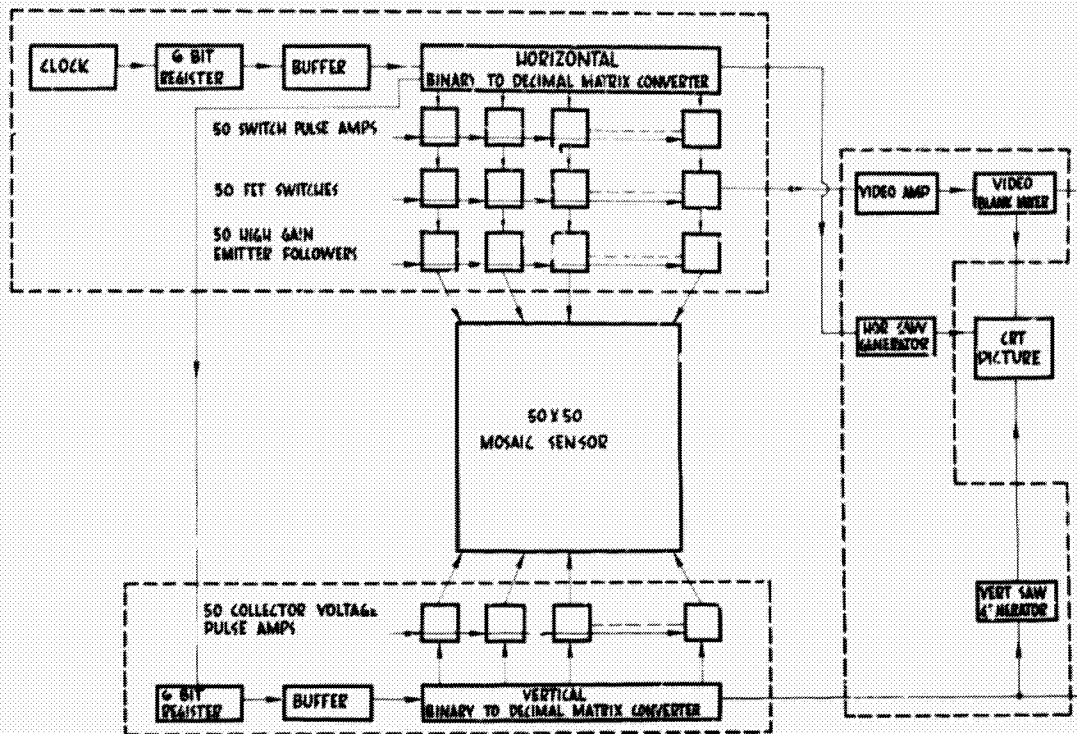


Figure 29-5—Block diagram of solid-state camera.

## SECTION OF MOSAIC WITH XY INTERCONNECTIONS

INTERNAL COLLECTOR STRIPS Y  
SURFACE EMITTER STRIPS X

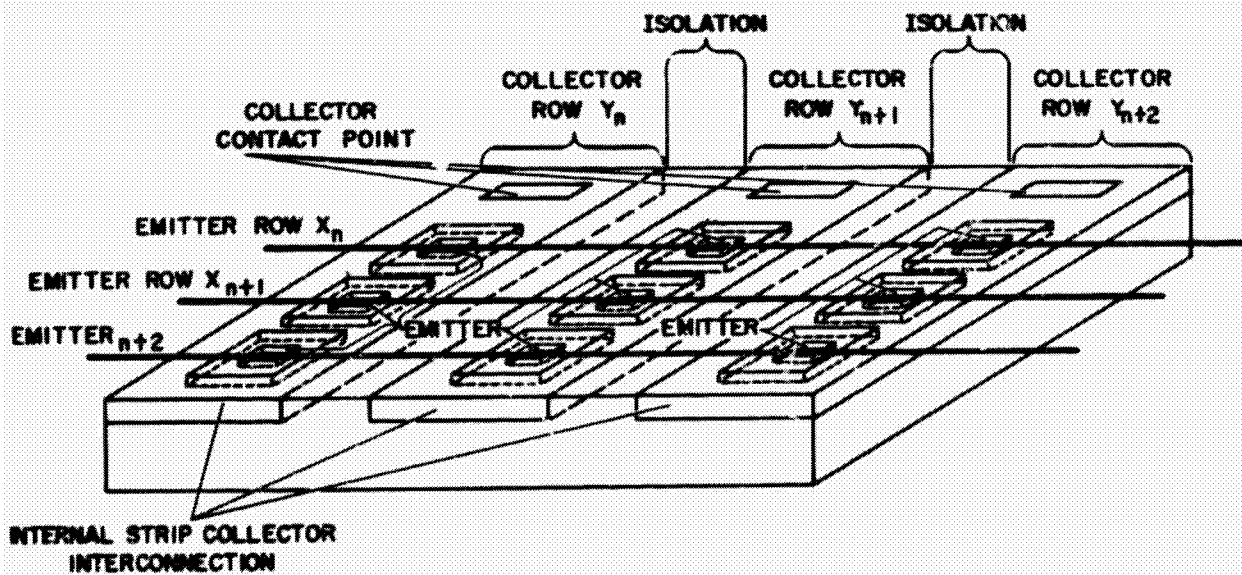


Figure 29-6—Illustration of mosaic interconnection.



The sensor mosaic is a matrix of  $50 \times 50$  NPN phototransistors on 0.00254 cm centers, giving a total of 2500 phototransistors. The phototransistor elements have a square geometry with discrete emitter and base regions, but with collector regions common to a row of 50 elements (Figure 29-6). No electrical access is provided to the individual phototransistor base regions. The emitters are interconnected with evaporated aluminum strips in 50 isolated columns.

Unique access to any individual element of the XY mosaic is available through one of the X leads and one of the Y external leads. Only the single element which lies at the intersection of these XY interconnections is interrogated. This structure of light-sensitive elements with XY diffused and deposited interconnections is shown in Figure 29-7 with a microphoto of part of the structure.

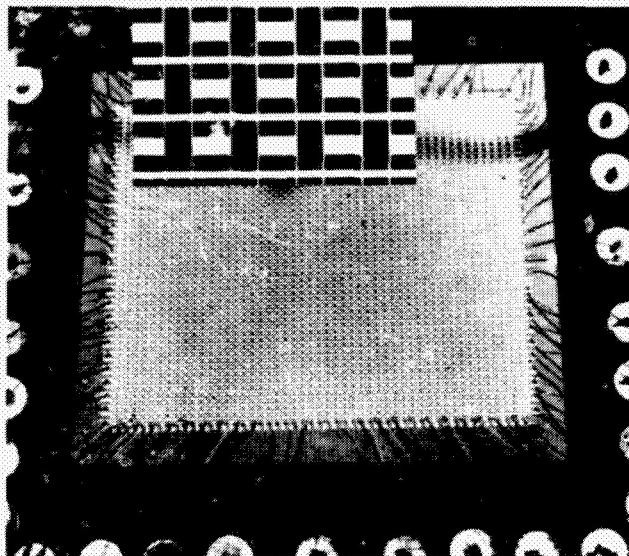


Figure 29-7—2500 element mosaic wafer.

Figure 29-8 shows the mosaic mounted for testing. Readout is accomplished by applying a voltage to a 50-element collector strip and sequentially commutating the rows of emitter elements (Figure 29-6). In this way, it is possible to sequentially read one element at a time while cutoff is maintained for all other elements.

Flip-flop logic is used to obtain a sequence of pulses necessary for multiplexing the mosaic. The logic provides the timing for pulsing the emitter readout switches, for the application of voltage pulses to the collector rows of phototransistors, and for synchronizing the horizontal and vertical saw generators for the monitor. With this logic, fanout requirements are nominal, and reliable operation is ensured because of the sequential nature of the set/reset operation in a string of flip-flops.

To enhance camera sensitivity, the emitter element readout circuitry includes 50 emitter follower-amplifiers. These emitter followers

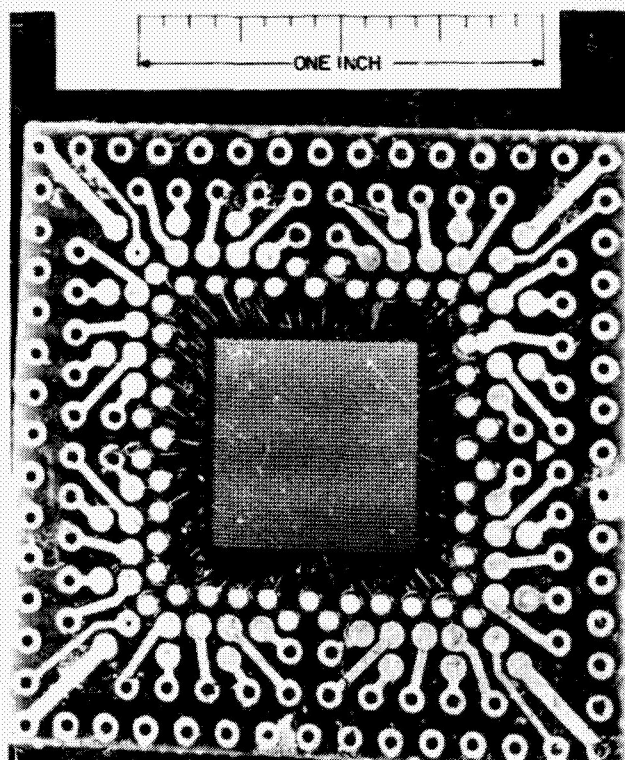


Figure 29-8—Mosaic wafer mounted for testing.

provide a high input impedance for each phototransistor element and a low output impedance for the switching circuit, which uses field effect transistors selected for minimum offset voltage and high impedance gating characteristics.

Since a phototransistor structure was selected for the discrete photon detectors of which the mosaic is composed, the diffusion junction depths must be minimized, bulk minority carrier lifetime must be maximized, and the width of the depletion layer at the base collector junction must be large. Extreme processing control is not necessary to obtain useful single phototransistor elements; however, it is absolutely essential to fabricate a uniform mosaic of as many as 2500 elements on a single monolithic crystal.

Like a vidicon camera tube, a phototransistor element is a current generator and therefore requires a current amplifier — the gain required being substantial (depending on the ambient subject light level) over a bandwidth which allows element signal rise-fall times of less than 1 microsecond (Figure 29-5). To prevent noise levels from being generated by unwanted transients in the switch circuits, it is necessary to put the amplifier before the emitter readout switch. The amplifiers in use now have a current gain of 300 at one microampere and an input impedance of 300,000 ohms. This allows operation in the linear area of the amplifier curve and produces sensitivity near that of the vidicon.

The emitter follower-amplifier is very necessary in the readout commutating circuitry for a number of reasons. The most important is that the impedance may be made so small that switching speeds required to read out mosaics of much larger than  $50 \times 50$  elements can be readily obtained. The sampling switches are now field-effect transistors so used as to provide excellent isolation between gate and source drained circuits, low noise level, and no offset voltage requirements. In addition, they require only one polarity switching pulse. The signal handling capability of the switches ranges from 1 millivolt to 1 volt.

The sampling switches multiplex 2500 mosaic analog signals into one output resistance. Since there are 50 discrete elements on a line, the dwell time per element is about 6.6 microseconds, and the clock frequency is 150 KHz. For the line switching, the dwell time is 50 elements times 6.6 microseconds, or 330 microseconds. The clock frequency for this sweep, which is synchronized with the element sweep, is 3 KHz. The choice of logic form to meet these requirements was determined by its compatibility with integrated molecular circuitry. From experience gained with diode matrix ring counting, it was decided to use standard NPN flip-flop binary logic. Reliable operation of the flip-flop was assured because of the sequential nature of the set/reset operation in the register of flip-flops and the nominal fanout requirements.

The required timing for the series of 50 pulses to drive the 50 element commutator for both X readout and Y readout of the mosaic sensor is obtained from the 6-bit flip-flop register. Since only 50 of the available 64 sequential outputs of the register are used, a carryover function or reset logic provision is necessary at the termination of readout of each line and row of mosaic sensor elements. This eliminates readout dead time. A diode matrix converter is used for

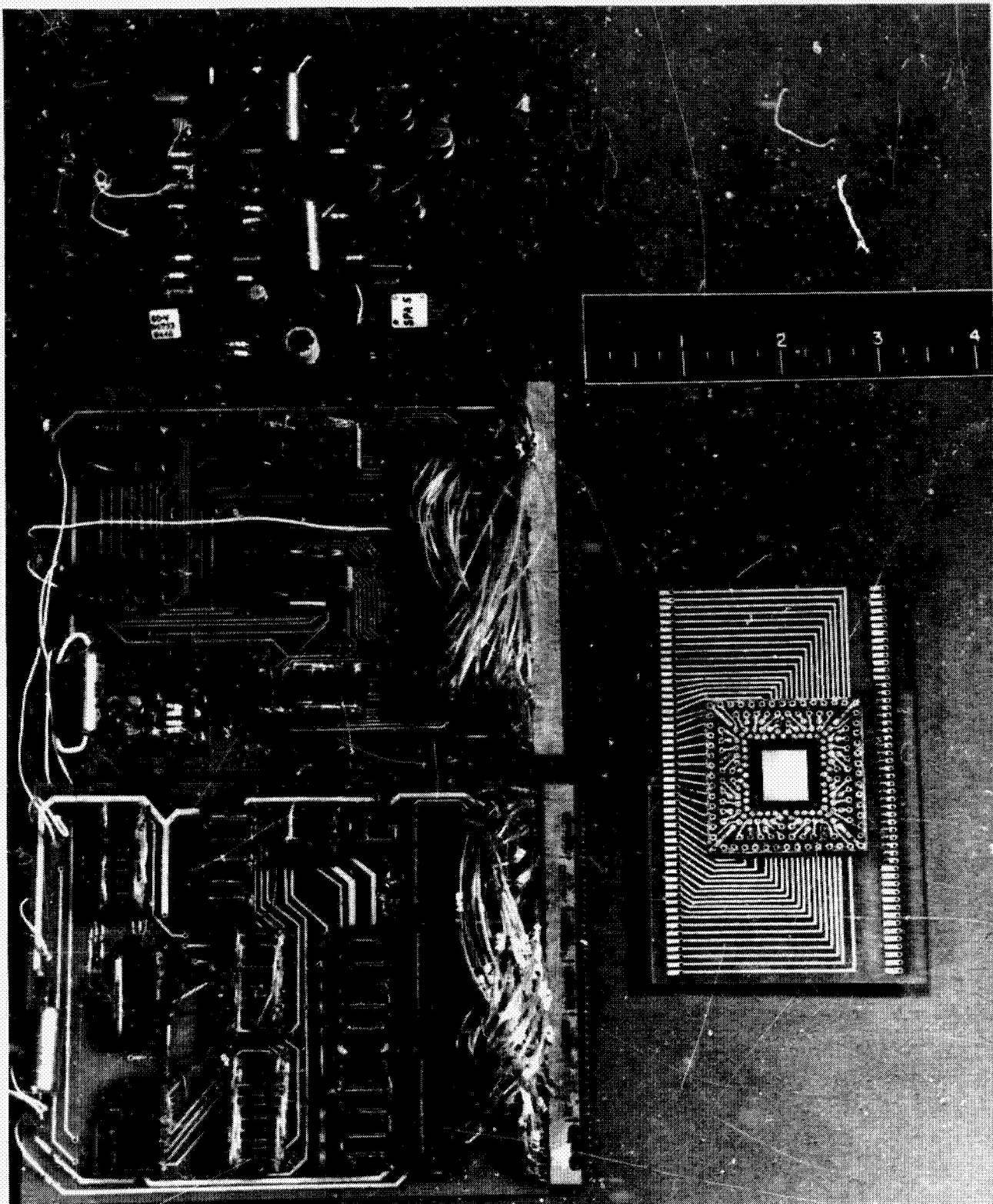


Figure 29-9—Component layout of solid-state camera.



translating each number of decimal notation. Amplifiers are needed at the output of the converter to provide correct amplitude and phase to drive each of the field-effect transistor switches. The Y-readout logic is similar to the X-readout logic, but it operates at a clock rate of only 3 KHz.

Figure 29-9 is an exploded view of the inside of the camera. The silicon mosaic wafer is 1.3 cm square and uses a standard 16-mm lens system. The readout circuitry packaged in the welded modules contains the required commutating switches, the logic and switch pulse generating circuits, and the coupling pre-amplifier between the mosaic and the switches. These circuits permit high packing density since they are all monolithic. Also included in the package are horizontal and vertical sweep generators and a video mixer amplifier. The package has a volume of  $15.2 \times 10.2 \times 8.9$  cm. No attempt has been made to eliminate the unused space in this package. The power consumption is approximately 4 watts.

## CONCLUSIONS

A camera that can be made more compact, economical, reliable, light weight, and that requires less operating power is indicated by present progress. An example of this is the size comparison shown in Figure 29-10 between the 1.27-cm tube used in the camera of Figure 29-3 and the 2500 element mosaic (Figure 29-8). Improved image, geometrical fidelity, greater dynamic range, less image smearing, and new types of signal processing with digital scanning should result from the successful completion of this program.

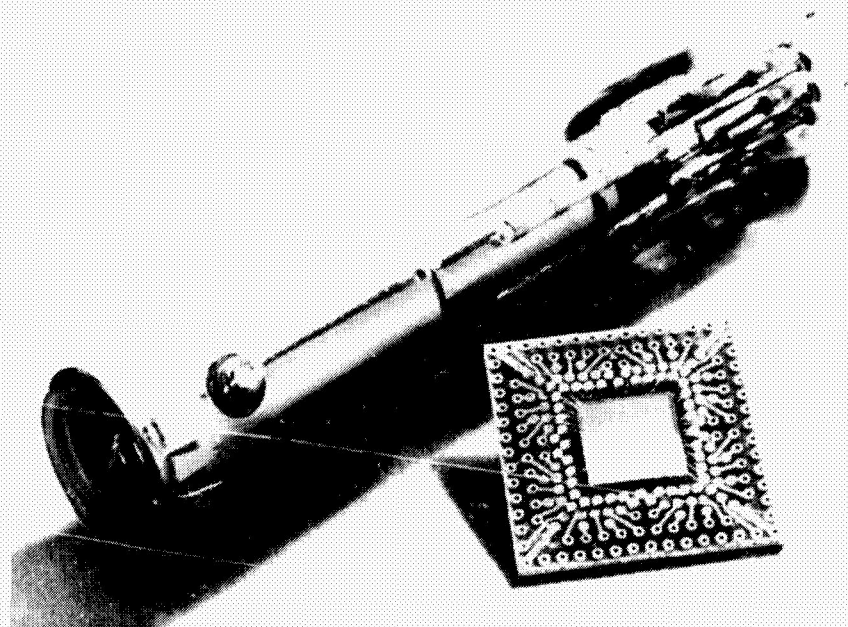


Figure 29-10—Comparison of vidicon and mosaic wafer.

A mosaic containing 12,800 phototransistors has now been fabricated and tested. This is an array of  $100 \times 128$  elements measuring approximately  $1.27 \times 1.52$  cm. The original geometry of

the phototransistors was square; but since the base area of the transistor is the light sensitive area, the new array uses a slightly rectangular design that requires much better isolation between adjacent base areas on the collector row.

Television on flight vehicles has proved its usefulness at every test including covering engine performance on the test stand as well as in flight, stage separation, upper stage ignition, vehicle attitude, deployment of the micrometeoroid panels on the Pegasus flights, and observation of fuel performance under zero gravity in orbit. More uses are now being planned and developed.



N67-51592

30. PACKAGING FLAT-PACKS FOR SPACECRAFT APPLICATIONS

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Four methods of interconnecting flat-packs are described. Three of them are well-known techniques. They are the multilayer board, laminated-comb, and magnet wire stick techniques. The fourth technique, the molded interconnect board, is a new technique just emerging from the experimental stage. Advantages and disadvantages of each technique are described.

Since functional electronic components encased in flat-pack geometries have become popular, many techniques have been developed for interconnecting these devices. As with any new technology, many new applications are developed, and only those which prove capable of satisfying the intended objectives survive the test of time. Although mass usage in itself does not constitute adequate reason for adopting a given technique, the fact that many engineers have found that technique usable is in itself sufficient reason for serious consideration of its application.

This presentation will deal with four methods of interconnecting flat-pack devices. Three methods are in various degrees of popular usage; the fourth is a new technique which is just emerging from the experimental stage. The fourth technique is being presented because it is believed that it has strong potential for future applications in the complex interconnecting of many integrated circuits in spacecraft.

The three popular techniques described are the multilayer board technique, the laminated-comb technique, and the magnet wire stick technique. Of these three, the most popular one today is the multilayer board. Because of this popularity, it is not necessary to go into a detailed description of the various processes available for the manufacturer of multilayer boards. There are two basic processes, an additive one and a subtractive one. The major advantages of multilayer boards are volumetric efficiency, weight efficiency, reproducibility, and adherence to more-or-less standard techniques and processes, both in the manufacture of the multilayer boards themselves and in their subsequent usage.

The disadvantages of multilayer boards are high cost, long lead-time, poor flexibility for change or modification in the end product, and, at the risk of being controversial, the questionable reliability of the product. Although plated through-holes and multilayer boards have been in use

for over 8 years, there is still much which is unknown about the process and its limitations. The yield of multilayer boards is still quite low, ranging from 50 percent to 75 percent.

In general, it is not considered advisable to use multilayer boards in situations where very few of any given type are required. This is true not only for economic reasons, but also for reasons of reliability and flexibility. In situations where large quantities of multilayer boards are required, it is expected that all changes will be incorporated over a period of time into the tooling required to produce these boards. Where only two or three multilayer boards are required, such as in spacecraft applications, the probability of the boards ever reaching their final intended state is small. More than likely, the boards will reach the end product requiring modifications. These modifications can be additive, subtractive, or both. The extent to which changes are required and the nature of the changes will greatly affect the product reliability.

The excessive handling, drilling, and jumpering required to incorporate changes in a multilayer board inevitably decrease total product reliability. Where the intended environments become less friendly, the possibilities of layer delamination and breaks in plated through-holes become greater. Although multilayer boards have been used in spacecraft, it is believed that the limitations previously described conflict strongly with the accepted definition of spacecraft component requirements.

It is claimed by some, and rightly so, that regardless of complexity, integrated circuits can be fully interconnected on a two-sided board. The implication is that if no limitation is placed on the amount of conductor stitching from one side of the board to the other, and if no limitation is set for the spacing between devices on the plainer carrier, then a two-sided board will be adequate for full interconnection. This concept has been demonstrated by many. In cases where the complexity level of interconnections is low, the demonstration appears to be more feasible and more advantageous. Where high levels of complexity occur, volumetric expenditure and the number of plated through-holes per device become increasingly large. Compromising the surface area per device can lead to conductor widths and conductor spacings which are below acceptable minimums.

Work is being done by several companies to optimize and pseudo-automate the procedures for multilayer board layout. This work is being done by computer techniques. The optimizing which a good computer program will afford is a minimum number of layers, a minimum number of interlayer connections, minimum lead lengths, and a minimum amount of surface area. The use of a computer for this type of designing will tend to reduce the human element of error and greatly simplify the end product.

Moving towards designing multilayer boards by computer will definitely tend to reduce the disadvantages associated with manual design. However, the disadvantages associated with processing the boards would still remain. If the entire process of manufacturing printed circuits were fully automated, the equipment required to control the processes and perform the operations in their proper sequence would be so complex that any poor reliability previously associated with the end product would now be associated with the equipment used to produce the product. The resulting

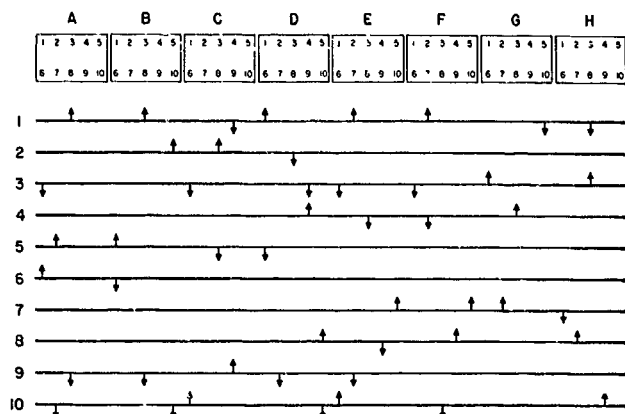


Figure 30-1—Chattered interconnect for ten busses.

effect would be no more predictable than when done by conventional manual-batch techniques. With all the disadvantages stated, the advantages of multilayer boards are so attractive that their continued use and acceptance in the industry is virtually guaranteed. Although the multilayer board is the most popular method of interconnecting flat-packs today, other techniques are used. The method of interconnecting flat-packs with laminated combs will be discussed next.

The laminated comb technique has gradually gained popularity in situations where fewer devices are to be interconnected. The technique is very suitable for situations where 8 to 20 reproducible flat-packs are to be interconnected quickly and inexpensively. The laminated comb when fully assembled resembles a long, thin module, the length being the cumulative length of all of the flat-pack devices which it interconnects. The width would be the width of the flat-pack including the leads; the thickness would depend on the number of combs which are laminated in order to form the complete assembly interconnect.

The input and output leads of this long module could extend from one of the long edges or from both of the long edges. The major advantage of this method of interconnecting flat-packs is the absence of layer-to-layer connections in the interconnect media. The entire system of interconnections consists of one interface or joint (solder or weld) per flat-pack lead used plus (depending on the method used) one joint per input or output lead. This minimum number of joints is possible because any given comb layer within the laminated structure will include all of the points which constitute a part of this circuit node. Since all points of this circuit node are a part of the comb, there is never a need to join one comb to another, as shown in Figure 30-1. Some combs will be shorter than others, and in order to minimize the number of layers in the total lamination, more than one comb may be placed on a given layer (Figures 30-2, 30-3, and 30-4). When a layer is

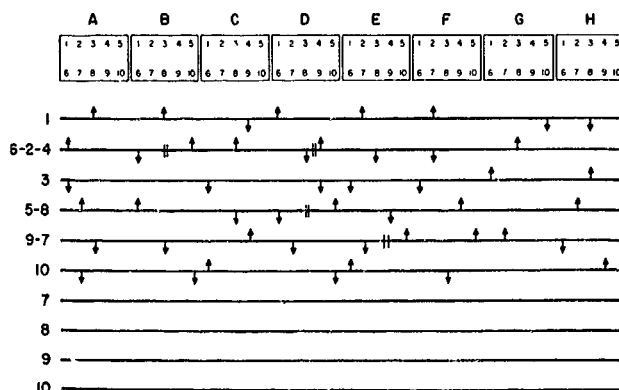


Figure 30-2—Combining nodes.

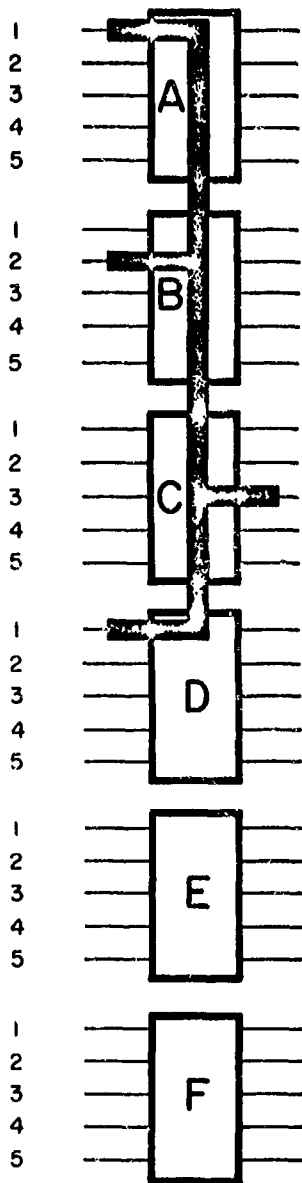


Figure 30-3—Complete circuit node on one level.

shared, the two or more nodes are put in series with each other; this arrangement looks like a comb with one or more cuts in the trunk. Although the laminated-comb process is no more repairable or modifiable than the multilayer board, it has the big advantage of being much less complicated. Because of this low level of complexity the entire laminated-comb structure can be redesigned and rebuilt, allowing any required changes to be incorporated with a minimum loss of time or expense.

The simplicity of the geometry has encouraged some companies to undertake automated production of the combs and their lamination. One manufacturer has limited his automation to selective removal of fingers from the full, blank comb, while another manufacturer has fully automated the entire process. The major disadvantage of the laminated comb is the limited number of devices which it will accommodate. This means that even after the module has been built and the devices attached, the problem is not fully solved. Because of the limited

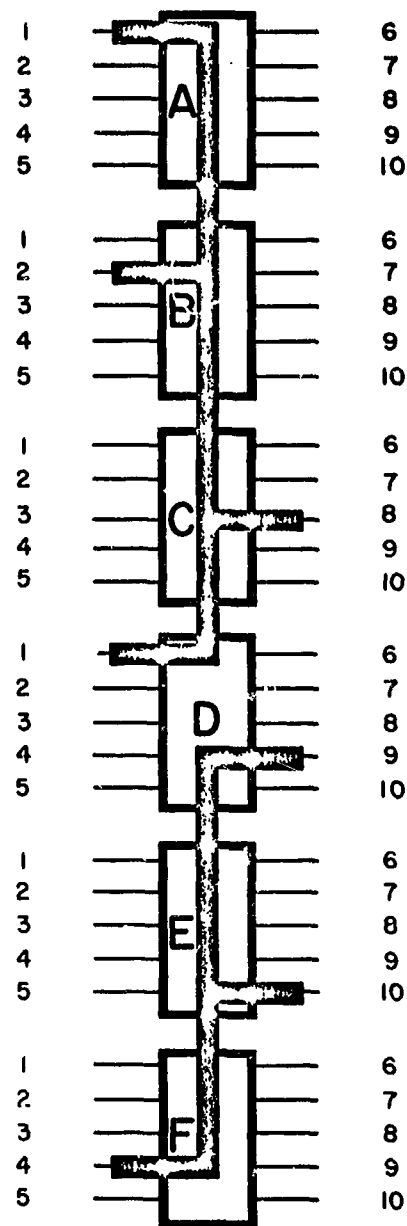


Figure 30-4—Two complete nodes on one level.

number of flat-packs that can be attached to a single, laminated-comb structure, the problem of interconnecting the laminated-comb structures still exist. The magnitude of this problem is much less severe than that of interconnecting flat-packs, since the spacing between input and output leads on the laminated-comb modules is considerably greater than the fifty-thousandths that exists in the flat-pack device. These modules can be interconnected very effectively by a two-sided printed circuit board, by point-to-point wiring, or by local harnessing.

The laminated comb offers a very simple visual check for accuracy. After the lamination of the combs, there should be only one comb finger per flat-pack lead position extending from the

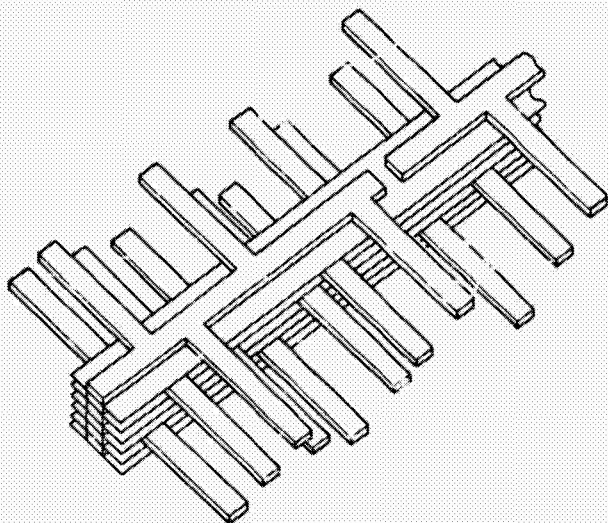


Figure 30-5—Superimposed segmented trunks.

side of the comb (Figure 30-5). If more than one lead appears, (superimposed) there has been an error either in layout or in lamination. A missing finger will also alert the operator. Once the artwork or the punched tape has been successfully completed, the chance of a faulty lamination is slim. Simple indexing, polarizing, and sequencing devices in the laminating jigs will prevent any possibility of faulty laminating.

One company makes a do-it-yourself kit which will permit the user to remove the fingers selectively from the combs, attach the flat-pack to the laminated column, and then insert the entire assembly into a shell; the shell contains connector pins for ready insertion and with-

drawal of the entire module in a breadboard arrangement.

The laminated-comb concept is refreshing because it is so very simple; however, the simplicity does not give it flexibility. It also does not solve the problem of interconnecting the laminated-comb assemblies.

The next technique described is the magnet wire stick technique. This technique boasts very high flexibility and good repeatability for low-volume usage. The magnet wire stick requires no artwork, since the sequence of interconnections is almost arbitrary. This is a technique which has been used at JPL on several projects, such as OGO-E, the Bio-Satellite, and a pulse height analyzer. Because of successful usage, this packaging technique has been selected for several future applications where flat-packs are involved. The magnet wire stick will accommodate flat-packs, discrete components, or a combination of both. The carrier of this module is a thermosetting plastic (EPIALL) tray in which output pins have been molded (Figure 30-6).

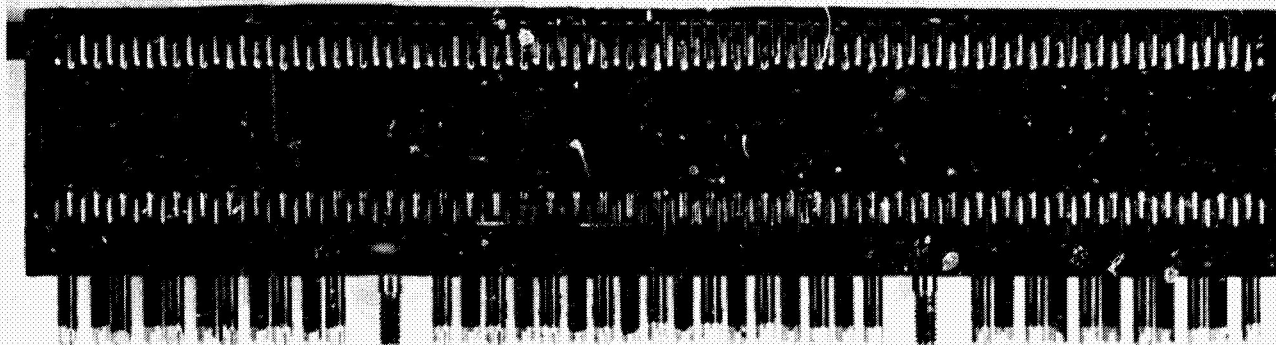


Figure 30-6—Magnet wire stick module.

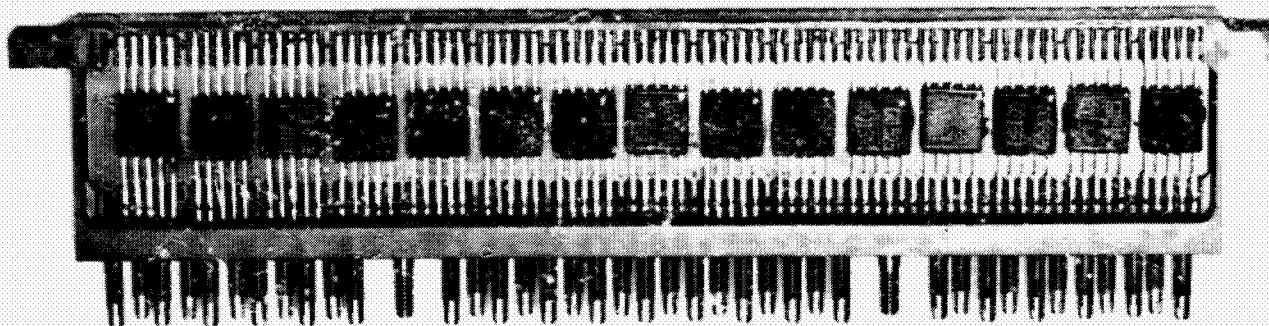


Figure 30-7—Component side of module.

Other terminals which are either molded in or added through the web of the molded stick are used on the one side of the web for attachment of the components such as flat-packs or discrete components (Figure 30-7). The other side of the terminals is used for routing polyurethane-coated wire from point to point to complete circuit runs (Figure 30-8). The magnet wire is soldered to the terminals on one side (Figure 30-9); on the other side, the components are either welded or reflow-soldered to the opposite ends of the same terminals.

The wire routing is done with a pencil-shaped tool through which the wire is fed (Figure 30-10). The wire passes through a tension-dereeling device which exerts equal pull on the wire at all times (Figure 30-11). Because of the three-dimensional flexibility of the wire and the ease with which the solder joint can be undone and redone at any time during, or subsequent to, the interconnection of the terminals, a wire run may be removed and rerouted. A mother board which interconnects many magnet wire sticks can be designed to avoid all conductor crossovers in the interconnect pattern. This is done by designing the mother board prior to designing or laying out the discrete, stick module magnet wire interconnects. When the mother board interconnect is laid out first, the discrete modules are assigned input and output pin designations based on the mother board design. The areas of a circuit interconnect which are not prone to change are the voltages and the ground conductors. Because of this situation, it is possible to make these interconnections less amenable

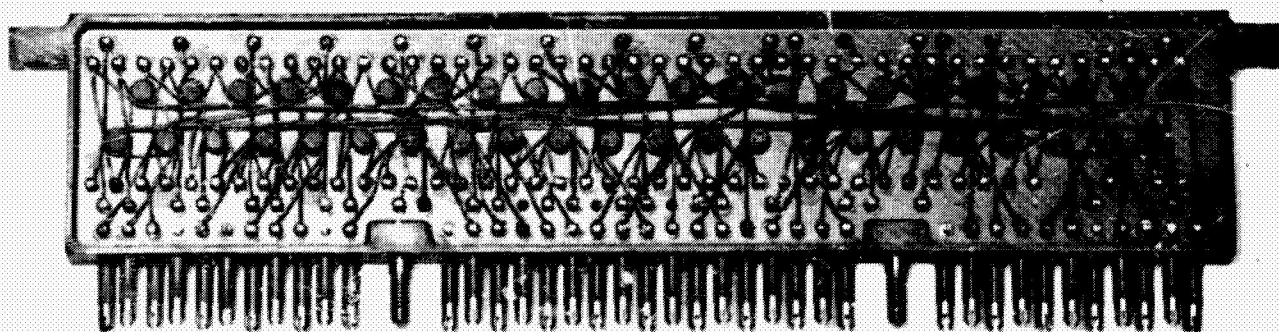


Figure 30-8—Wiring side of module.



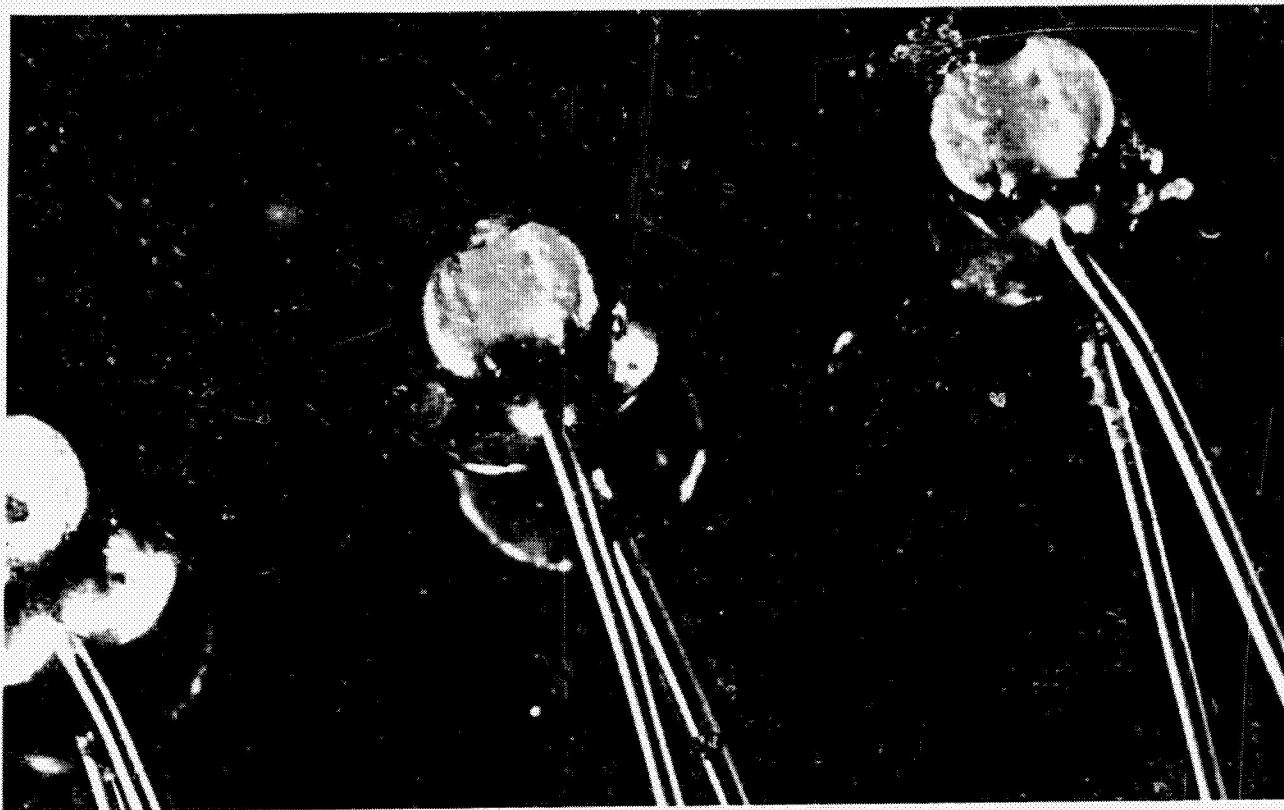


Figure 30-9—Magnet wire soldered to terminals.

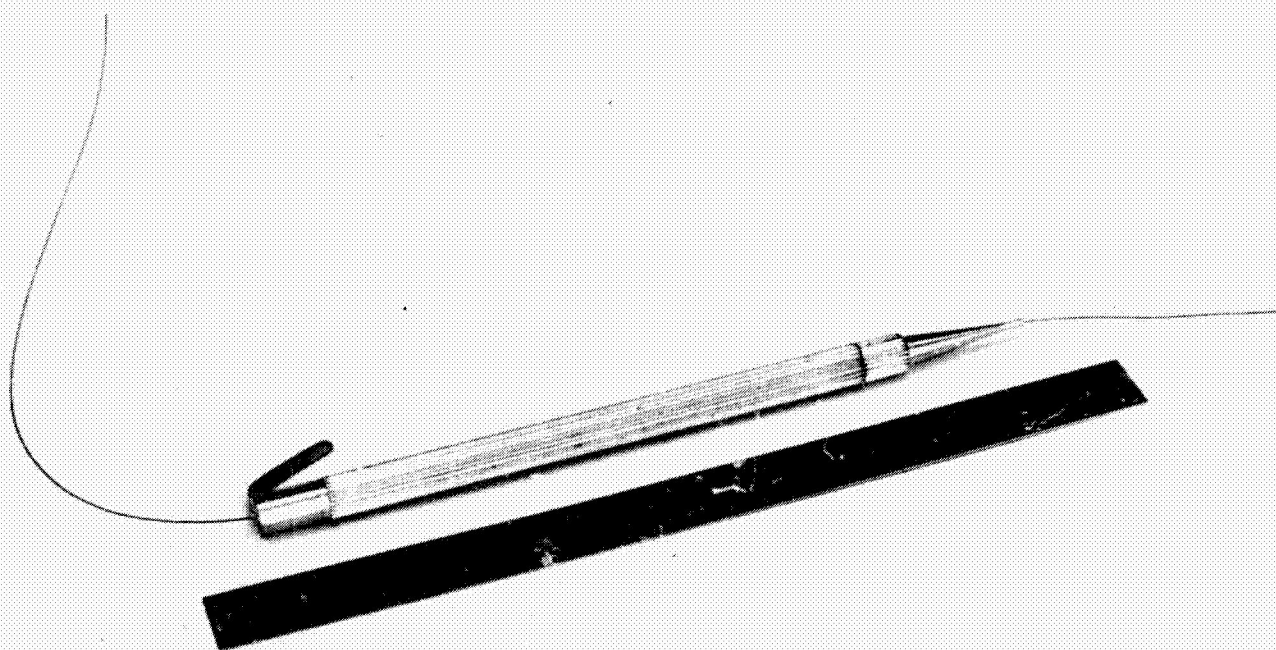


Figure 30-10--Wire routing tool.

to change or replacement. This is done by using etched performs which fit over the respective circuit terminals and are subsequently soldered in place.

The stick module can be used in conjunction with test connectors. These connectors, when mounted on a chassis and fully wired, provide a plug-in subsystem test capability. The stick modules can be plugged in and removed from the wired chassis. It is true that in order to wire the magnet wire stick modules effectively, economically, and reliably, an operator training program is required. This training cycle for operators familiar with delicate wiring techniques, is only two or three days. Once operator training has been successfully accomplished, complete complex subsystems can be interconnected in a matter of days. Any changes which have to be made can be introduced in minutes. The ability to plug the sticks in and out of an interconnect chassis makes testing down to the basic circuit function fast and effective.



Figure 30-11—Wire routing station.

Because of the previously described flexibility and reliability, the magnet wire stick module is accepted and used for spacecraft packaging applications at JPL. Although this module does not have the volumetric efficiencies that are possible with multilayer boards, its other advantages far outweighs this deficiency for most spacecraft usages.

The multilayer boards, which were discussed previously, have some very definite advantages, and as was noted, these advantages are so desirable that the multilayer board is used very much even though the disadvantages are thoroughly understood by the user. The magnet wire technique, as was noted, has limitations and disadvantages also. The interconnect scheme which will be described next, the molded interconnect board, has the geometric advantages of the multilayer board and the process advantages of the magnet wire technique. It compromises some of the versatility and flexibility of the two schemes so that the result is a product more flexible than the conventional multi-layer, but less flexible than the magnet wire stick module.

Simplicity is perhaps the major attribute of the molded interconnect board. This technique was developed by a West Coast corporation which had worked with us on the stick module. Recognizing the inherent advantages of the magnet wire routing and the weakness of the geometry, they developed a product which resembles a multilayer board (or a printed circuit board). The board is 1/16 inch thick and has either edge contacts or termination pads to which wires or flat cables may be connected. Because of the unique process used to create the pad geometry, the pads unlike



printed circuit boards, can extend the full thickness of the board. Pad material can be stainless steel, nickel, or a combination of various metals. The process begins with a metal plate approximately 1/8 inch thick (Figure 30-12) into which grooves are machined on both X and Y coordinate axes. These grooves can be on fifty-thousandths centers or any other increments which are convenient. The increments need not be the same for both axes. The resulting effect is that of a waffle plate with small metallic cubes arranged symmetrically on a plate (Figures 30-13 and 30-14). The magnet wire is welded to these pads. This welding is accomplished through the insulation by use of a heated electrode, or a three-electrode system. The wire is routed from cube to cube as required. When all of the wiring has been completed, the plate is placed in a mold which is filled with a thermosetting plastic either by compression molding or by transfer molding. The molding material completely encapsulates the wires so that when the part is removed from the mold, one side is solid metal, and the other side is solid plastic.

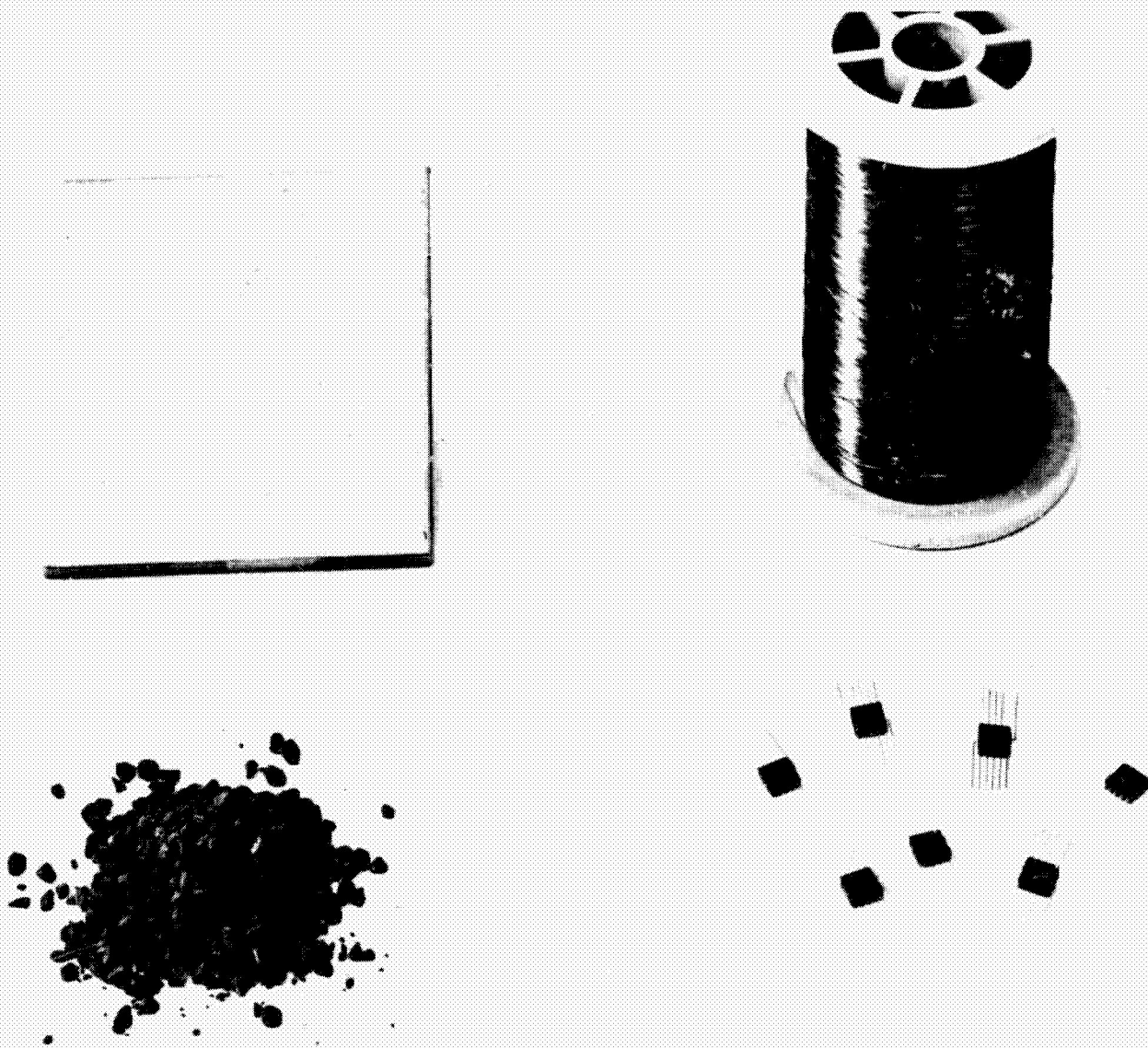


Figure 30-12—Molded interconnect board ingredients.

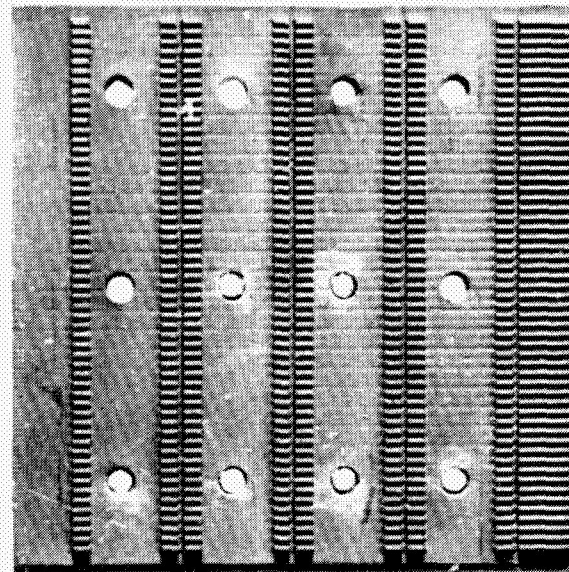


Figure 30-13—A machined plate.

If the X and Y grooves are machined to varying depths, then selective rows of metallic squares or rectangles can be exposed on the plastic side of the molded part. Next the metal side is etched away and then ground and polished to a smooth finish. This side will now be plastic since the metal was removed down to the level of the plastic interface, and there will be exposed rows of square or rectangular metallic terminals, flush with the face of the board (Figure 30-15). These terminals are fully (selectively) interconnected, the interconnections being inside the plastic. As previously stated, by cutting groove depth selectively, the edge fingers of the board can extend the full thickness of the board so that they are solid and visible from both sides of the board. The flat-packs are attached to the terminal pads on the face of the board by parallel gap-welding or by reflow soldering (Figure 30-16). Because of the thickness of each terminal, there is no danger in lifting the pads, and heat sinks and mounting frames can be molded into the assembly as an integral part of the interconnect board. Boards can be laminated back-to-back for maximum volumetric efficiency. Delivery time for a 40- to 50-flat-pack board is 1 to 2 weeks. The time difference depends on whether a mold exists for the specific product size required.

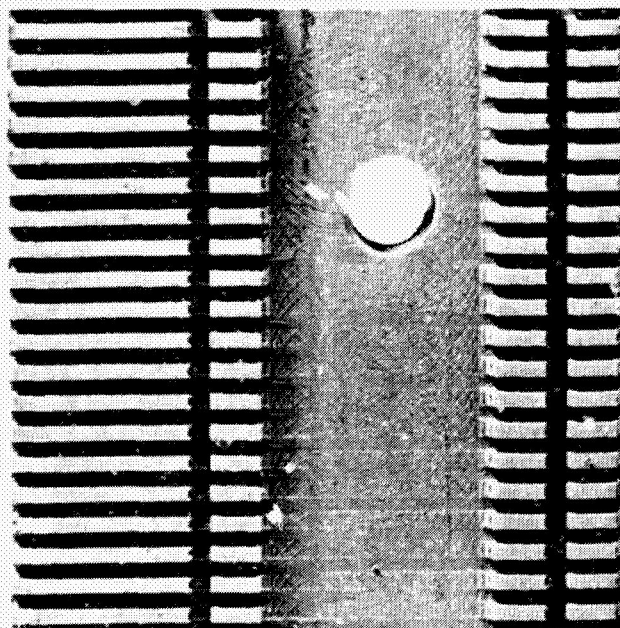


Figure 30-14—Close-up of machined plate.

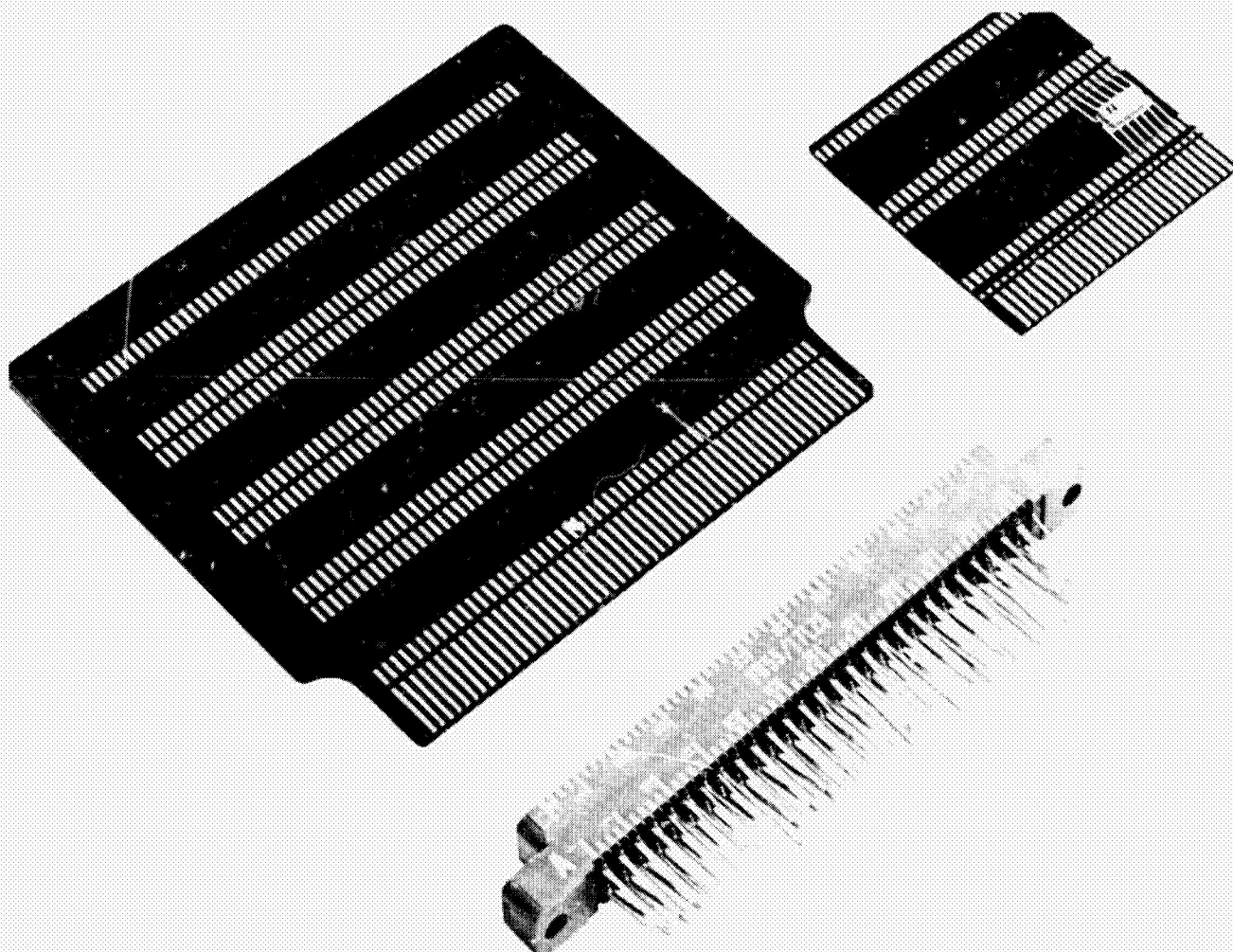


Figure 30-15—Molded, etched, and ground plate.

The cost of the molded interconnect board in small quantity is considerably less than for equivalent multilayer boards. As quantities increase, there is a cost crossover. The flexibility of this technique subsequent to the molding operation is limited to the addition of jumpers. However, prior to molding, any additive, subtractive, or corrective modification can be made. Because the molded interconnect board concept seems to fill so many of the requirements that are unique to spacecraft application, greater usage of this technique is anticipated in the future.

In this presentation four types of flat-pack interconnecting schemes were discussed. They were the multilayer board, the laminated comb, the magnet wire stick module, and the molded interconnect board. These techniques can be used to their best advantage by weighing the attributes and deficiencies of each scheme as applied to a specific product and its application. There will be trade-offs since ultimate superlatives are nonexistent. Careful matching of the proper interconnection process to the packaging task at hand will yield a more optimized end product.



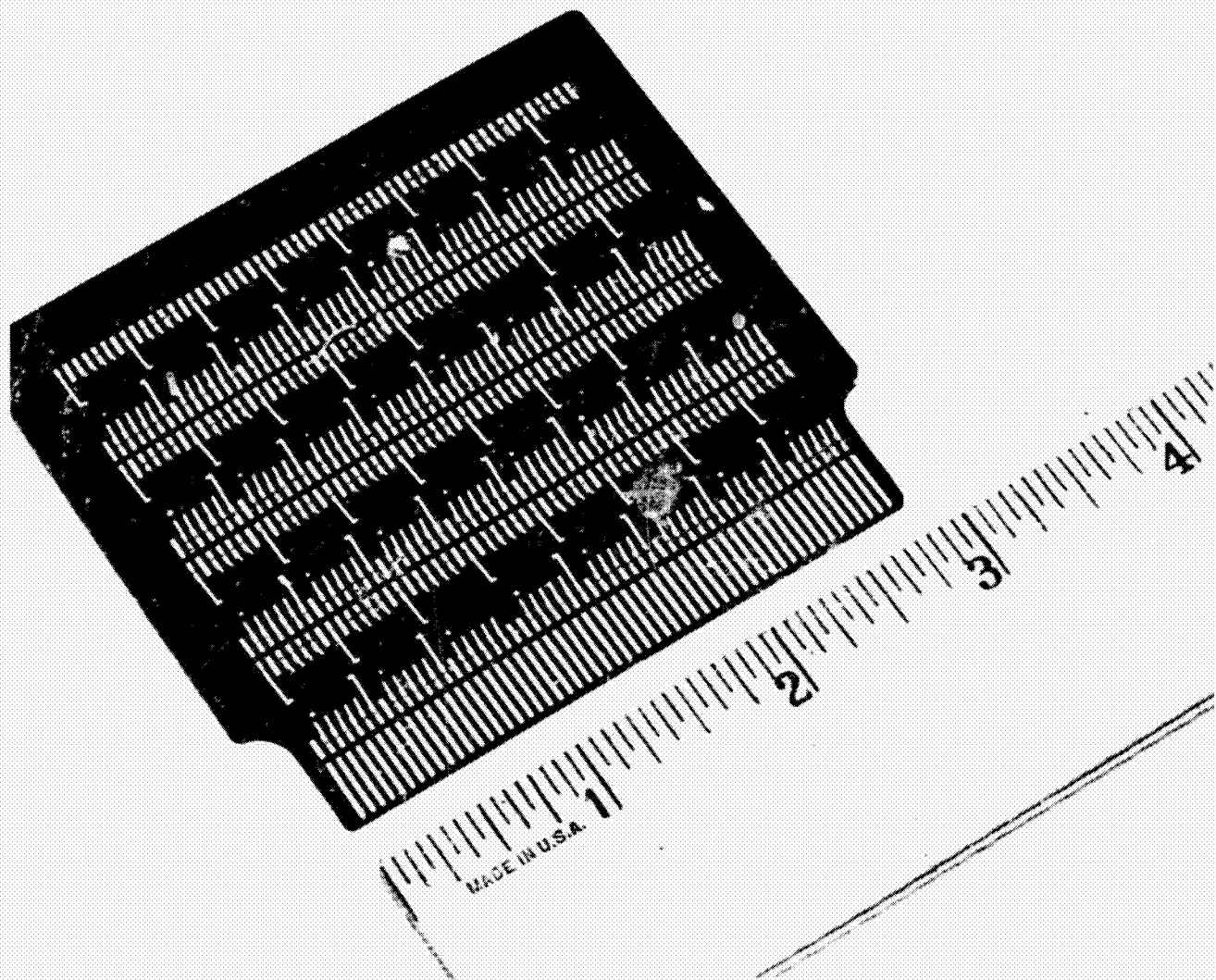


Figure 30-16—Fully assembled board.

**N67-31593**

**31. THE INTEGRATED-CIRCUIT CONTROL AND TIMING SYSTEM OF THE  
HIGH-ALTITUDE ROCKET-RADAR PROJECT**

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This report covers the work accomplished in designing an integrated-circuit control and timing system used aboard the high-altitude rocket radar launched at White Sands, New Mexico, USA on June 30, 1965, and May 1966. The system has been designed with basic integrated-circuit modules which have been programmed in a particular manner for this project, but which are designed so that they can be programmed in many alternative configurations such as shift registers or counters of various lengths. The important points discussed are: The design of integrated digital circuits into programmable and functional three-dimensional modules, the voltage margins and noise sensitivity obtained, the use of a nonmagnetic interconnect material in welding, a clear encapsulation used for the modules, the unique method of integrated-circuit packaging, and an analysis of the failures that have occurred in the integrated circuits on this project to date. A discussion of how the specific method of failure analysis has upgraded the integrated-circuit manufacturer's state-of-the-art in his production methods is also presented. A high-reliability integrated-circuit inspection plan, an outgrowth of the above failure analysis, is now being used on the Mariner-Venus '67 project to procure integrated circuits. It also is discussed.

**INTRODUCTION**

This report covers research and development done on an integrated circuit system incorporated into the flight tape recorder of an Aerobee rocket launched at White Sands Missile Range, New Mexico (USA), June 30, 1965, and May 1966. An integrated-circuit Hi-Rel specification, which has been generated with the knowledge gained from this work, is also discussed.

The work done on integrated circuits was accomplished with the idea of developing a system which would be valuable for the future use of integrated circuits in space research. General philosophies were developed in the packaging and electrical design of functional modules. The

integrated circuit system is part of the flight tape recorder system, and is a self-contained control system. Its functions are to pulse the radar transmitter at a fixed rate, insert a digital pattern on two of the six channels of the flight recorder, and command the flight camera that takes pictures of the location in which the radar is pointing.

The prime purpose of these launchings and subsequent launchings is to transmit to the surface of the desert and receive echoes from altitudes up to 125 miles above the surface. The echoes are recorded by the flight magnetic tape recorder and also are telemetered to a ground station. These echoes will be analyzed in detail as to shape and amplitude to determine if these analyses can be related to surface structure and terrain characteristics.

## SYSTEM CONSTRAINTS

The following is a list of certain criteria which were imposed on the design of this system:

1. Develop a self-sustained master clock for the control system. This clock will be used to:
  - a. Trigger the radar transmitter at 150 pps.
  - b. Trigger the flight camera at the rate of once every 6.8 seconds.
  - c. Insert a pseudo-noise sequence on two tracks of the six-track flight tape recorder.
2. Use the absolute minimum weight and volume.
3. Design of the prototype stage must be accomplished in 2 months.
4. Use modules or components that can be easily replaced in the field.
5. Satisfy the environmental parameters:
  - a. 6 g's 20—2000 cps, three axes.
  - b. 10 g's white noise, three axes.
  - c. 100 g's, 1 msec. shock, three axes.
  - d. Operate from 0° C to +70° C.

## DESIGN PHILOSOPHY

It has been demonstrated in past flight programs such as Ranger, Mariner Venus, and the Mariner Mars, that a maintainable system-interconnection scheme requiring minimum electrical and mechanical interfaces is of prime importance. This approach, based on weight and geometry constraints, may complicate the functional grouping of electronic components and result in the

use of sophisticated parts and module-interconnection schemes. However, it is more desirable to sacrifice optimum module design than to experience system-interconnection degradation due to handling.

It is believed that the system designed satisfied the criteria. The primary reason for this is that the packaging and electrical design were done, as much as possible, in parallel. In this way, the electrical design was greatly influenced by thinking in terms of logic functions of the system rather than discrete flip-flops. The external programming or the different modes of wiring the system were designed by knowing in advance which functions could be brought out physically. In all cases, the approach was kept as general as possible to allow the work to be applicable to future systems.

## DESIGN APPROACH

The design was started with the selection and qualification of the integrated circuits to be used. Following this, the electrical and packaging design was accomplished.

### Integrated Circuit Selection and Qualification

In 1964, a contract was let to perform a worst-case analysis on a four-transistor flip-flop and a NAND gate. The flip-flop had buffered outputs, was capable of being externally reset or set, and used diode-transistor logic. The worst-case analysis confirmed our thoughts that excellent noise and voltage margins could be obtained with this particular circuit design. The worst-case analysis was performed, assuming the use of specific high-reliability standard components. The worst-case analysis was weighted in terms of the particular components used. In other words, not only were limits placed on circuit function, but realistic and proven values were used for component parameters. As an example, when it was desired to know the actual voltage-drop variance of a particular

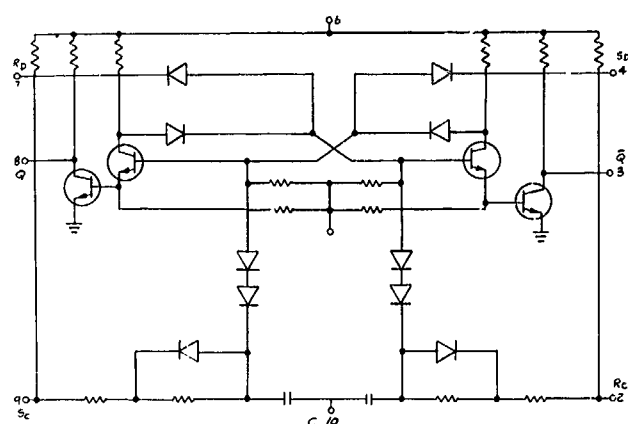


Figure 31-1—Binary element, SE124G.

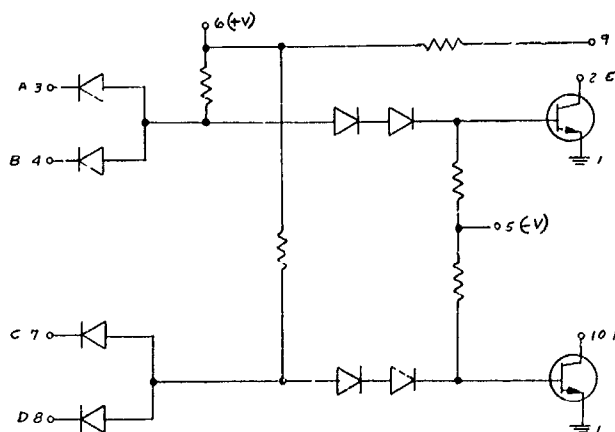


Figure 31-2—Dual NAND gate, SE115G.

diode with specific currents used, the measurements were made to determine these values.

In the fall of 1964, it was decided to investigate circuits that would complement the standard component line of available flip-flops and NAND gates. Also, the High-Altitude Rocket-Radar project requirements demanded the use of integrated circuits because of the severe volume and weight constraints. In reviewing the literature, it was found that two manufacturers were producing integrated circuit flip-flops with circuits very similar to our worst-case flip-flop and NAND gates (Figures 31-1 through 31-4). Several units were procured from both manufacturers and tests were performed. These tests determined how well each manufacturer met his published specification and how uniform about a mean the particular parameters of interest were. The integrated circuit used is a monolithic silicon substrate fabricated by the planar technique.

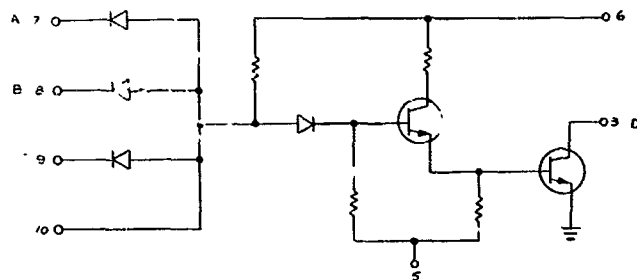


Figure 31-3—Power gate, SE110G.

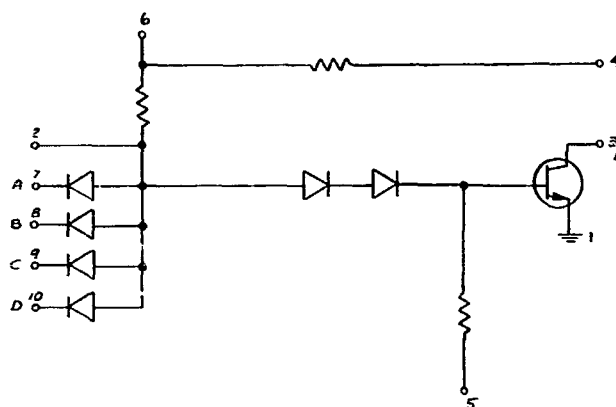


Figure 31-4—NAND/NOR gate, SE101G.

Since the integrated circuit is essentially a black box with an inaccessible interior, the test philosophy must be different from that required for standard components, such as a standard-component flip-flop. Thought must be given to making external measurements which will be meaningful to the circuit margins available. The following tests were made:

First, a test was conducted to determine the current drain of each of the 10 to 15 parts procured from both manufacturers. This was done for two reasons: to determine how close to specifications the values would be and to establish the uniformity of current between one circuit and another. It was felt that this would be one way of establishing a process-control checkpoint of each company's product. It was found in both cases that the current matched the specified values; but there was, indeed, a significant difference between the two manufacturers in the uniformity of the current.

The next test was the loading test. Here, specific resistive and capacitive loads were applied to the outputs of the flip-flops. The B+ voltage was changed in an effort to discover what the actual drive capability of the flip-flops was with respect to each other and the specifications. The tests indicated that the drive capability was well within the specification. This was very encouraging. Also, indications of the integrated circuit's uniformity of transistor betas and resistor values were derived. It was found that the circuit that had more uniform current drain and also slightly higher current drain was able to drive more loads than the other unit. It should be noted that,



because of time limitations, some of these tests were run under only one temperature besides room temperature, but each test performed took this into account when the margins were calculated.

The next test was electrical noise sensitivity. Because the flip-flops have a capacitor in the clock line, noise sensitivity is dependent on the input voltage amplitude swing, as well as the rise and fall time and the pulse width. Another factor affecting noise sensitivity is the B+ and B- voltage levels. Since the power used on this project had to be minimum, a compromise had to be made between the B+ and B- voltages required for excellent noise sensitivity and low power drain. One of the disadvantages of this circuitry, for JPL's application, is that it uses 10-mc logic. Therefore, the input must be able to trigger the flip-flop with a pulse 100 nanoseconds wide. This means that the high-frequency noise sensitivity will be worse than low frequency. Pulses were fed into the trigger line, and the rise times and amplitude were varied to determine margins. The B+ and B- voltages were changed and the different results noted. It was found that by increasing the B+ voltage by 1 volt (4 volts to 5) the input noise-pulse amplitude would have to be increased by approximately 20 percent to trigger the flip-flop. This increase is necessary because of the back bias on the input-trigger circuit changing with increasing B+ voltage. It was found that a good compromise of noise sensitivity versus power drain was to use +5 and -2.5 volt as the supply voltages. The input-noise sensitivity for a 1-usec pulse is approximately 1 volt. It was also realized at this time that, later in the testing of the first complete system, the B+ and B- voltages may be changed to allow for wider voltage margins.

Another important method of deciding which integrated circuit would be used was to visit the manufacturers to see, firsthand, the process controls used. This visit was used to determine which company had a better understanding of what was required to produce a reliable part and also to determine what delivery dates could be expected. When all of these tests were complete, the company was selected.

### Electrical and Logic Design

A logic system was required that would contain a master oscillator, command the radar system to transmit at the rate of 150 pps, and generate a camera trigger pulse synchronized with the radar pulse and occurring approximately once every 7 seconds. The master oscillator had to be of high enough frequency so that reasonable accuracy could be obtained on range information by counting the clock track pulses between the transmitted pulse and the echo in the adjacent track. Also, the master oscillator pulses had to be put on the tape in such a manner as to have a cyclic identity. A sequence had to be established of a length that would enable one to identify the reversal time of the recorder and the missing echoes during this period.

The oscillator frequency had to be easily changeable by at least 25 percent. The radar trigger frequency had to be flexible, as well as the number of camera pictures to be taken. It was

decided, therefore, to build a system which would satisfy the nominal requirements and yet be as flexible as time and budget would permit (Figure 31-5).

The clock frequency decided on was 76.65 kc. The frequency was determined by considering the frequency response of the tape recorder and also by arriving at a desirable range resolution. In other words, the amount of time between the transmitter pulse and the echo could be resolved to  $\pm 6 \mu\text{sec}$ . A decision had to be made on the technique to be used to divide the clock down to two different submultiples, one being pulses occurring 150 pps and the other, pulses occurring approximately once every 7 seconds. The radar transmitter pulse repetition rate dictated the need for the 150 pps. The camera system did not place a strict requirement on the number of pictures that should be taken, but a range of 3 per second to 8 per second was deemed desirable. A decision was made to use a 9-bit, pseudo-noise (PN) generator to divide down by 511 from the master clock to the radar trigger rate of 150 pps. This would be used instead of a 9-bit ripple counter because of the problems inherent in such a counter. The problems of a 9-bit counter are: One, the fact that each flip-flop in the chain changes state in series individually — this means that a noise pulse on any particular trigger line needs only the energy (volt-microseconds) to trigger one flip-flop for the counter to be noise sensitive. In a PN generator, all flip-flops are triggered at once. Therefore, the trigger current necessary to shift the information is nine times that of the ripple counter.

The PN generator is a 9-bit shift register with nonlinear feedback. The feedback is set up so that the register will not stop shifting at the end of its cycle, but be reset automatically. The sequence at the output will be a unique identifiable sequence whose cyclic period is that of the clock pulse repetition rate divided into the bit length of the register. In other words, at the clock rate of 76.65 kc, a 9-bit PN generator ( $2^9$ ) would have a sequence period of

$$\frac{511 \text{ pulses}}{76.65 \times 10^3 \text{ pulse/sec}} = 6.7 \text{ msec.}$$

The PN generator module was designed so that the outputs of all the flip-flops had leads attached which extended out of the module and also the important gate inputs that controlled the length of the register were brought out. In other words, the PN generator is a functional module that can be wired externally to be a 2—9 bit shift register. It can also be wired to be a 6—, 7—, or 9-bit PN generator. Therefore, this module is a very versatile piece of instrumentation for systems construction and use. Flexibility has been achieved and yet the amount of power, volume, and weight of the module is at a minimum. The module, as well as the whole system, was designed to work with power-supply voltage margins of  $\pm 10$  percent over a temperature range of  $-20^\circ$  to  $+70^\circ \text{ C}$ .

The camera trigger rate is reduced another two orders of magnitude from the radar trigger. Therefore, the use of another 9-bit PN generator was investigated for dividing down the radar trigger signal. The radar trigger (150 pps) divided by 511 is one pulse occurring every 3.4 seconds. Therefore, a second 9-bit PN generator was used with one flip-flop to divide down by two to make the time between camera pulses 6.8 seconds.

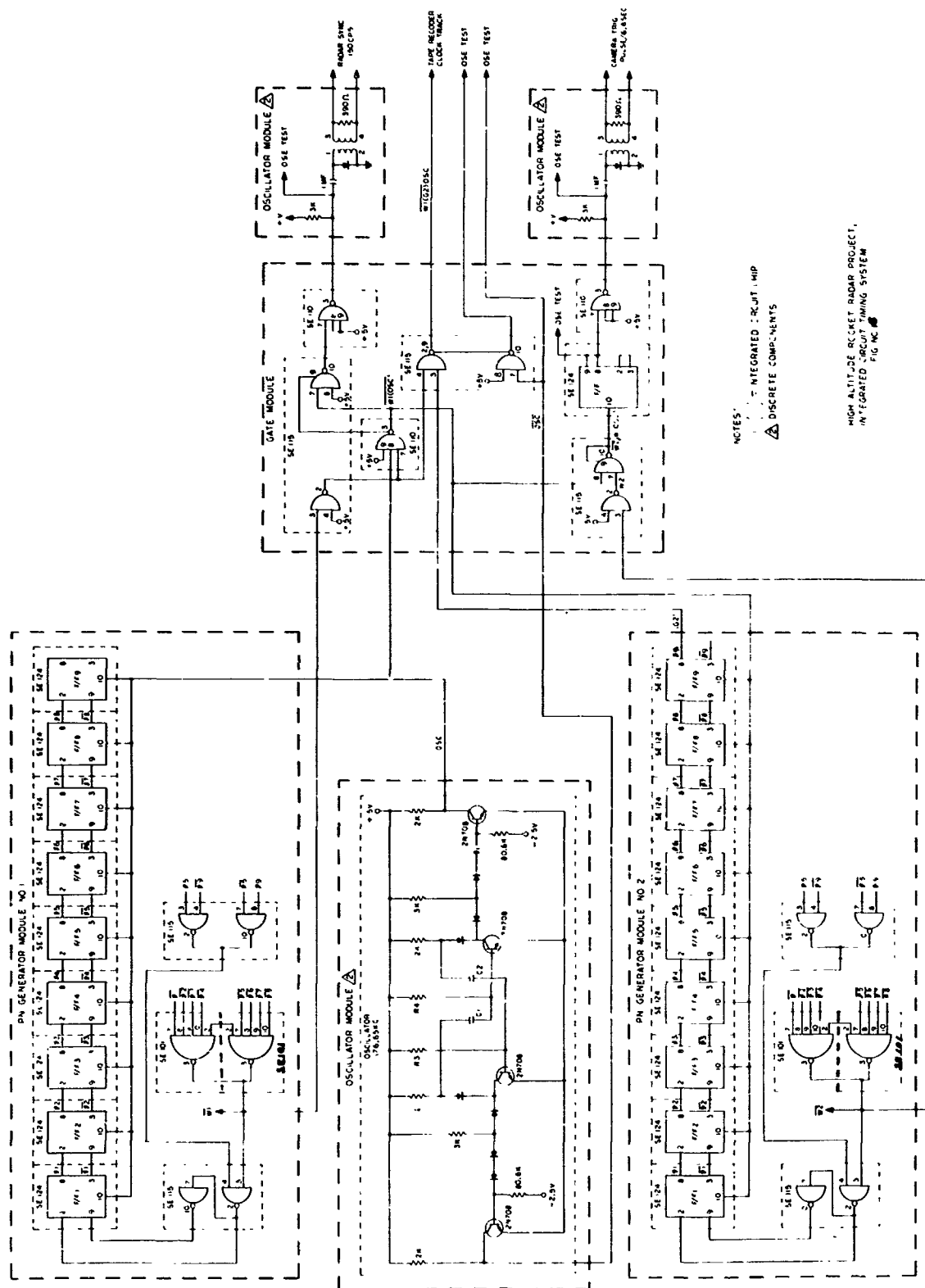


Figure 31-5—High-Altitude Rocket-Radar project, integrated circuit timing system.

Since the two PN generators did not include the miscellaneous gating logic necessary, a module was designed as a miscellaneous integrated-circuit module. This module was designed so that it could be enlarged to hold all those integrated circuits, such as gates and flip-flops needed for the logic, but not part of the PN generators. This module was called the "gate module."

Since the oscillator could not be designed easily using integrated circuits, standard components were used. A separate module was designed for the oscillator, including the interface circuits. Instead of connecting the B+ (power-supply voltage) of the oscillator to the interface circuits internally, two points were brought out of the module and the connection was made externally. In this way, the two points could be tied together or a separate voltage could be used on the interface circuits. For instance, if it was found that at some time in the project an interface circuit should put out a larger amplitude pulse for better triggering margins, a separate higher B+ could be tied to just the interface circuits, enabling the minimum power to be used.

An important design parameter was to try to ensure that the highest priority job of the logic, that of triggering the radar, was accomplished by using the minimum number of series elements between the radar and the oscillator. If the logic is examined, one sees that there seems to be an extra gate before the interface circuits. The reason for this gate is to keep the interface circuit turned off, thus saving a considerable amount of power, since the duty cycle is very low. There are two other gates used for ensuring that no false triggers are given to either the radar or the camera. There are "glitches" or partial voltage swings which occur each time the PN generator is triggered. However, since only the correct one is wanted for triggering, the input trigger and output are "anded" so that there is only an output from this gate in synchronism with the input trigger.

The digital pattern which is put on two channels of the tape recorder is RZ. This pattern will have a 1 plus voltage or a 0 zero voltage every 511 oscillator bit times, in a unique sequence every 3.4 seconds.

## PACKAGING DESIGN

A review was made of the weight and geometry available to package the recorder timing circuits. Particular emphasis was placed on the use of vacant cavities in the tape recorder chassis in order to provide electrostatic-noise protection and maximum utilization of weight and geometry (Figures 31-6 and 31-7). The cavity selected to house the control electronics was 1-1/2 inches by 1 inch by 6 inches. The cavity volume of 9 cubic inches could only be realized with the use of integrated circuits. It was estimated that if the equivalent number of discrete components were used (approximately 1000), these components would occupy a volume of 6 inches by 6 inches by 1 inch and would require 16 welded cordwood modules. This volume would require an additional chassis and would increase the noise sensitivity of the circuits because of increased wire lengths and increased exposed surface area.

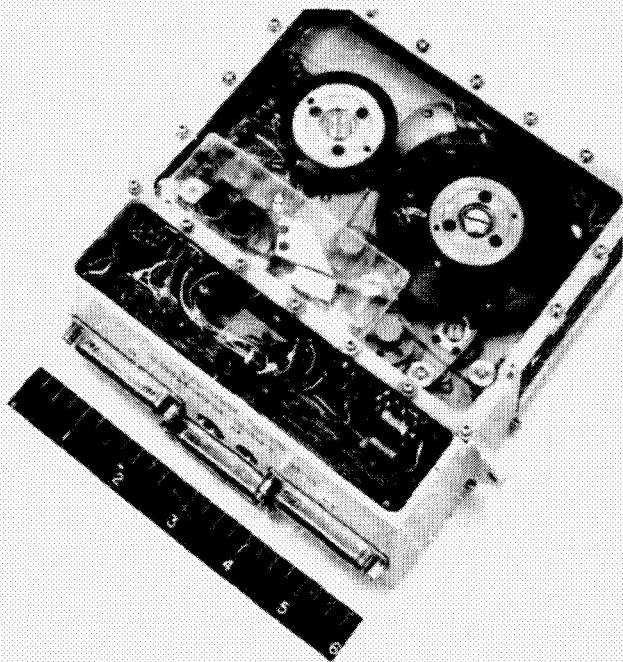


Figure 31-6—High-Altitude Rocket-Radar project, tape recorder, side A.

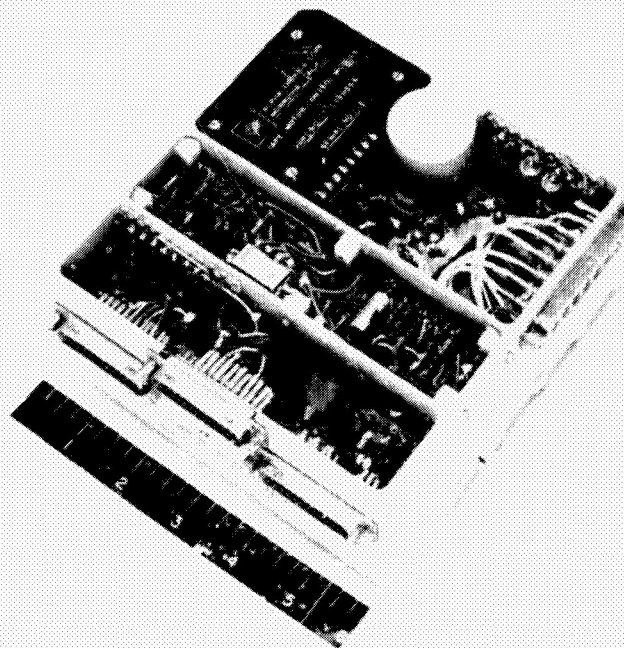


Figure 31-7—High-Altitude Rocket-Radar project, tape recorder, side B.

The geometry of the cavity dictated a welded-cordwood-module packaging approach. Integrated circuit flat-packs were selected over TO-5 cans because of increased volumetric efficiency. A system interconnect scheme was designed using a standard Teflon "hook-up" wire harness on a prewired glass epoxy rib located between the modules and attached to the subassembly structure (Figure 31-8). Nine multiwire splices were positioned in the rigid harness to minimize wire density. The harness height with respect to the top of the module was located to optimize wire

routing and facilitate system wiring changes. Module riser wires were designed to protrude from the top of the modules and be bent to form eyelets for a soldered system interconnection. Preliminary module design indicated that functional grouping of circuits, module programming, limited replacement of critical discrete components, and additional area for growth were feasible.

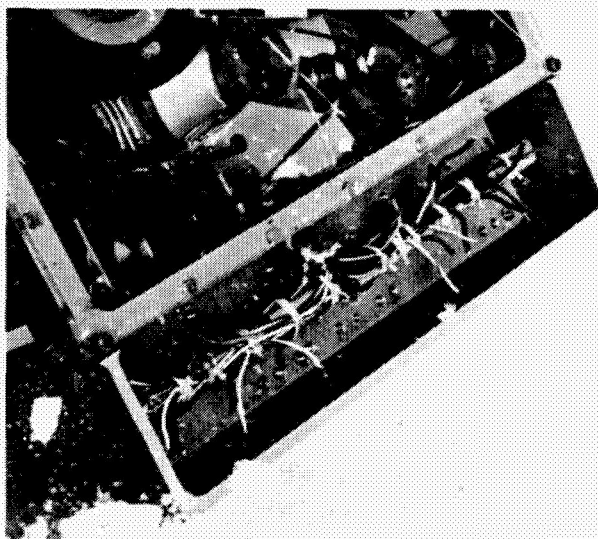


Figure 31-8—High-Altitude Rocket-Radar, integrated circuit modules in system cavity.

The circuits were grouped into three distinct modules. A PN generator module was designed, using integrated circuits to satisfy two logic functions and provide for a maximum amount of external programming (Figure 31-9). A gate module was designed using integrated circuits packaged so that additional circuit chips



could be added to the end of the module to accommodate minor system redesign (Figure 31-10). An oscillator module was designed to accept all the discrete components in the system and provide for external forked terminals to accept the frequency-dependent components (Figure 31-11). These modules were designed to attach independently to the subassembly web by two internal mounting screws for ease of replacement. Internal hollow epoxy standoffs provide structure and bearing surface for the mounting.

Future applications for a nonmagnetic module-interconnect ribbon influenced the decision to select 0.010 inch by 0.021 inch alloy 45 over standard nickel interconnect ribbon. JPL's prime effort is concerned with large spacecraft data systems; therefore, a search for a good nonmagnetic material to satisfy spacecraft magnetic requirements has a high priority. Previous experience had indicated that alloy 45 is a suitable material for welding although not completely qualified. Weld schedules were developed for the use of alloy 45 interconnections, and it became apparent that the weld force and energy parameters were more critical (narrower process margins) than if nickel had been used.

Some problems were encountered in welding alloy 45 to dumet diode leads. Some welds exhibited blow holes of less than 10 percent of the cross-sectioned area and from 15 to 20 percent of the weld depth (Figure 31-12). It was decided that the degradation was permissible on this project, but consideration should be given to the limitations of this interconnect material for future projects.

An integrated circuit chip holder was designed to eliminate integrated circuit-lead bending required for module interconnection because of lead reorientation and to minimize abuse during assembly (Figure 31-13). Experience has shown that 0.005 inch by 0.016 inch integrated circuit leads are extremely fragile and should not be relied on for structure prior to the module encapsulation. The chip holder was designed with a cavity to accept the chip and provide 0.016-inch diameter alloy 45 risers for chip lead attachment. The chip holder risers were then used for the next level of

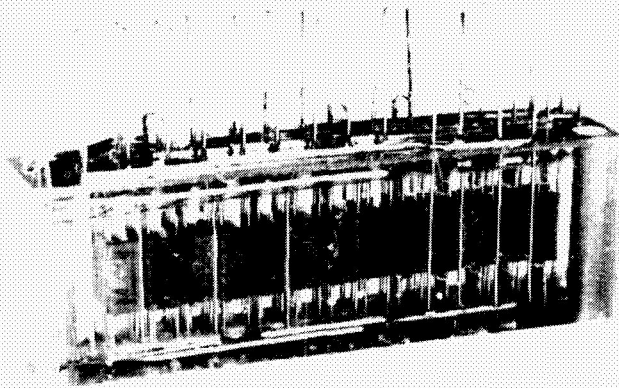


Figure 31-9—High-Altitude Rocket-Radar, integrated circuit PN generator.

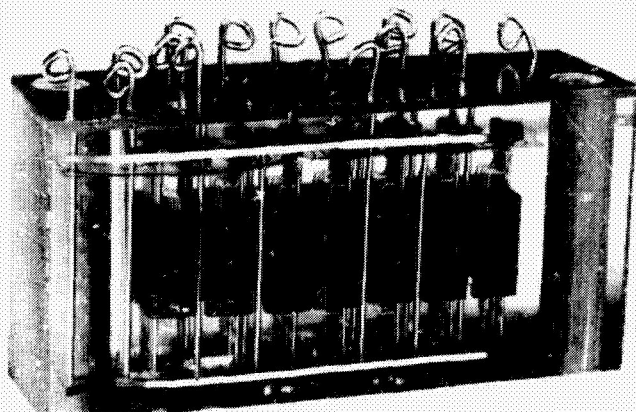


Figure 31-10—High-Altitude Rocket-Radar, integrated circuit gate module.

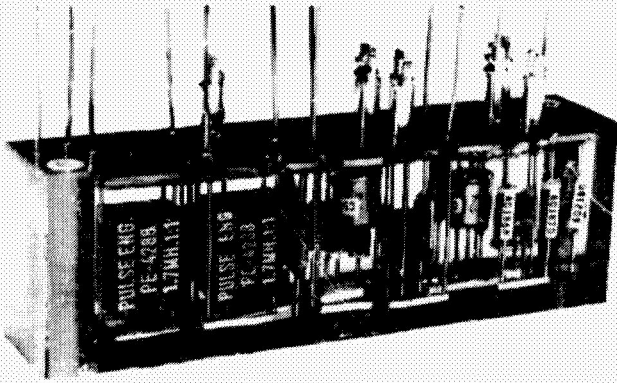


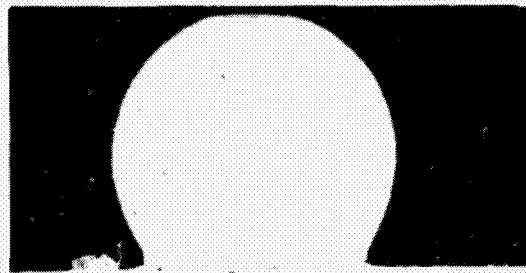
Figure 31-11—High-Altitude Rocket Radar, oscillator module.

interconnection. The capability of using continuous risers through the chip holder to minimize module risers was available but was not used on this program.

It was decided at the prototype design review, because of evidence of seal abuse at the flat-pack lead exits, to provide lead strain relief between the chip and the holder risers (Figure 31-14). Tooling designed to shape the lead proved satisfactory. No problems were encountered in the use of the chip holder, and its use is recommended for future application.

Standard JPL opaque encapsulation systems (Stycast 1090) were not considered for this program because of JPL's limited experience with integrated circuits and the resulting need for rapid visual and mechanical access to the chips for troubleshooting and failure analysis. Module interconnection layers were held to a minimum and the modules were encapsulated in a clear, resilient polyurethane (Figure 31-15). Component traceability was maintained throughout all assembly levels.

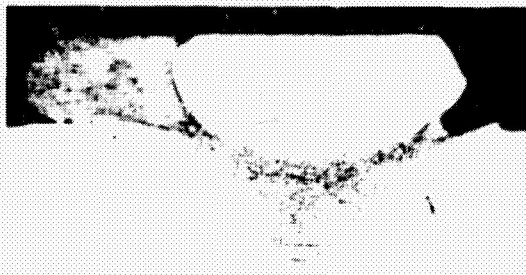
Resin LD213 was procured from DuPont and the curing agent was formulated at JPL. Sterilization and "outgassing" tests were conducted to determine if this material could be



WITHOUT BLOWHOLES  
ALLOY 45 TO DUMET



WITH BLOWHOLES  
ALLOY 45 TO DUMET  
FRONT VIEW



WITH BLOWHOLES  
ALLOY 45 TO DUMET  
SIDE VIEW

Figure 31-12—High-Altitude Rocket-Radar, control system alloy 45 to dumet interconnection photo-micrographs.

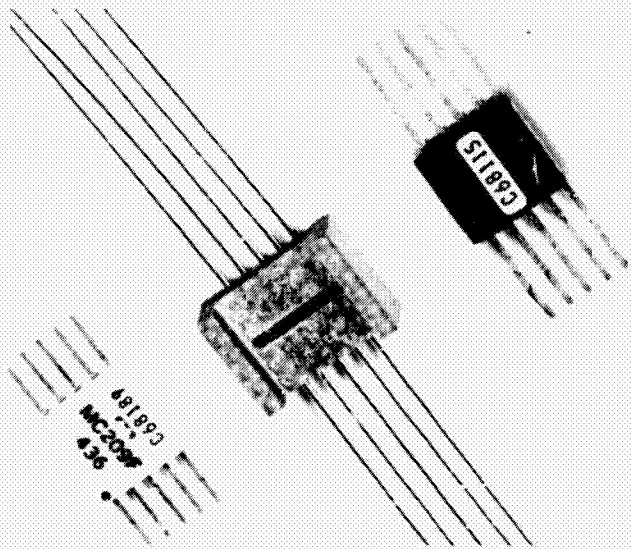


Figure 31-13—High-Altitude Rocket-Radar, integrated circuit chip holder.

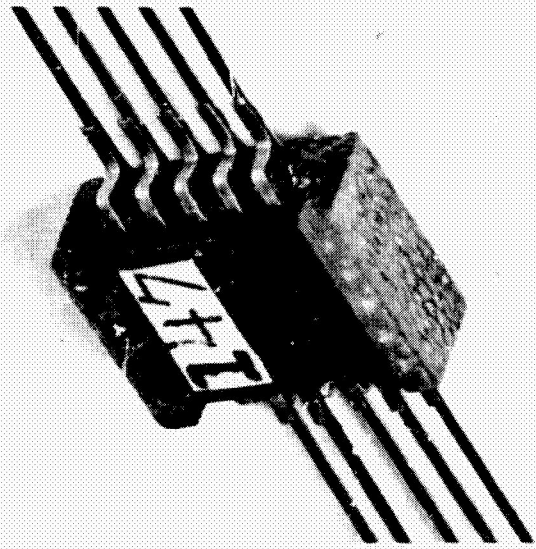


Figure 31-14—High-Altitude Rocket-Radar, integrated circuit flat-pack lead strain relief.

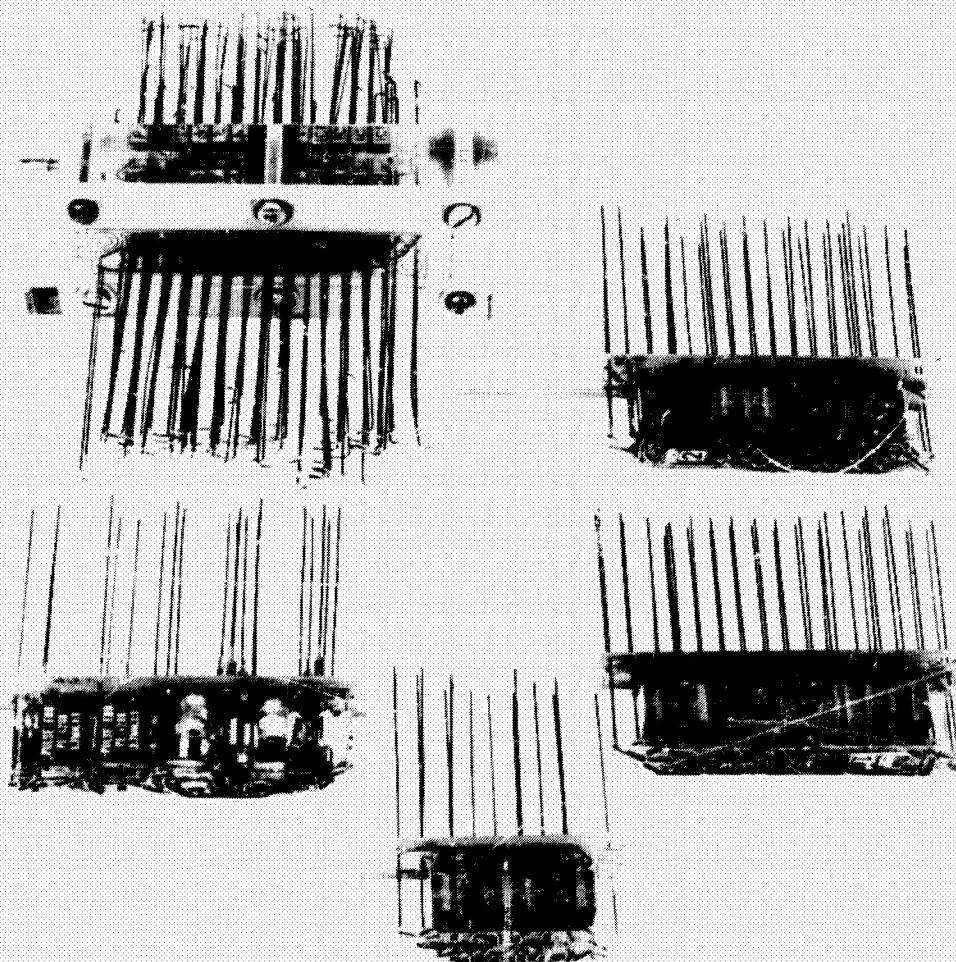


Figure 31-15—High-Altitude Rocket-Radar, control system module layout.



used in future programs. The following results were obtained:

1. Sterilization tests were conducted in an airtight oven at  $145^{\circ}\text{C}$  under an atmosphere of nitrogen for 108 hours. No significant change in material hardness was observed.

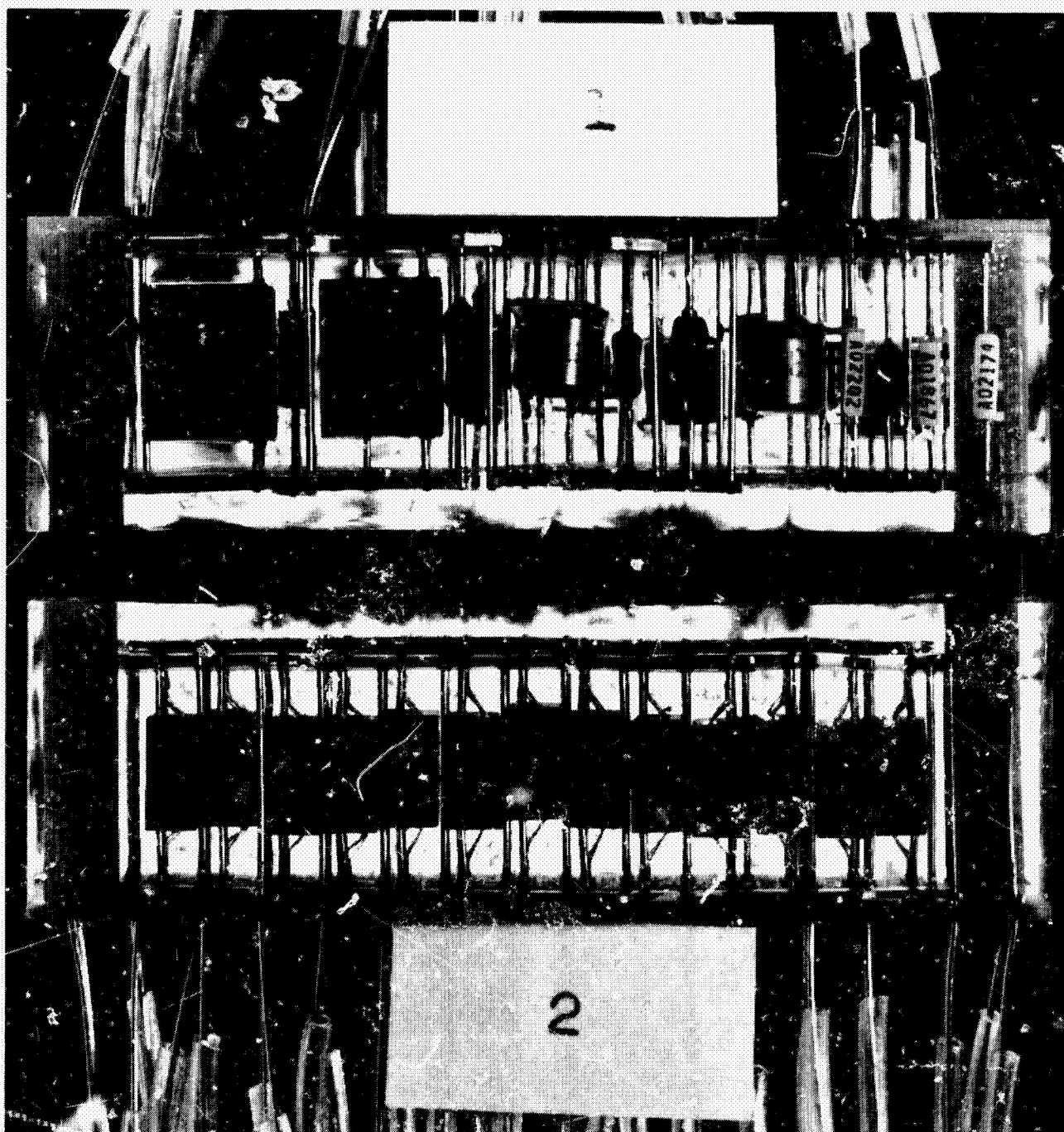


Figure 31-16—High-Altitude Rocket-Radar, polarized light stress photograph of LD213 resin system, oscillator and PN generator number 2 modules.

2. Outgassing tests were conducted at  $110^{\circ}\text{C}$  and  $1 \times 10^{-6}$  torr pressure. Total percent outgassing was 0.54 percent and the amount of volatile condensable material was 0.15 percent.

Modules were encapsulated and evaluated with polarized light to detect stress (Figures 31-16 and 31-17). The intensity of the colored streaks (fringes) is an indication of the internal stresses present around the components. These stress concentrations were found to be less than they are with clear, rigid epoxy (Figure 31-18).

The JPL contractor was funded to develop the technology required to use new encapsulation material. The limited shelf life of resin caused problems; in addition, the material was sensitive to humidity. New resin was procured and the following constraints imposed upon its usage:

1. Limit the resin exposure to air and purge the can with dry nitrogen after each application.

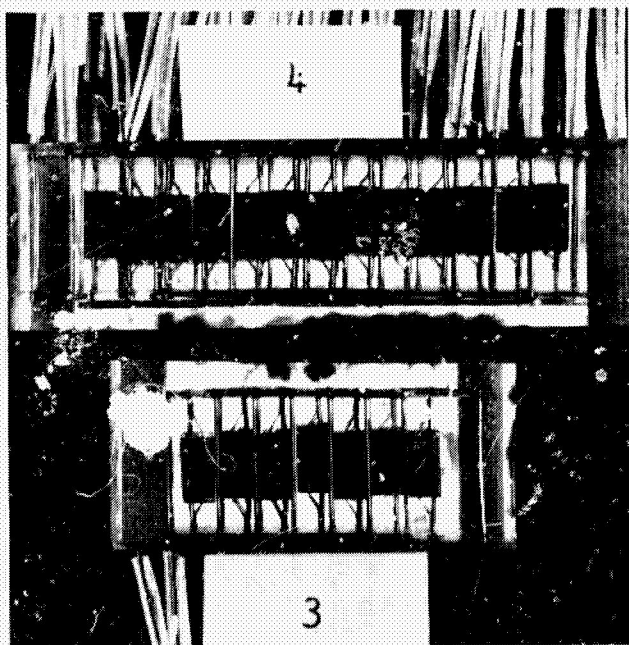


Figure 31-17—High-Altitude Rocket-Radar, polarized stress photographs of LD213 resin system, PN generator number 1 and gate module.

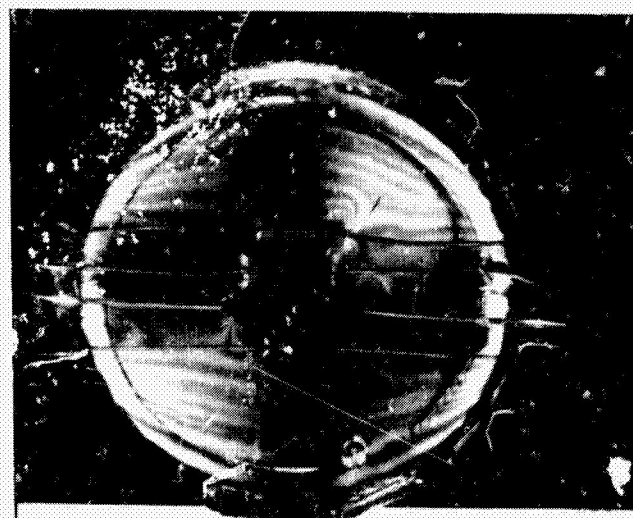
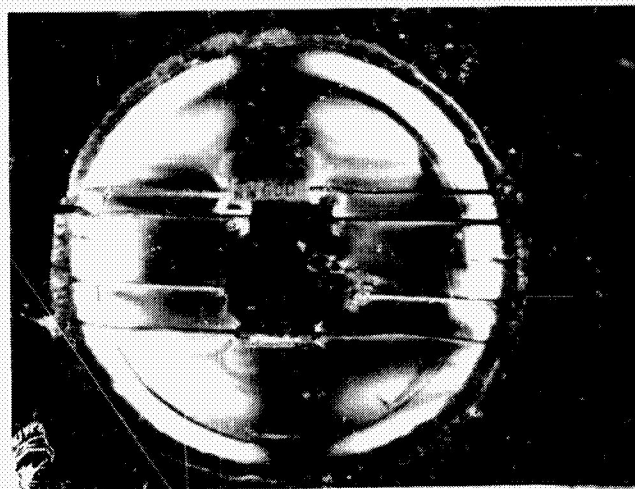


Figure 31-18—High-Altitude Rocket-Radar, polarized light stress photographs, epoxy and polyurethane samples.

2. Under the conditions stated in 1, consider the shelf life of the resin to be 1 week.

The encapsulation of the modules with the controlled use of LD213 proved satisfactory; however, its use on future programs is not recommended because of its limited shelf life.

A quality assurance plan covering receipt of materials through delivery was generated by the contractor and approved by JPL. The plan called for three mandatory JPL inspection points per module. Fabrication travelers were used to document part traceability and JPL source inspection signoff. Approximately 50 JPL source inspections were conducted on this program. To date, there have been no operational problems attributed to poor workmanship on the part of the contractor. System assembly at JPL had both in-process and final inspections.

#### INTEGRATED CIRCUIT PROCUREMENT

The integrated circuits were procured in September 1964 to a JPL specification written with the manufacturer to ensure a thorough understanding of the tests to be performed. The important constraints in this specification follow:

1. All parts to be visually inspected by JPL before their final encapsulation. This is primarily an inspection of whisker uniformity and color differences in passivation and could possibly be supplemented by X-rays taken by JPL incoming inspection.
2. All flip-flops to be screened to ascertain B+ current limits using a fixed voltage. The average power used by these units was reduced by 10 percent from standard off-the-shelf parts by this technique.
3. All parts to be 100 percent screened for their important parameters both before and after environmental testing.

Out of approximately 150 integrated circuits that were procured, there have been three failures. Two of the failures were isolated to punch-through in the crossover region between the plus voltage interconnection and the anode of D1, effectively shorting out D2. Figures 31-19 and 31-20 show the punch-through or bubble in the aluminum intraconnection going to D2 and the pin-hole in the oxide layer after removal of the aluminum. Figure 31-10 shows the components as they occur physically on the silicon substrate. Since these failures were not noted in the screening tests by the manufacturer or in the initial tests at the module manufacturer, it was concluded that the failure could have been caused by any of three reasons: One, that there was a voltage transient in the power-supply voltage during the testing by the manufacturer which exceeded the specified maximum voltage; two, that the oxide thickness between the two layers is too thin to be controlled accurately enough; three, that the potting of the module somehow put a stress on the chip that caused the failure. It is interesting to note that the manufacturer has since increased the thickness between these specific layers and has also redesigned the chip to minimize crossovers.

The third failure was a shorted capacitor. In attempting to accomplish a more thorough analysis of this failure, the chip was destroyed by mishandling.

During microscopic failure analysis, pre-seal visual inspection, and detailed discussions of possible problem areas in integrated circuits in general, many points were noted as items which should be stipulated in future procurement and inspection of integrated circuits. Some of these important points are:

1. X-ray inspection after vibration and centrifuge tests should be mandatory.
2. Ball-bonding equipment pressure and temperature calibration is extremely important to the reliability of the ball-bond and wedge-bond attachments.
3. Placement of ball-bonds in respect to each other and to the die surface is extremely important.

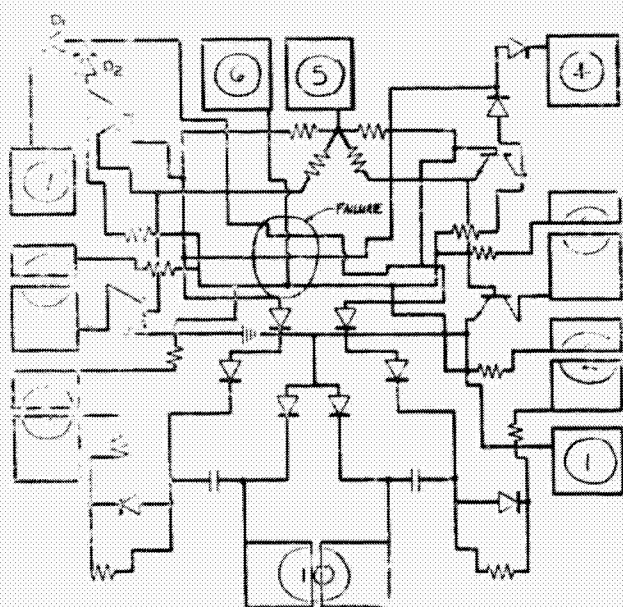


Figure 31-19—Binary element, SE124, physical layout of components on silicon substrate.

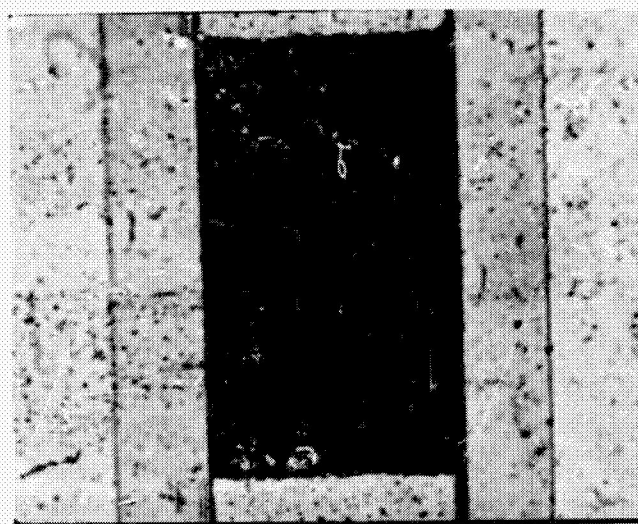
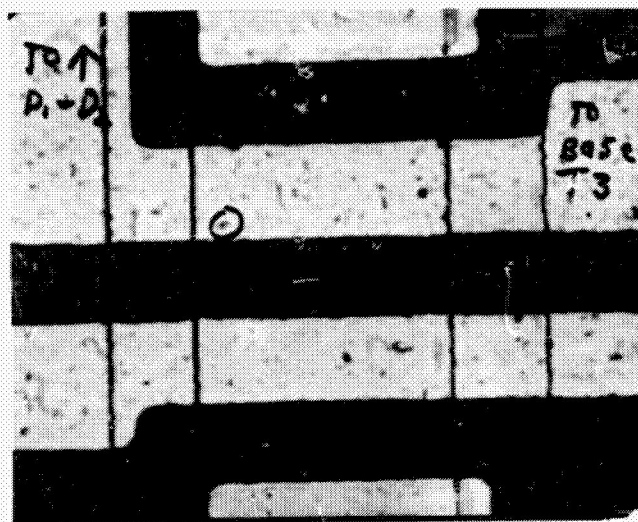


Figure 31-20—Photomicrographs of silicon chip failure areas.



4. Handling of the unattached die must be improved to eliminate the several scratches apparent on the majority of the die.
5. Handling the external leads needs extreme improvement in order to be able to use the integrated circuits without causing severe stress on the package when straightening the leads.
6. The amount of gold preform used in die attach must have high-power visual inspection to ensure that minute gold modules in the preform do not exist.
7. Visual inspection is necessary to guarantee that no pigtailed are left attached to the wedge bonds after the bonding operation.
8. Higher power visual inspection of the die surface is necessary to ascertain whether there are any foreign particles on the die surface and whether there has been misalignment of the die or any imperfections which may affect the lifetime of the chip.
9. Serialization of circuits at die attach is mandatory for traceability purposes.

The foregoing criteria as well as several others were negotiated with the integrated-circuit manufacturer and an integrated-circuit specification was written by JPL and the manufacturer of the integrated circuits. To apply many of the aforementioned criteria that have never been applied before, three categories of parts were developed -- A, B, and C parts. The "A" category is those parts that are theoretically "perfect" after being through all tests, including visual, electrical, environmental and X-ray. The "B" category is those parts that do not meet some criteria in the Hi Rel inspection and testing, but that do pass the normal integrated-circuit manufacturer's specifications. The "C" category is those parts that do not meet the manufacturer's standard criteria. The "A" and "B" parts are procured; the "C" parts are not.

A procurement of several thousand circuits has been initiated for the Venus '67 spacecraft data automation subsystem using the above-mentioned specification.

## CONCLUSIONS

It is doubtful whether a standard-component logic system would have worked successfully with the noise environment on the rocket. This environment consisted of 125 kw of 100 mc from the radar transmitter and 5 watts of 248 mc and 20 watts of 234 mc from the telemetry.

The reliability of the system is believed to be improved by a considerable factor because of the discrete number of steps needed to fabricate a welded-cordwood module system of standard components as opposed to the number needed to fabricate this integrated system. Also, the ease

in procuring flip-flops and NAND gates, instead of procuring resistors, diodes, capacitors and transistors from several manufacturers is a tremendous savings in time and money.

It has been demonstrated in vibration and shake tests, as well as in flight, that the three-dimensional module, chip-holder design can indeed produce a reliable system. The module has since undergone shocks in excess of 8000 g's before a failure occurred.

The programming capability allowed a major interface change to be made weeks before the first launch without significantly changing the wiring of the system. Troubleshooting was greatly enhanced by the fact that many functions were brought out to satisfy the external programming requirements that would normally not be brought out. The PN generators can be connected as a shift register to expedite troubleshooting. A method of interconnection between modules and external points was devised that did not sacrifice the gain in volume brought about by the use of the integrated circuits.

The programming capability used in this project does produce some hardships in the testing phase. A handling fixture or connector would have to be developed for the next project. The system tests used about one-tenth of the interconnecting wires and therefore did not present the problems that testing a single unit represented.

The cordwood-module approach does not have the advantage of easy parts replacement that planar layouts would have; but before a particular method of packaging is decided on for a project, the highest priorities must be resolved: Reworkability, functional flexibility, volume, or form factor?

The breadboard system originally fabricated for this system used TO-5 cans. This breadboard system is still on life test at room temperature; there have been no unit failures with over 520,000 unit hours of operation. The results that have occurred in the procurement of integrated circuits for the Venus '67 spacecraft are still preliminary, but several important points have been learned that will be applied to future space programs.

The primary point is that severe rejection rates have occurred at the die level. Dies have been found discolored, with severe contamination, and with resistor traces shorted to other resistor traces. This rejection has been very costly because it has occurred after the dies were attached and ball bonding has occurred. Future programs will demand a tight screening program at the slice level after depositing the die patterns. At this point the dies are relatively inexpensive and can be screened very effectively.

Other points which have been made clear as needing more work in our specification are: (1) Closer specification of the amount of preform to be used with different sized die, (2) closer specifications on the curvature of the ball-bonding wire, (3) tighter control on pressure and temperature calibrations of ball-bonding equipment, (4) some stipulation as to the people that will work on the job, (5) one person at the integrated circuits manufacturer who spends full time overseeing the entire job from visual inspection through environmental to X-ray.

It is believed that the reliability of already reliable integrated circuits has been upgraded by JPL's continual thorough failure analysis in conjunction with the manufacturer and by the use of our Hi-Rel integrated circuit specification.

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**N67-31594**

**32. APPLICATIONS OF A COMBINED COUNTER/SHIFT REGISTER MODULE**

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Integrated circuit technology has progressed to the point that it is now practical to consider manufacturing complicated devices which contain a large number of components. Whole registers, or significant portions thereof, may be included in a single package. The counter/shift register is a particularly useful configuration. It can be used to simplify spacecraft telemetry encoders and at the same time it can provide logarithmic data compression.

**INTRODUCTION**

This paper is the result of speculations about possible uses of complex integrated circuit modules. The counter/shift register is a particularly promising example of what can be done when complex integrated circuits become available. This register can count as a normal binary scaler, and it can also act as a shift register. These properties make it adaptable to a number of tasks in data collection and handling equipment.

**THE COUNTER/SHIFT REGISTER MODULE**

Figure 32-1 is a drawing of the counter/shift register module as the author conceives it. There are a Counter Input and a Serial Data Input. Output data are in serial form also.\* Other than power supply and ground connections, only two more leads are required. One is for the Shift Clock, which causes the register to shift; the other is for a Count/Shift Command, which converts the register from a counter to a shift register.

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\*It would be handy for many applications to have parallel data input and parallel data output. Unfortunately, this would complicate the circuit and greatly increase the number of leads which would have to be brought out of the package. Because the module is very useful without parallel input and output, they have not been provided in order that the number of external leads be held to seven for any length register.

## USE IN A TELEMETRY ENCODER

### Accumulators and Commutating

The counter/shift register module just described should find use in spacecraft telemetry encoders. These encoders usually contain a number of accumulators which count pulses from the experiments. In order to transmit this data it must somehow be read out of the accumulators.

At present, a digital commutator scans the outputs of the accumulators, selecting four bits at a time to be connected to a digital oscillator. This oscillator then generates the PFM code which is transmitted. Some of the commutator hardware is included in the accumulator modules, thus minimizing the hardware required external to the modules. However, if counter/shift registers were used, the amount of external circuitry could be decreased even more.

### Proposed Application

Each accumulator, as accumulators are now built, requires numerous input and output leads, and the longer the register, the more leads required. The counter/shift register, however, requires only seven leads for any length register. Figure 32-2 shows how simple a system can be, using counter/shift registers. The box labeled SELECTOR controls the operation of the ACCUMULATOR counter/shift registers at the right.

Normally all of the count/shift command lines are at the logical zero level and all of the accumulators act as counters. Then, when it is time to read out the contents of one of the accumulators, the selector places a logical one on the associated count/shift command line. This freezes the counting action and prepares the selected accumulator to receive shift clock pulses.

The selector then resets the COUNTER at the left of Figure 32-2. This allows shift clock pulses to pass through the AND GATE to the BUFFER REGISTER and to all of the accumulators.

Only the buffer register and the accumulator that has been chosen by the selector are affected. Data shifts from right to left, out of the accumulator and into the buffer register. When enough shift clock pulses have passed to empty the accumulator, the counter closes the AND GATE and the transfer operation ceases. Data may now be read into the digital oscillator,

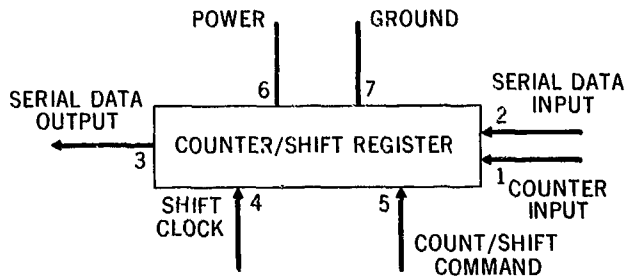


Figure 32-1—Counter/shift register.

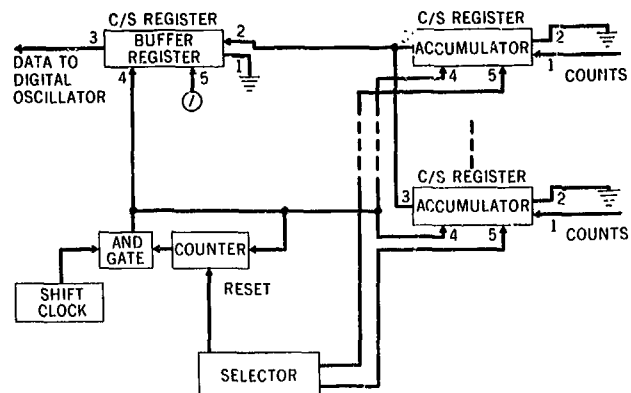


Figure 32-2—Telemetry encoder using counter/shift registers.

four bits at a time, by shifting the buffer register left four places at appropriate intervals.

### Advantages

There are several advantages in this approach. First, the logical interface between an accumulator and the rest of the encoder consists of only three lines. This is particularly convenient if the accumulator happens to be located in an experimental package. The system can also directly handle serial data from experiments which produce serial data. And because the buffer register has been provided, data may be rapidly read out of the accumulators so that the accumulators need be frozen for only a short time.

## LOGARITHMIC COMPRESSION

### S-T and Log Counters

On board spacecraft it has been customary to compress data from counters in one of two ways. Either S-T or logarithmic counters have been used. S-T counters count data pulses until the counters overflow; then they count clock pulses for the remaining portion of the data-taking period. Thus, when only a few pulses are received, the number is known exactly, but when many pulses are received, only an estimate of the number is obtained. The logarithmic counter is a little neater. It gives the exact count for small numbers of pulses and the approximate logarithm of the count for large numbers of pulses. Unfortunately, the logarithmic counter is much more complex than the S-T counter.

### An Easier Way

It is easy to modify the counter/shift register system shown in Figure 32-2 so that it will perform logarithmic compression. As a matter of fact, it is only necessary to add one flip-flop, one OR gate, and one AND gate! In this system the logarithmic compression is similar to the process of conversion to normalized floating-point format which is used in digital computers.

### Operation of Improved Encoder

Figure 32-3 shows the modified system. It operates as follows: First, the selector chooses an accumulator. Then it resets the counter and flip-flop. In its reset condition, the flip-flop causes the buffer register to act as a counter and causes AND GATE 2 to prevent shift clock pulses from reaching the counter. Shift clock pulses do pass through AND GATE 1, however. These pulses cause the selected accumulator to shift left. Data from the accumulator does not

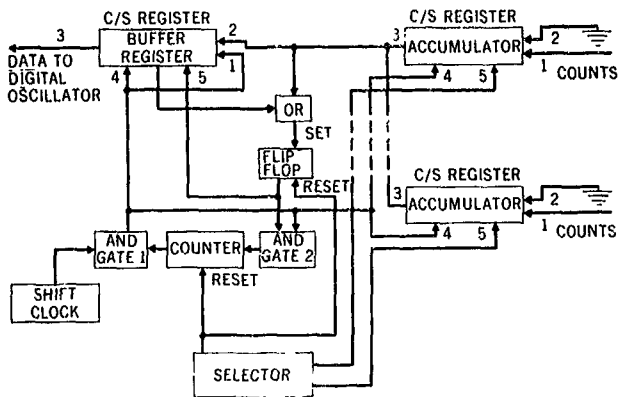


Figure 32-3—Telemetry encoder with logarithmic bit compression.

enter the buffer register because the buffer register is in the counter mode. Instead, the buffer register counts shift pulses.

Operation continues in this manner until a 1 appears at the output of the selected accumulator. The 1 causes the flip-flop to enter the set state. This changes the buffer register to the shift-register mode and opens AND GATE 2. At this point, the buffer register contains the count of the number of zeros which preceded the first 1 to emerge from the accumulator.

Now the buffer register and the selected accumulator shift left together until the count of leading zeros is at the extreme left-hand end of the buffer register. The rest of the buffer register contains the significant part of the data from the accumulator, followed by some trailing zeros. The count of leading zeros and the first few bits of the shifted data constitute the logarithmically compressed data; the rest is discarded.

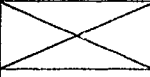
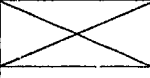
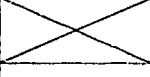
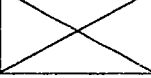
If, after a predetermined number of shifts, no 1's have emerged from the selected accumulator, the changeover to shifting, rather than counting, is initiated by the connection from an output tap on the buffer register to the input of the OR GATE. This requires that a parallel output be brought out from one stage of the counter/shift register, increasing the number of leads from seven to eight. In the following example the tap would be on the 5th stage, so that the 16th shift pulse would set the flip-flop.

### Example

An example will clarify the operation of the system. Suppose that the accumulators are 15 bits in length. If we retain the five most significant bits of data, our maximum error will be about  $\pm 3$  percent for numbers greater than 31. For smaller numbers there will be no error. To handle the maximum shift count of 15, we will need four more bits. Now if we use the 16th combination of the leading zero-count bits to indicate that the accumulator was zero, then the first significant bit of the data is redundant, because for all non-zero numbers it will always be a 1. Therefore, this bit may be discarded. The result is a compression of 15 bits into eight bits and the introduction of an uncertainty of  $\pm 3$  percent for numbers greater than 31. For longer accumulators the savings is even greater; 31 bits may be compressed into nine bits with  $\pm 3$  percent error. Table 32-1 shows the relationship between accumulator length, percentage error, and bit compression ratio. Given in Table 32-2 are several examples of accumulator contents and the associated compressed result for a 15-bit accumulator.

Table 32-1

## Summary of Bits Required and Compression Ratios Obtained

Accumulator length			7	15	31	63
Largest number			127	$3.3 \times 10^4$	$2.1 \times 10^9$	$9.2 \times 10^{18}$
Bits required in count			3	4	5	6
Maximum error	$\pm 3.1\%$ (4 bits retained)	Total bits	7	8	9	10
		Ratio	1	1.9	3.4	6.3
	$\pm 1.6\%$ (5 bits retained)	Total bits	8	9	10	11
		Ratio		1.7	3.1	5.7
	$\pm .78\%$ (6 bits retained)	Total bits	9	10	11	12
		Ratio		1.5	2.8	5.2
	$\pm .39\%$ (7 bits retained)	Total bits	10	11	12	13
		Ratio		1.3	2.6	4.8
	$\pm .20\%$ (8 bits retained)	Total bits	11	12	13	14
		Ratio		1.2	2.4	4.5

## Additional Comments

There are some small points which remain to be clarified. First, in order to discard the first 1 which emerges from the selected accumulator, it is only necessary to introduce a delay in the count/shift command line of the buffer register. This gives the shift clock pulse which produced the first 1 enough time to pass before the buffer register is converted to shift register operation. Second, no mention has been made of clearing the registers because they will always contain zero just before data is entered into them anyway. However, for the sake of generality it would be a good idea to include a clear line in the module design. This raises the lead count to 9, which is still quite modest.

## SUMMARY

An integrated counter/shift register module would certainly be a boon to spacecraft electronics. The application to encoders — counting, commutating, and logarithmically compressing — has

Table 32-2

## Examples of 15- to 8-Bit Compression

Accumulator contents	Compressed result	
	Zeros count	Significant bits
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 1 1	0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	1 1 1 0	0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	1 1 0 1	0 0 0 0
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1	0 0 0 0
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 0	0 0 0 0
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1	0 0 0 0
0 0 0 0 0 1 1 0 1 0 0 1 1 1 0	0 1 1 0	1 0 1 0
0 0 0 0 0 0 0 0 1 1 1 1 1 0 1	1 0 0 1	1 1 1 0
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 0 0 1	0 1 0 1
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	0 0 1 0	1 0 1 0

great potential. Such modules would have many other uses also. For instance, 10 12-bit modules would replace over 90 percent of the optical-aspect computer for the AIMP-D spacecraft. The computer presently contains 250 Series-51 integrated circuits. Even if a 10- or 15-bit register is impractical at the present state of integrated circuit technology, it would be advantageous to have 2- or 3-bit registers. These could easily be cascaded to make longer registers.

## ACKNOWLEDGEMENT

The author wishes to acknowledge the contribution made by Mr. Andrew B. Malinowski of the Flight Data Systems Branch. It was his suggestion that integrated construction of counter/shift registers might be feasible which led to this paper.

**N67-31595**

**33. A MICROELECTRONIC DATA SYSTEM FOR WIND-TUNNEL RESEARCH**

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This paper describes the development of an analog data and digital command control system for research aircraft models to be tested in the transonic dynamic wind tunnel at Langley Research Center. Microelectronic circuits are employed in this instrumentation and control system which could not have been developed with discrete electronic components. The instrumentation employed in test models includes: (1) 20 microminiature subcarrier oscillators, (2) 20 complex signal conditioning units which employ hybrid thick film and integrated circuit microelectronics, and (3) a 30-channel command decoder constructed entirely from integrated circuits. The gain and offset for the 20 data channels can be remotely programed. Artificial vibration and flutter can be introduced into the test model and controlled remotely by command, and there are provisions for maintaining angle of attack by a remote-control function. The microelectronic circuits and hardware that are used for these and other functions will be described.

**INTRODUCTION**

The increasing variety and complexity of NASA aerospace research facilities present many problems in instrumentation and electronics. The solution of these problems is as much a challenge to the designer as is the solution of the problems encountered in the development of systems for aerospace flight vehicles. An analog data and digital command control system is under development at the Langley Research Center. This system will be employed for research testing in the transonic dynamic wind tunnel. To meet the total system objectives, discrete electronic and microelectric devices are required. This paper presents a brief description of the system requirements and the design approach selected. Several critical design areas are discussed in detail.

**GENERAL CONSIDERATIONS**

The Langley transonic dynamic tunnel is used for research to determine the dynamic effects of turbulent airstreams on aircraft structures. Figure 33-1 depicts the test technique. Scale

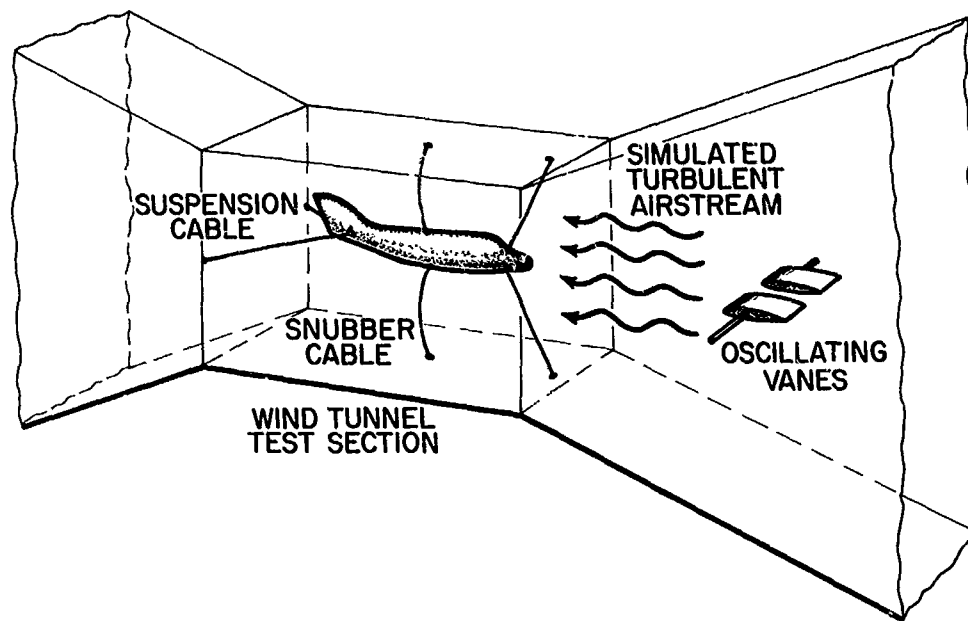


Figure 33-1—Sketch of test technique.

models of aircraft are suspended in the test section from two orthogonal cables; the cable ends are attached to the tunnel structure. Pulleys placed in the model allow the cables to move freely, enabling the model to have appreciable freedom of movement about three axes. In addition, several light snubber cables are used to prevent the model from striking the tunnel walls. Upstream from the model large vanes are oscillated to induce a sinusoidal turbulence. Freon gas is substituted for air in the tunnel to provide the proper conditions for testing the scale models.

An instrumentation system is required for both the transmission of data from transducers within the model and for the remote actuation of control motors within the model. There are three important considerations in the development of the instrumentation and control system. First, attachments which significantly alter dynamic performance or freedom of movement of the model cannot be used. Second, the fact that numerous tests are conducted on a single model at varying stream velocities and vane frequencies, precludes access to the model for setups between test runs since a minimum of 2 hours is required for the removal and replacement of the Freon gas in the test section. Third, the system must be adaptable to many models, which may vary appreciably in size and weight.

## SYSTEM REQUIREMENTS

The primary physical consideration in the system design is weight. If excessive volume is available, weight of the instrumentation must still be restricted to maintain total model weight within prescribed scaling limits. However, the use of Freon gas as the test medium does allow an increase in the scaled weight of the model within reasonable limits. Further, it is necessary to consider the distribution of weight in the model. The range of permissible weight for instrument



Table 33-1

## System Requirements

Data System	System Requirements
20 channels Millivolt input levels Variable gain and offset 200-CPS response Matched phased and amplitude accuracy Long-term stability	22 channels Remote control of gain and offset (20 channels) Remote control of aerodynamic control surfaces (1 channel) Remote control of three vibration motors (1 channel)

and control systems is 5 pounds for the smaller models and 10 pounds for the larger models. The permissible volume of the complete system is 200 cubic inches maximum.

Table 33-1 summarizes both data system and control system requirements for the larger models to be tested. To measure acceleration and structural forces, 20 low-voltage data channels are required. The variation in stream velocity and vane frequency for a given test regime produces a broad dynamic range of outputs from the strain-gage transducers. To achieve the required instrument sensitivity, gain change of the data channels is necessary. For example, full-scale transducer outputs may vary from 5 to 50 millivolts during a single run of the tunnel. Also, during a test, the model may have variable angles of attack which produce variable lifting forces. The transducers sense these forces as offset voltages added to the higher frequency voltages sensed from dynamic forces. If maximum dynamic sensitivity is to be achieved, it is necessary to null these steady-state voltages. The maximum frequency at which the vanes oscillate is 20 cps. However, higher order modes of dynamic forces are induced in the model. In order to obtain data for all significant modes, a channel frequency response of 200 cps is required. Further, time correlation of data from the 20 channels is significant in data analysis, a matched phase response of 5 percent at 200 cps is required. High-amplitude accuracy is not required, but long-term stability is important. If the weight and complexity of providing automatic or remote calibration is to be avoided, stability must be maintained for several days. The thermal environment of the tunnel may cover a 25 to 65° C range during this period of time.

A command control system is provided for two purposes. First, remote control of the data channels is necessary, as discussed. In addition, remote control is required for the actuation of trim controls to maintain angle of attack of the model and for the actuation of three small vibration motors located in the model to induce dynamic forces that are used to determine critical vibration and flutter modes. The speed of these motors must be controlled to produce a linear frequency sweep; a control channel is used for this purpose.

## SYSTEM DESIGN

Several techniques have been investigated for the instrumentation and control of models tested in the tunnel, but none of these techniques have satisfactorily met all requirements. Initially, the models were instrumented and controlled by an attached umbilical cable which routed a large bundle of wires to the control and data recording areas of the tunnel facility. The most serious disadvantage of this technique was the significant inertial forces which the cable imparted to the model through the umbilical connection. Also, cable motion produced noise in data channels; in some cases this motion resulted in damage to wires, necessitating repair between test runs. Tests were conducted to determine whether the suspensor cables could be used for model access, but the action of the pulley and cable generated prohibitive noise voltages over a wide frequency spectrum. These tests did indicate, however, that the snubber cables could be used satisfactorily. A system employing constant-bandwidth, frequency-modulated telemetry was then developed. This system contains only six data channels and is not capable of control functions.

A design study was conducted to determine whether microelectronic techniques combined with high-density, discrete electronic techniques could be employed to meet total system objectives. The promising results of this study led to a detail design and breadboard development of a system which is currently being packaged in final form for application within a model.

Figure 33-2 is a block diagram of the system design. Advantage is taken of the snubber cable for model access to avoid RF propagation which would increase system weight and complexity and add additional error sources in the analog data system. Commands are encoded in a PDM/PCM serial format and amplitude-modulate a 10-megacycle carrier. This carrier is transmitted to the model through a small coaxial cable attached to a snubber cable. The commands are demodulated and decoded to a serial binary code. The command system can provide a maximum of (30) six-bit command words. Since only 22 words are required in the system for the current testing program, eight words are provided as spares.

The data-conditioning systems in the model will in general consist of sensor amplifiers for strain gages and for angle-of-attack and accelerometer sensors. The commands for the data-conditioning systems provide for 16 offset and 4 gain control signals. The commands for the vibration-motor system include motor selection, start-stop, increase-decrease frequency, slow-fast frequency sweep, and reset. The commands to fly the model consist of on-off and forward-reverse controls for trim tabs on the model.

The outputs of the signal control and conditioning units modulate 20 voltage-control FM

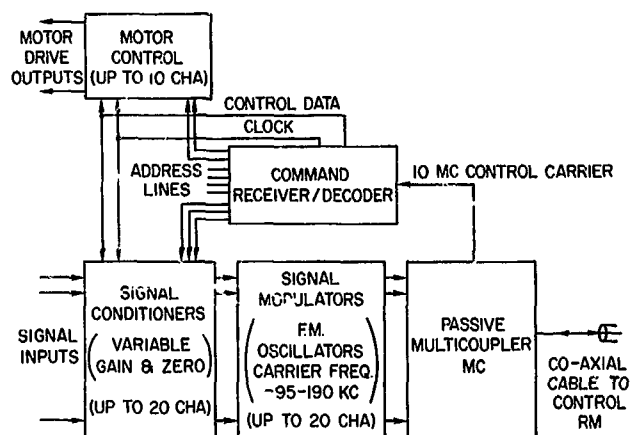


Figure 33-2—Simplified system block diagram.

oscillators. These oscillators are constant bandwidth types (200-cps response capability) and are distributed within a bandwidth of 95 to 190 kc. The oscillators are grouped in four blocks of five oscillators each. This arrangement was selected for two purposes. First, a modular approach is obtained wherein a data system of 5, 10, 15, or 20 channels may be selected as required. Second, the four blocks are frequency-translated and recorded on separated tape channels both to simplify and to take advantage of existing data-reduction equipment. A passive multicoupler combines the 20 FM channels. Since the data spectrum is significantly below the command carrier, the same coaxial cable is used to obtain the data from the tunnel as is used to insert command data into the model. The snubber cable is used for inserting power to the various dc-to-dc converters necessary to supply the various system voltages.

Specific parts of the system relative to the microelectronic development problems encountered are discussed in the following pages. However, Table 33-2 provides a summary of the components contained in the total system. The table is arranged to indicate the relative distribution of microelectronics and discrete electronics. On a total-component, part-count basis the 263 integrated circuits represent less than 8 percent of the total system number. If a conservative estimate is made that the integrated circuit is the equivalent of 15 discrete parts, approximately 4000 parts are replaced by these integrated circuits. This figure would more than double the total system count. The thick-film technology employs both screened resistors and discrete chips (transistor, diode, and capacitor). A count of 1930 such parts represents 58 percent of the total system component parts. The remaining 1129 parts are discrete electronic parts.

## SYSTEM DEVELOPMENT

A complete development history covering the various engineering trade-offs considered in the selection of each circuit design will not be presented. Instead, the major areas where microelectronics

Table 33-2

Distribution of Microelectronic and Discrete Parts in System

Unit	Integrated circuits	Screened circuits include active and passive chips	Discrete
Signal conditioner (data channels)	148	1320	780
Trim motor controls	25	30	223
Vibration motor controls	47	60	18
Command demodulator decoder	43	20	58
FM oscillators	0	500	9
Multicoupler	0	0	41
Total	263	1930	1129

is employed to a systems advantage and where microelectronics is not being employed because of systems limitations will be discussed.

As noted in Table 33-2, there are 263 integrated circuits, all of which are used to implement the design of the command control system. Also, the majority of these circuits are located in the signal conditioner devices to be controlled. This characteristic of the design is used to reduce wiring interconnections and to achieve a modular systems approach. The command demodulator and decoder detects and decodes the command signal to a binary serial PCM format. Each code word consists of 11 bits, of which 5 bits are channel-address, and 6 bits are command data. The output of the command demodulator and decoder consists of 30 addresses, as well as the command data and the clock rate. Command data are routed in serial format to all conditioning circuits with the clock rate. It is the function of the address lines to insert the command into these circuits in proper time sequence. This approach requires that all command data be decoded in the conditioning circuits. These circuits become complex, and maximum advantage is taken of microelectronics to achieve this complexity with reduced size and weight.

Figure 33-3 is a block diagram of the complete signal conditioner, including command circuits required for each of the 20 data channels. Two differential amplifiers are used to amplify the transducer signal to a 5-volt full-scale level for modulating the FM oscillators. The first amplifier is fixed gain; the second may be switched to four gain settings to accommodate 5-, 10-, 25-, and 50-millivolt full-scale inputs. The fixed offset voltage is inserted at the input of the second amplifier. A storage register accepts the sequential data command words for all data channels. The six-bit parallel output of this register is connected to storage registers in each conditioner circuit. Also connected to these registers are address lines. These lines shift command data into each of the five conditioner registers at the proper time in the command sequence so that each signal conditioner accepts a single and unique command. A four-bit, digital-to-analog converter generates 16 offset voltages. The remaining two bits control two miniature relays to obtain four gain settings.

This detailed description is given to emphasize the complexity of the control conditioner circuits and the requirements for miniaturization to meet system weight and volume guidelines. The advantage of this design is that only seven wires are required from the command decoder and demodulator to command the 100 functions in the five circuits. In addition, the complexity of the command system is more a function of the number of command functions used than of the total capacity of the command system.

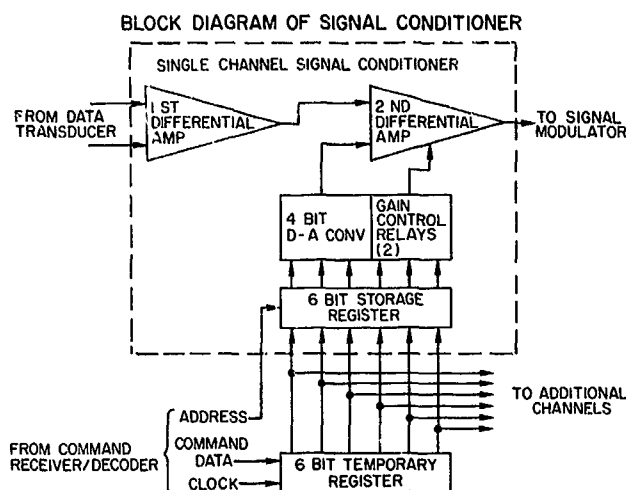


Figure 33-3—Block diagram of signal conditioner.

Figure 33-4 is a photograph of the signal conditioner circuits. Six Fairchild DTL, integrated-circuit flip-flops are used to enter command data into the circuit. The digital-to-analog converter is implemented with the screened circuit technology with the exception that discrete resistors are used to obtain a low-temperature coefficient. The miniature relays for gain switching are not shown. The two differential amplifiers are also screened circuits.

#### CIRCUIT DEVELOPMENT

The primary circuits developed at the Langley Research Center were the differential amplifier and the FM oscillator. It was determined that available amplifiers and oscillators could satisfy most of the requirements with the exception of long term stability. An overall amplitude accuracy of  $\pm 2.5$  percent is required. This accuracy must be maintained without calibration during a 24-hour period in a thermal environment of 25 to 65° C.

Table 33-3 is a summary of the salient electrical performance characteristics of the amplifiers evaluated. The impedance, gain, bandwidth, and other characteristics of these amplifiers

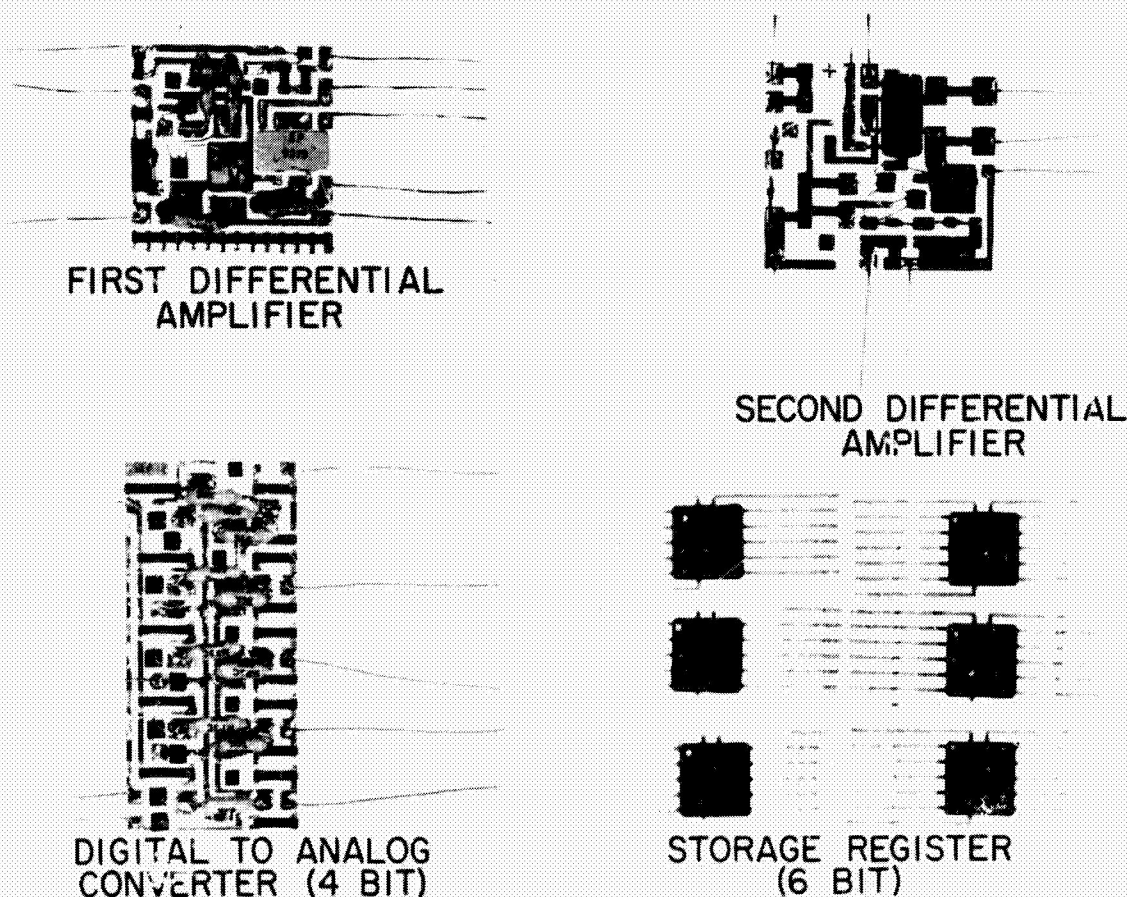


Figure 33-4—Typical signal conditioner construction.

Table 33-3

## Summary of differential Amplifier Performance Characteristics

Characteristic	Available integrated circuit amplifiers				LRC amplifier
	A	B	C	D	
Voltage gain	4 500	20 000	1 000	2 600	2 300
Differential input impedance	200k $\Omega$	10m $\Omega$	10k $\Omega$	10k $\Omega$	57k $\Omega$
Differential input offset voltage drift	10 $\mu$ V/ $^{\circ}$ C	75 $\mu$ V/ $^{\circ}$ C	24 $\mu$ V/ $^{\circ}$ C	8.8 $\mu$ V/ $^{\circ}$ C	0.5 $\mu$ V/ $^{\circ}$ C
Bandwidth	50 kc	1 mc	50 kc	80 kc	50 kc
Total power dissipation	220 mw	200 mw	72 mw	70 mw	125 mw

could be obtained by any of the four commercial models evaluated. The important parameter that limits application of these amplifiers is the input zero-offset drift voltage as a function of temperature. The best performance of one of these units is 8.8 microvolts per degree Centigrade. Over a 40° C range this performance produces a 352-microvolt total drift. For the 5-millivolt full-scale input condition, this drift represents an error of  $\pm 3.5$  percent. The screened circuit amplifier, as noted, has a drift of 0.5 microvolt per degree Centigrade, with a resulting total drift of 20-microvolts over the same thermal range. For the 5-millivolt input condition, this drift represents an error of  $\pm 0.2$  percent of full scale. The relative thermal performance of these amplifiers is plotted in Figure 33-5.

A substantial increase in performance of the screened circuit amplifier is obtainable if electrical and thermal compensation are incorporated in the design. There is a limit on how closely a pair of transistors can be matched in gain, leakage, and emitter-to-base voltage and all of these parameters affect thermal stability. However, it is possible to overcome this limitation by matching collector currents over the thermal range in the circuit external to the transistors. In the screened circuit amplifier this matching is accomplished by employing matched, discrete resistors having low thermal coefficients, in conjunction with a discrete sensistor. In effect, the resistors are used to obtain a precise match; the sensistor maintains this match by compensating for transistor parameter variations over the thermal range. Figure 33-6 is a photograph of the input differential amplifier as fabricated in screened circuits.

Table 33-4 is a comparison of the characteristics desired in the FM oscillator and characteristics found in available units. It can be seen that the primary area where the available units do not meet the requirements is that of stability. All of the available units utilize multivibrator (R-C) circuits which provide excellent linearity. These circuits are well adapted to microminiature construction, but are relatively difficult to stabilize with respect to both power supply and temperature variation. Utilizing a high "Q" R-C oscillator with a voltage-variable capacitor

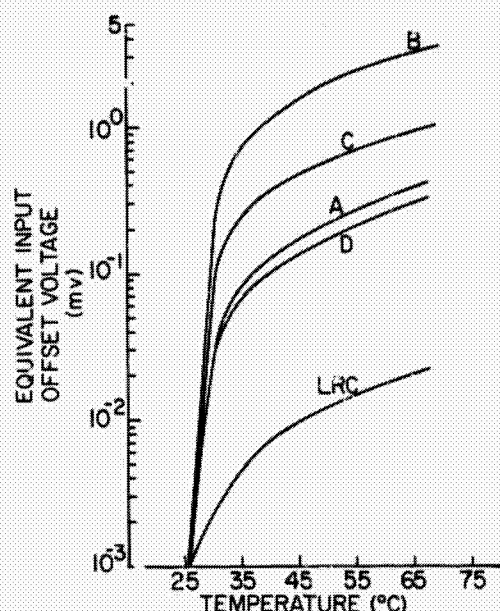


Figure 33-5—Comparison of zero drift versus temperature characteristics for differential amplifiers.

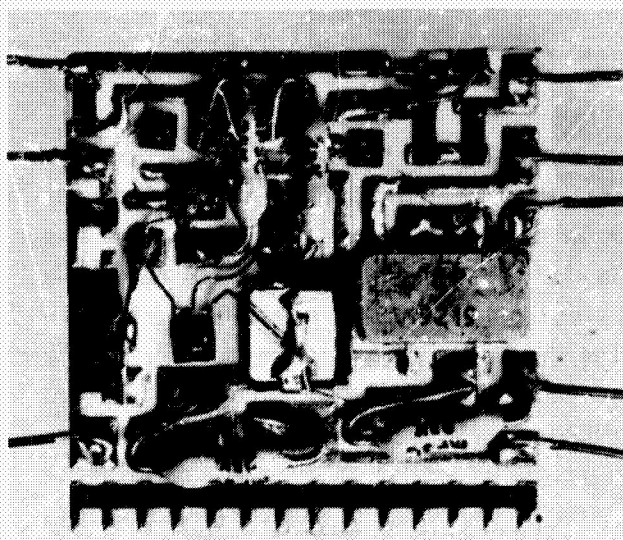


Figure 33-6—Detail construction of first differential amplifier.

results in a unit which is inherently more stable but which does not have the linearity of a multi-vibrator. A prototype of such an oscillator developed at the Langley Research Center provides a power supply stability of better than  $\pm 10$  cps, a temperature stability of better than  $\pm 20$  cps, and a linearity of better than 0.7 percent. The  $\pm 20$ -cps temperature stability is the equivalent of a full-scale zero drift of  $\pm 2$  percent. This unit, however, was not packaged within the required volume. Work is presently being conducted at Langley to miniaturize this oscillator. Figure 33-7 shows a comparison between the commercial oscillators and the package which will be used for the L-C oscillator. The L-C oscillator will consist of a discrete resonator with all additional circuitry fabricated by a screened circuit process.

Table 33-4

Comparison of Available and Required F.M. Oscillator Characteristics

Characteristic	Required	Available (IRIG constant BW)
Operating frequency	95 to 190 kc	up to 190 kc
Frequency deviation	$\pm 1$ kc	$\pm 2$ kc
Linearity	$\pm 1\%$	$\pm 0.25\%$
Frequency stability		
$\pm 10\%$ power supply	$\pm 20$ cps	$\pm 80$ cps
$\pm 20^\circ\text{C}$ temperature	$\pm 35$ cps	$\pm 120$ cps
Output power	5 mw	0.1 mw
Size	6 cm <sup>3</sup>	5 cm <sup>3</sup>



## CONCLUDING REMARKS

The results of the work performed have established that microelectronics can be successfully applied to help solve the difficult instrumentation and control problems encountered in ground-research test programs. It is noted that analog-data requirements cannot be satisfied completely with microelectronics, as is true in space vehicle systems. However, the use of microelectronics in performing digital functions is significantly advantageous. Here an appreciable saving in weight and volume is realized in the design of complex digital command and control systems. It is noteworthy that the design and construction of the digital portions of the systems were accomplished with little difficulty. To obtain the required analog-system performance, considerable development effort was necessary.

A five-channel data and control system is currently being constructed. This system will be evaluated in the Langley transonic dynamic wind tunnel. The earliest anticipated application of the complete system will be for the research tests to be performed on a model during the calendar year 1957.

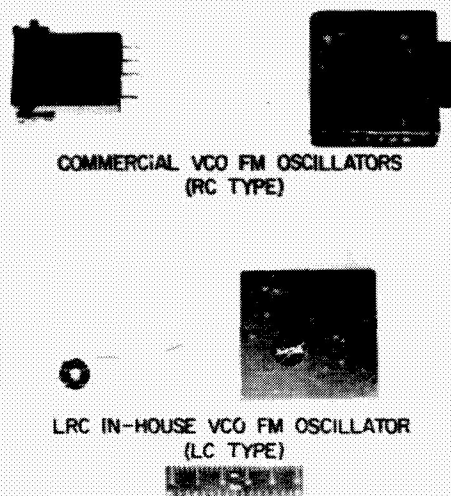


Figure 33-7—Typical oscillator types.



N67-31596

34. MAGNETIC OR INTEGRATED CIRCUITS: A COMPARATIVE ANALYSIS OF THEIR  
APPLICATION TO A MICROMETEOROID SENSOR SCANNING PROGRAM

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A proposed experiment to obtain statistical data on micrometeoroid penetration rates in spacecraft structural materials containing 1 to 50 mils of aluminum requires the deployment of 6000-7000 square feet of sensor material during a 1- to 2-year period. The physical dimensions imposed by the thin sensor materials dictate the use of 1000 micrometeoroid pressure-cell sensors for this purpose. Instrumenting and scanning such numbers of sensors on a spacecraft with an 85-foot span poses formidable problems. For example, the amount of cable and electronics required to do so with conventional circuitry makes the task very difficult and affects reliability and power consumption. To alleviate this situation, a method of segmented data scanning was developed that permits direct entry of sensor data into a matrix of electronic devices which scan all sensor switches. The method has been implemented through the use of both integrated and magnetic circuit techniques. This paper compares the two techniques with regard to operation, power requirements, size, and potential reliability. Some limitations of the integrated circuits employed are discussed, and areas for further development are suggested.

## INTRODUCTION

The Advanced Micrometeoroid Program currently under study at the Langley Research Center involves a dual-mission spacecraft. The two missions are an interplanetary flight (out to about 2.5 astronomical units) and a near-earth orbital mission (300 to 600 miles), with as much commonality in spacecraft hardware between the two missions as possible. A proposed version of the spacecraft (Figure 34-1) has a weight of 20,000 pounds, a wing span of 85 feet, and 1000 micrometeoroid pressure-cell sensors totaling 6000 to 7000 square feet of exposed area. Sensors with several thicknesses of test material are used on the spacecraft to establish a micrometeoroid flux rate for different thicknesses. The sensors consist of a pressurized volume, a bellows diaphragm, and a microswitch. When the sensor is punctured by a micrometeoroid, pressure is lost, the diaphragm is displaced, and the microswitch is actuated. This switch action takes place only once; it is permanent and irreversible.

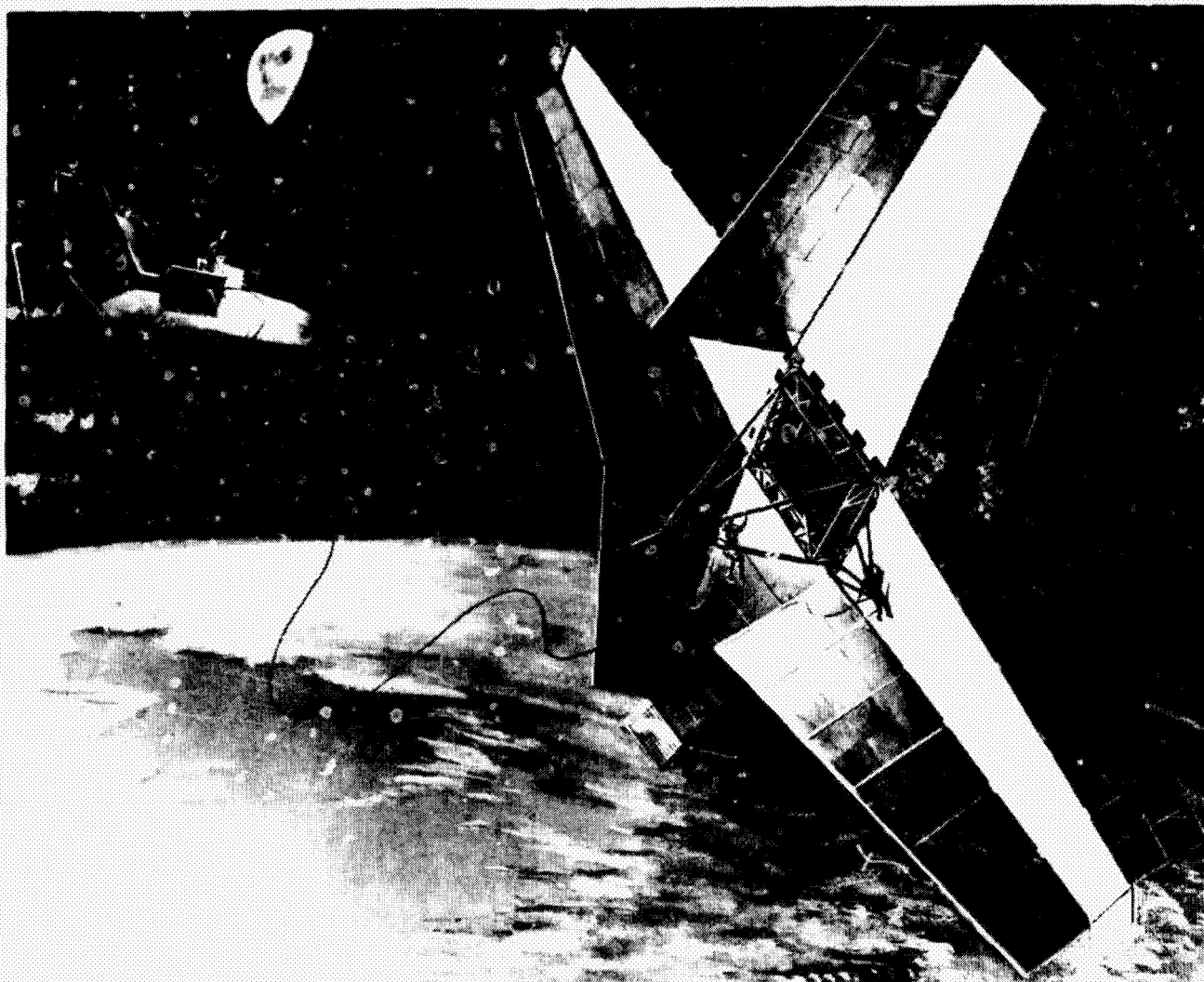


Figure 34-1—Advanced meteoroid spacecraft.

The lifetime of the interplanetary mission experiment is approximately 200 to 250 days, and that of the near-earth mission approximately 2 years. In order to obtain a 2-year lifetime for the experiment, emphasis must be placed on the use of highly reliable devices and techniques in the signal conditioning circuit. For both missions, there may be as few as zero to 20 punctures in the thick sensor material, but as many as several hundred in the thinner materials. Since considerable significance can be placed on one or two punctures, every attempt must be made to assure that all data received during the experiment are valid and not the result of spurious noise or data-system failures.

When the number of solder joints and connectors required to instrument 1000 sensor switches are considered, it becomes apparent that there is a high probability of errors in experimental data due to wiring failures (e.g., cold solder joints). A technique was developed to scan both the normally open (NO) and normally closed (NC) contacts of each sensor switch to increase the confidence in the data received from the spacecraft. This technique is shown graphically in Figure 34-2. The sensor

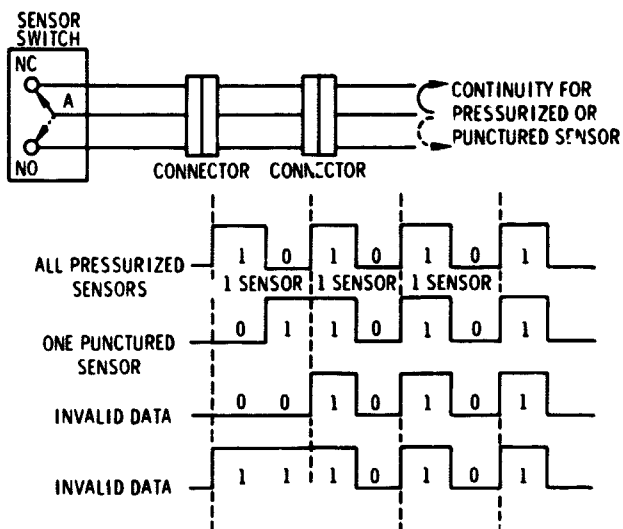


Figure 34-2—Technique for wiring continuity verification.

in a pressurized state has continuity through the NC contacts of the switch, and a logic "1" is generated. The NO contacts have no continuity, and a logic "0" is generated. If the sensor is punctured, scanning the NC contact causes a 0 to be generated, and the NO contacts cause a 1 to be generated. In both the pressurized and unpressurized states, continuity through the sensor and all of its wiring is required to code the state of the switch. The other combinations of data, "11" and "00", occur as a result of wiring or switch failures. In order to falsely generate the valid bit combinations, two failures must occur. This technique adds additional complexity to the data conditioner, although the increased confidence in experimental data justifies the expense.

Although various techniques for scanning a large number of sensors have been explored, it has been determined that a matrix technique is the best approach for this application. The matrix has an advantage, in that each sensor switch and the state of the switch (ON or OFF) can be uniquely identified. In addition, the matrix can be implemented in such a manner that most failure modes can be determined by analyzing the data output. Finally, the matrix can be implemented by means of digital circuit technology.

A single, large matrix for scanning all sensor switches offers the least number of parts and the lowest power consumption than any other scanning technique. However, a single component failure may result in the loss of either all or a large percentage of the experimental data. The use of several smaller matrices increases the probability of receiving a portion of the sensor data. Considering the configuration of the spacecraft, it was decided to provide a matrix for each of the four wings of the spacecraft. Thus, each matrix was required to scan 250 sensors. If the various sensor thicknesses are assumed to be equally distributed among the matrices, a catastrophic failure of one matrix results in a loss of 25 percent of the exposed micrometeoroid sensor area.

Two types of circuits, magnetic and semiconductor, each having its own particular advantages and limitations, may be used for scanning the sensor switches. To further investigate the merits of each type circuit for this particular application, it was decided to breadboard both types of matrix circuits and then compare them. Because of the requirement for high reliability and relatively small size, integrated circuit diode transistor logic was used in building the semiconductor matrix. As an expediency, only half-size matrices for 125 sensors were built since any factors uncovered in the smaller matrices could be scaled to the full-size matrices. It was not intended in the design of the matrices that an optimized, flight-quality package would be built.

## DESCRIPTION OF INTEGRATED CIRCUIT MATRIX

Figure 34-3 is a simplified block diagram of the integrated circuit matrix. The 16 Y-axis address lines are sequentially enabled at the clock input rate. At the completion of this cycle, the X-axis address line is advanced to select the next line, and the Y-axis cycle is repeated. In this standard manner, the complete matrix is scanned. A gating arrangement is included in the X-axis address lines to provide a serial output as the Y- and X-axis address lines are scanned to check for continuity through the pressure switches.

Figure 34-4 shows the connections between the pressure switches and the matrix. These switches are located in the wings of the spacecraft, remote from the data conditioner matrix. For 125 sensor switches it is necessary to route 266 wires to the data conditioner. As shown, two wires are required for each switch to monitor both the closed and open contacts on the Y-axis lines. The arms for the 16 switches on a common X-axis line are connected together in the spacecraft wings, with a single wire routed to the data conditioner. The diodes shown are provided to prevent ambiguous paths in the matrix.

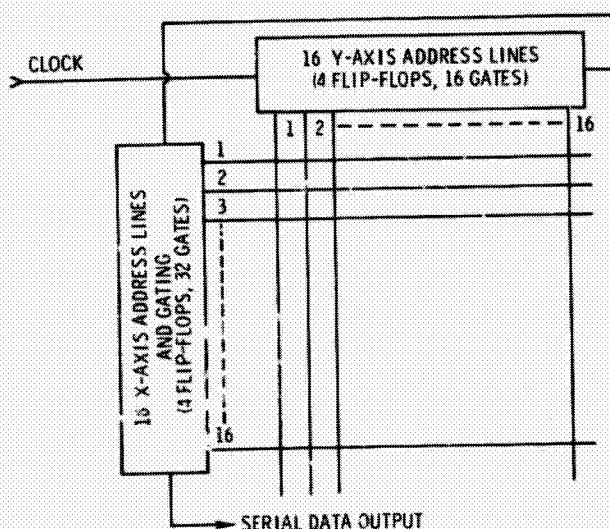


Figure 34-3—Integrated circuit matrix.

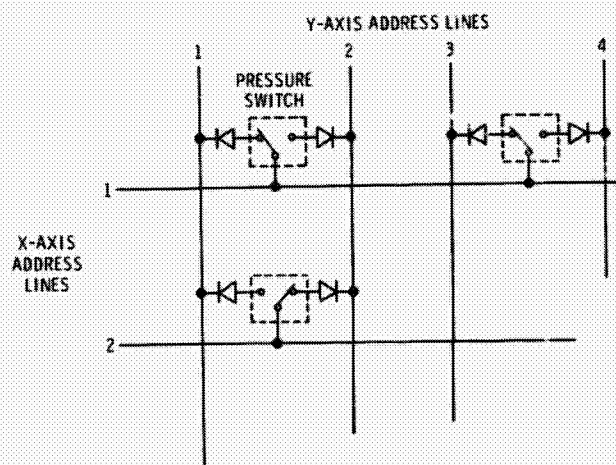


Figure 34-4—Pressure switch connection to matrix.

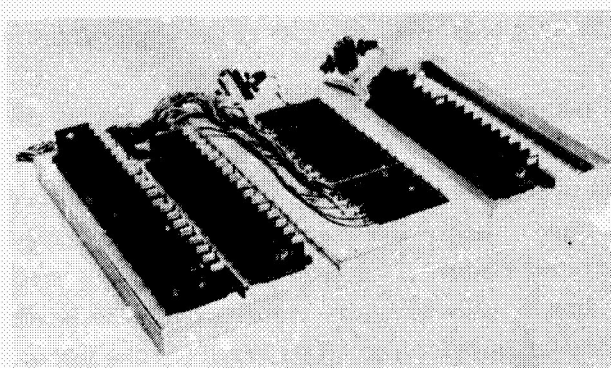


Figure 34-5—Integrated circuit matrix.

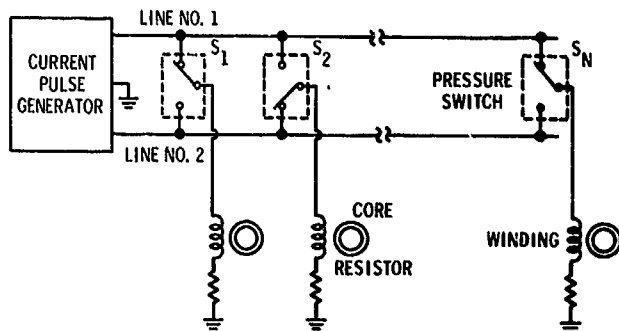


Figure 34-6—Magnetic core loading technique.

Figure 34-5 is a photograph of the breadboarded integrated circuit matrix, built by use of diode transistor logic. The flat packs are mounted in carrier boards which are then mounted on a metal frame. A total of 51 flat packs is used in the breadboarded system, although 30 flat packs could have been used if more suitable logic units, such as multiple gates per flat pack, had been available at the time of construction. Reliability figures to be discussed subsequently are based on the use of

optimum flat packs. The listings for power consumption are not appreciably affected by either approach since basically the same number of logic elements is involved.

## DESCRIPTION OF MAGNETIC MATRIX

Magnetic circuits for a scanning matrix offer potential savings in power requirements and reliability, provided that a simple method for entering the sensor pressure switch data into the matrix is available. Figure 34-6 is a diagram of the technique that is used for placing sensor data into a core plane for subsequent readout. A single wire from the arm of each sensor switch is routed back into the matrix, through a winding on a core, to a resistor, and to ground. The current pulse generator simultaneously stores sensor data in all cores by placing a positive voltage on line 1 and a negative voltage on line 2. All cores associated with a pressurized sensor are then set to a 1, and all cores associated with a punctured sensor are reset to 0. The core plane is next read out to determine the states of the cores. The current pulse generator then places a negative voltage on line 1 and a positive voltage on line 2. The cores associated with a punctured sensor are set, and those associated with a pressurized sensor are reset. The core plane is again read out. The two readouts, which are complements, are compared bit-by-bit to determine the states of the pressure switches, thus verifying continuity through the sensor wiring.

For a half-size matrix, only 127 wires are required in wiring the sensor switches. A full-size matrix of 250 sensors requires 252 wires (a single wire from each switch arm plus a wire each for line 1 and line 2) to connect the sensor switches completely.

Once the cores are loaded with sensor data, any number of available standard techniques for reading out magnetic memories can be implemented to determine the states of the cores. The technique selected consists of magnetic circuits which use core-transistor ring counters to address each core. Full currents are used in addressing the cores. The sense amplifier utilizes discrete semiconductor circuitry and is the only circuit requiring continuous power.

The magnetic matrix (Figure 34-7) is constructed with discrete components. All semiconductors are silicon, and all cores (except two of them) are 22-maxwell, square loop, tapewound



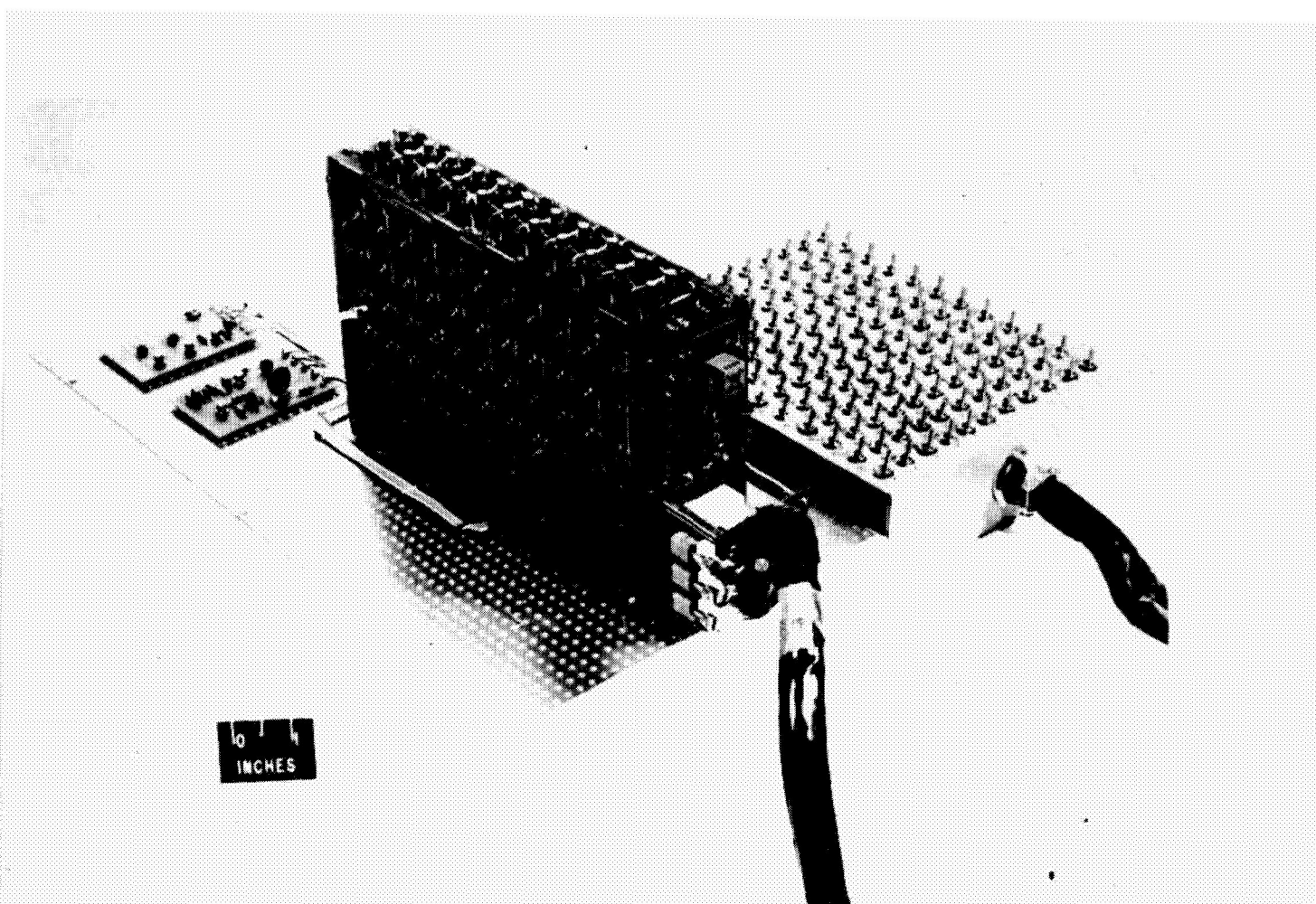


Figure 34-7—Magnetic circuit matrix.

cores. The system is fabricated on printed circuit boards to afford some protection to the large number of small wires on the cores during testing.

## COMPARISON OF MATRICES

### Tests Performed

To allow a more direct comparison of the two circuit techniques, identical tests were performed on each matrix breadboard. These tests included temperature cycling, power-supply variations, power consumption, system noise susceptibility, and impedance variations on the wiring to the sensor switches. Temperature extremes were selected at  $-20^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ ; power supply variations were  $\pm 20$  percent of nominal. Supply voltages were  $+4.5\text{ vdc}$  for the integrated circuit matrix and  $+28\text{ vdc}$  and  $+4.5\text{ vdc}$  for the magnetic matrix. Operating speeds for the matrices were 10 bits per second (a requirement for the interplanetary flight) and 1000 bits per second (a requirement for the near-earth mission). These tests were considered the most representative for revealing the over-all system parameters that would permit evaluating the two circuit techniques.

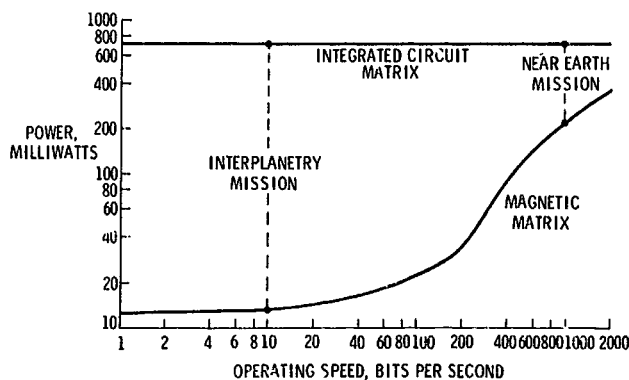


Figure 34-8—Power consumption of matrices.

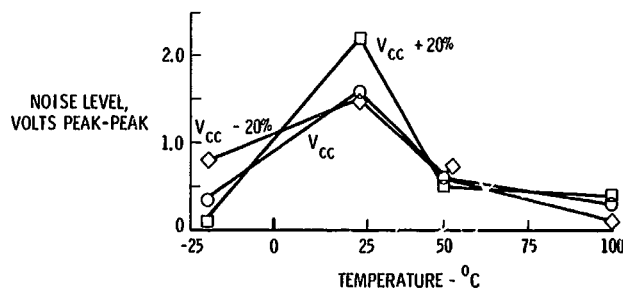


Figure 34-9—Noise susceptibility, integrated circuit matrix.

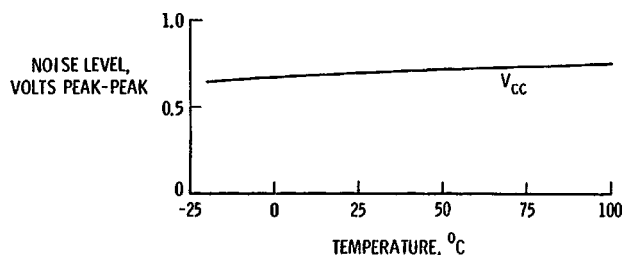


Figure 34-10—Noise susceptibility, magnetic matrix.

### Noise Susceptibility

The test for noise susceptibility included white noise and synchronous and asynchronous spikes inductively induced onto the supply voltage and ground leads. The system output of the matrices was used as the evaluation point for noise susceptibility. The noise susceptibility of the integrated circuit matrix (Figure 34-9) is controlled by the flip-flops. The shape of the curve is attributed to two characteristics of the flip-flops, noise susceptibility and trigger sensitivity. These characteristics are such that the worst noise susceptibility is at the temperature extremes, and the best noise susceptibility occurs at room temperature. The limiting factor for the noise susceptibility of the magnetic matrix (Figure 34-10) is the sense amplifier. No significant variations in noise susceptibility due to power supply variations were measured. Although noise susceptibility for the

### Power Consumption

The main difference between the two matrices is power consumption, as shown in Figure 34-8. Power requirements for the integrated circuit matrix do not vary with speed. However, the power requirement for the magnetic matrix varies significantly with speed. When the system is scaled to a full-size matrix (250 sensors), power consumption increases to 1.0 watt for the integrated circuit matrix but does not change significantly for the magnetic matrix.

For the near-earth mission where operating speeds of 1000 bits per second are desirable, four full-size matrices accommodating 1000 sensors would require 4.0 watts for the integrated circuit approach and 0.8 watt for the magnetic matrix. For the interplanetary mission, operating speed is reduced to 10 bits per second. The integrated circuit matrices still require 4.0 watts, but the magnetic matrices now consume 55 milliwatts. This is a reduction in power requirements by a factor of approximately 70.

For both matrix techniques, variations in power consumption as a result of supply voltage and temperature variations were equivalent, so that neither technique showed a significant advantage over the other.

magnetic circuit at temperature extremes is better than that for the integrated circuit matrix, higher levels of noise susceptibility are desired for both systems. Techniques have been investigated to improve the noise susceptibility of both systems. Results of this work indicate that a redesign of the sense amplifier may significantly improve the noise susceptibility. Unless it is possible to develop integrated circuit flip-flops with better noise susceptibility, it will be necessary to change system techniques to improve the noise susceptibility of the integrated circuit matrix. These techniques have the disadvantage of addition system complexity and will result in increased power requirements and reduced reliability.

### Sensor Wiring Impedances

The tests for varying sensor impedances are intended to determine the amount of resistance and distributed capacitance that can be tolerated in the wiring loop from the signal-conditioning circuit to the sensor switch without degrading system performance. These impedances are simulated by inserting lumped resistance in series with wires to the sensor switches. Distributed capacitances are simulated by placing lumped capacitors between sensor wiring and ground. Figure 34-11 is a plot of resistance for the integrated circuit matrix. Under the worst conditions of voltage and temperature, this resistance can be as high as 400 ohms. When the upper resistance limit is approached, the system becomes more susceptible to noise. Lumped capacitance up to 1000 picofarads on the sensor lines does not affect the operation of the system. Figure 34-12 is a plot of the varying sensor resistance for the magnetic matrix. The limiting requirement for the matrix is the current necessary to set each of the cores in the core planes. This current can be adjusted by the amount of overdesign in the current pulse generator. The worst condition at low temperature and voltage is lower than desired and will be increased above 100 ohms by providing more current capacity from the current pulse generator.

### Matrix Implementation

The implementation of the matrix technique on a spacecraft presents another comparison between the two matrices. A package of 70 cubic inches is required for each magnetic matrix, whereas approximately 80 cubic inches are required for the integrated circuit matrix. Although the

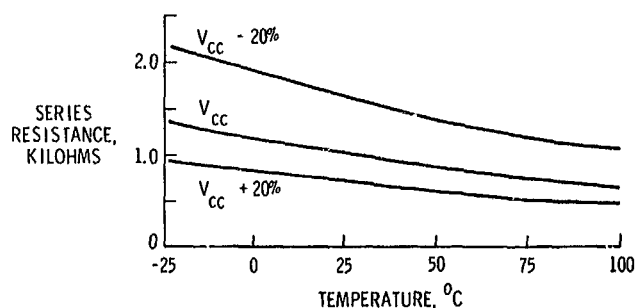


Figure 34-11—Resistance in sensor wiring, integrated circuit matrix.

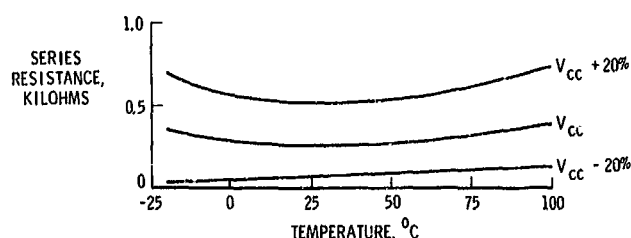


Figure 34-12—Resistance in sensor wiring, magnetic matrix.



integrated circuit packages require 5 percent of the total volume, the requirement for twice as many wires and diodes results in a larger volume. The 516 wires in a full-size integrated circuit matrix as compared to 252 wires in a full-size magnetic matrix result in a difference in weight for the wiring of the two matrices of 200 pounds on the spacecraft. The use of the integrated circuit package for this application results in a system weight and volume penalty, as compared with use of the magnetic circuit techniques, a fact which was not obvious before the study was made.

It is possible to implement the integrated circuit matrix in order to reduce the complexity of the sensor wiring to that for the magnetic matrix. A full-size integrated circuit matrix requires 45 flat packs in optimized packaging configuration. To implement the matrix where the design consideration is one wire per sensor switch would require 123 integrated circuit packages. This would significantly increase power and reduce reliability.

#### Reliability

The reliability calculations are intended to be comparative in nature and were obtained by using identical ground rules for both matrices. The full-size integrated circuit matrix is a  $32 \times 16$  configuration. The full-size magnetic matrix is an  $11 \times 23$  core plane configuration. The results of the reliability calculations are presented in Table 34-1. Also shown are the reliability calculations with the sensor wiring included. A failure in the sensor wiring normally results in the loss of data for one sensor; such a failure is detectable and is not a total system failure.

TABLE 34-1

MATRIX AND SYSTEM RELIABILITY, TIME = 2 YEARS

#### PER SPACECRAFT WING

	MATRIX	SENSOR WIRING	MATRIX + WIRING
INTEGRATED CIRCUIT	0.923	0.905	0.835
MAGNETIC CIRCUIT	0.975	0.953	0.929

#### PER SPACECRAFT

	MATRIX	MATRIX + WIRING
INTEGRATED CIRCUIT	0.968	0.870
MAGNETIC CIRCUIT	0.996	0.973

The magnetic matrix has a 5 percent better reliability number than the integrated circuit matrix. When sensor wiring is considered, the magnetic matrix has a 10 percent better reliability number. On a spacecraft system basis, including sensor wiring, the magnetic matrix has a 10 percent better reliability number than the integrated circuit matrix. It is important to note that for both matrices, the reliability of the sensor wiring is less than that of the matrix itself, which justifies the need for scanning both sides of the sensor switch to verify continuity through the sensor wiring. Inherent in the design of both matrices are critical failure modes since both systems depend on a series type of operation for a complete scanning of the matrix. Neither matrix lends itself to internal or element redundancy (except for quad-diodes) for increased reliability, and any attempts at redundancy are best accomplished by using completely redundant matrices, redundant sensor wiring, and a double-pole double-throw switch at the sensor.

## CONCLUSIONS

For the particular mission studies, integrated circuits do not provide the best solution to system power, weight, and reliability requirements. The design and implementation of the integrated circuit matrix are such any advantages that might be gained through the use of integrated circuits are masked. The two major disadvantages of integrated circuits are high power consumption and a weight penalty due to the additional sensor wiring. Although the use of integrated circuits instead of custom designed discrete semiconductor component logic circuits offers considerable size reduction and increases in reliability, these advantages are at the expense of power consumption. This application study illustrates a definite requirement for low-speed, low-power logic. The development of more lumped logic circuits in a single package such as 16 and 32 line-drivers would substantially increase the over-all reliability of an integrated circuit matrix. Until more suitable integrated circuit logic becomes available, hybrid semiconductor and magnetic circuit techniques offer the best solutions to system design for this application.

N67-31597

### 35. POWER INTEGRATED CIRCUITS IN THE SATURN SYSTEM

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Until recently, there has been a general feeling that integrated circuits are not suited to high-voltage, high-power applications. If properly designed and mounted for heat removal, however, there is no real limitation to the power handling capabilities of integrated circuits. For several years Marshall Space Flight Center (MSFC) has had an active program in developing power circuits. This paper outlines the development of three individual circuits and the Saturn three-phase, 400-Hz static inverter.

#### INTRODUCTION

Integrated circuits and microelectronics have made it possible to design better electronic systems for ground and spaceborne equipment. This paper covers three individual circuits and the Saturn integrated static inverter, all developed under contracts at Marshall Space Flight Center. The integrated power amplifier and integrated oscillator amplifier described in this paper incorporate some of the techniques developed by Westinghouse. The integrated power bridge amplifier was the outcome of an excellent effort by Norden and Goodyear Aerospace in solving a very difficult problem. Integration of the static inverter involved complicated low-power circuits and high-power circuits. This work was accomplished by Texas Instruments.

#### INTEGRATED POWER AMPLIFIER

In the design of an integrated power amplifier, factors such as gain, voltage, switching speed, secondary breakdown, and thermal runaway must be considered. Reliability is a major factor for any design approach. Since many of these factors do not complement each other, some logical trade-offs must be accomplished to obtain maximum reliability. Secondary breakdown is the major limitation on the reliability of power transistors, but it can be minimized by utilizing a device with the lowest adequate frequency characteristics for the application. For example, an audio frequency transistor is more reliable than a VHF transistor in an audio circuit. Similar arguments can be advanced for other characteristics of the device.

The electrical schematic and package of the integrated power amplifier developed by Westinghouse for MSFC are illustrated in Figure 35-1. The single, or simultaneous, diffusion procedure was selected in fabricating this system because of the excellent secondary breakdown characteristics so obtained. The base region of the single diffused transistor is essentially virgin silicon crystal. The grown ingot is generally considered superior to diffused or epitaxial material. This is especially true for large areas, where local defects leading to hotspot failure are to be avoided.

The voltage design of the amplifier was based on a previous configuration known to provide the required frequency and punchthrough between 150 and 200 volts. The circuits fabricated by Westinghouse exhibited collector sustaining voltages between 125 and 150 volts. The units were designed for  $h_{fe}$  at 10 amperes to be 20 at 25°C, and not to exceed 15 at 150°C. The actual circuits exhibited  $h_{fe}$  values between 20 and 50 at 25°C. Although the current gains greatly in excess of the design values could have created instability, the circuits performed well at approximately two times the rated design goal of 10 amperes. Since the circuits were designed to operate in the common-emitter configuration with large collector currents, better balance could be achieved by encapsulating the discrete transistors in the same package. This approach permitted matching of Betas, saturation resistances, and input resistances before encapsulating.

Each complete device was built on a piece of silicon 63.5 by 114.3 mm. The power transistor is interdigitated and occupies 80 percent of the area. The remaining 20 percent of the area is devoted to the resistor and diode. The base electrode completely circles the emitter, resistor, and diode regions to avoid surface channel formation. The base fingers are slightly tapered to reduce the injection near the root of the emitter fingers. This reduces the tendency to generate hotspots. The diode, located beneath the metalized square area at the resistor end, offers the additional feature of a large pad for lead attachment. It is capable of handling about three-fourths of ampere, giving adequate protection to the transistor. The shunt resistor is integrated into the transistor unit for each half of the amplifier.

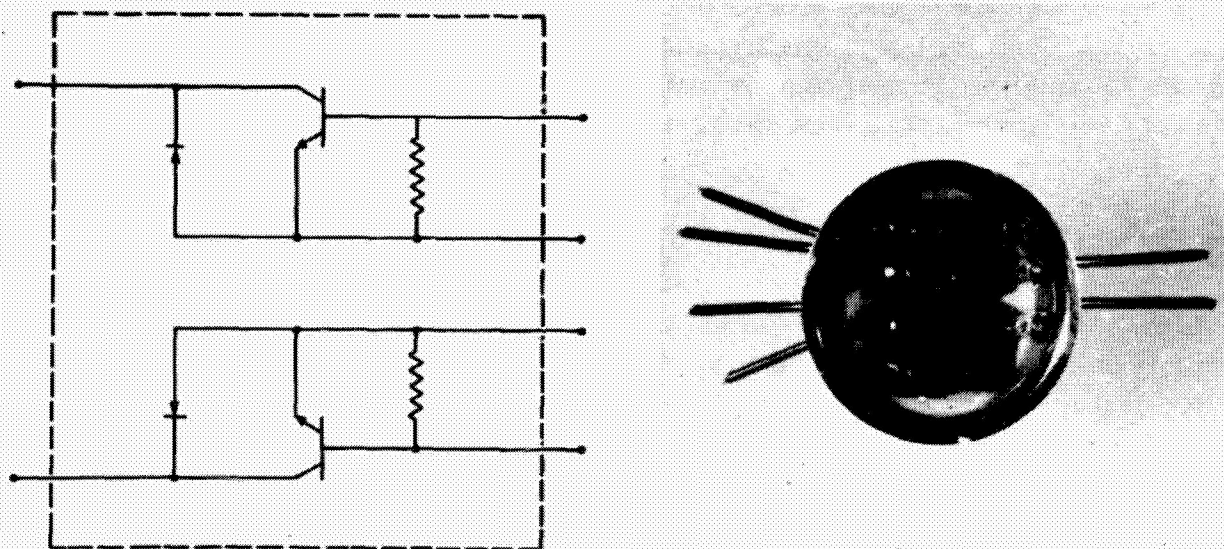


Figure 35-1—Integrated power amplifier.

The basic design, although apparently simple, is actually quite sophisticated, permitting some latitude for modifications to meet specific circuit needs. Different masks were developed to provide variations in resistance, tapping of emitter fingers, and diode capacitance through additional etching. The circuits delivered under this contract met or exceed the specified objectives.

### INTEGRATED OSCILLATOR AMPLIFIER

In practically every electronics system the need arises to convert or change the voltage level of the primary signal source. This has created a recognized need for integrated power oscillator circuitry. NASA's Astrionics Laboratory has taken the initiative in fulfilling this need by awarding a contract for development of a 20-watt and a 70-watt, 50 kHz amplifier. The circuit configuration and package common to both units are shown in Figure 35-2.

As more sophisticated circuits appear, more complex methods evolve in obtaining solutions. The design approach for this oscillator amplifier is drastically different from the single diffusion approach used in the power amplifier, described previously. In the oscillator amplifier design, both mesa and planar epitaxial approaches have been conducted in parallel. To date, the mesa approach has yielded the best results.

The semiconductors (dashed line area in Figure 35-2(b)) are fabricated on the single chip shown in Figure 35-2(a). The two epitaxial diffused transistors are isolated by a moat. The resistors are on a moat between the two transistors to provide additional isolation between the transistors and to aid in stopping the channel formation for the junction of the collector diodes.

The semiconductor chip is fabricated on the epitaxial layer using double diffused profile. Two epitaxial layers of n-type material with different resistivity are grown consecutively on a

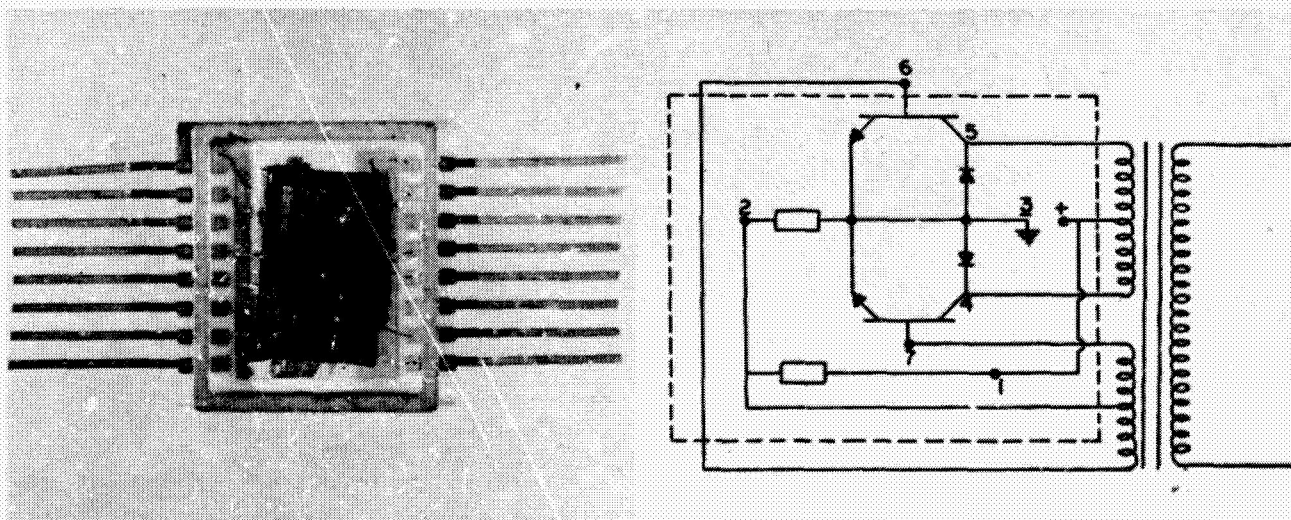


Figure 35-2—Integrated oscillator amplifier.



p-type silicon substrate. To make collector contact, n+ wall channel is also diffused at a different region of the epitaxial side in such a way that the n+ channel touches the epitaxially grown n-layer.

The base and emitter of the transistors and the resistor strips are diffused with proper maskings into the epitaxial layers within the walls; the contacts are metalized. The adjacent transistors are isolated by mesa etching.

The six diodes are also fabricated on the single chip. The basic structure is built upon the high resistivity n-type base. The diodes are formed by a combination of controlled epitaxial and selective diffusion techniques. Current crowding is avoided by the long, narrow geometry of each individual device. Electrical isolation is achieved by moat etching and a beryllia disc between the chip and the stud.

This circuit is not complete to date, but results thus far look very favorable.

#### INTEGRATED POWER BRIDGE AMPLIFIER

One of the most outstanding integrated power circuits is the power bridge amplifier developed by Astrionics Laboratory, Gyro Stabilizer Branch (Figure 35-3). For years engineers have looked for new ways to improve pulse duration modulated amplifiers. The Gyro Branch spent approximately 2 years breadboarding various pulse duration modulation circuits. After combining the most desirable features, a serious effort was made to reduce the circuit to the best integrable form using discrete components. A joint effort by Norden and Goodyear Aerospace produced probably the most outstanding integrated power circuit at that time. Basically, the circuit utilizes

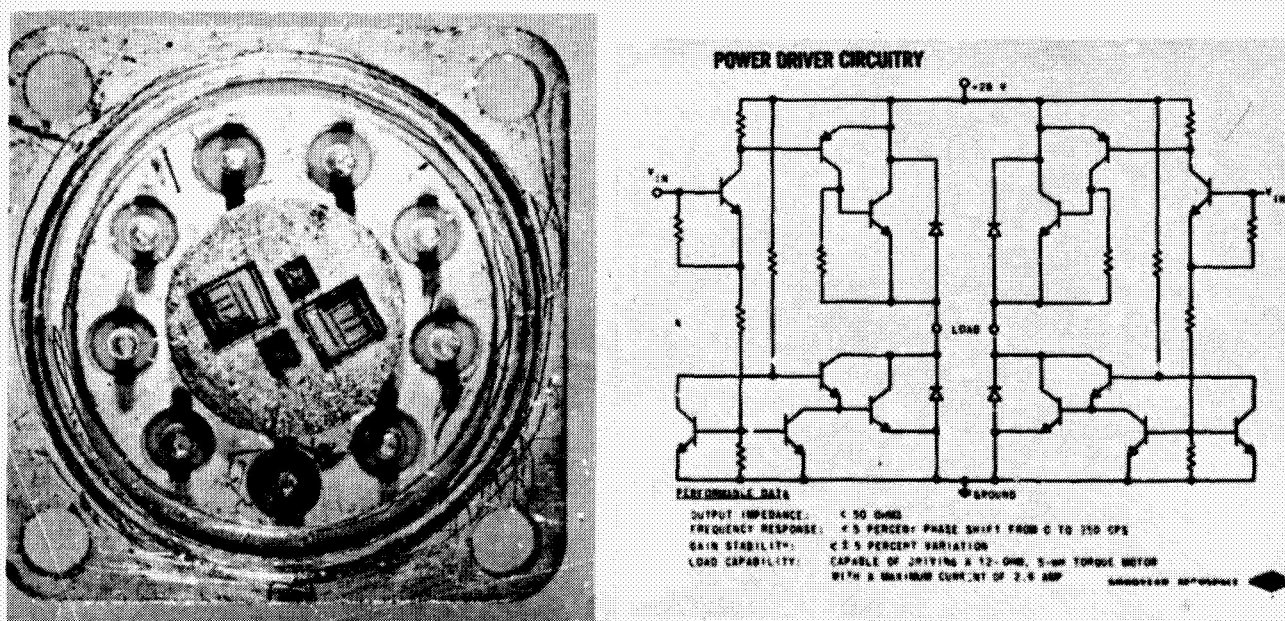


Figure 35-3—Integrated bridge amplifier.

a sawtooth wave superimposed on a dc level. The halves of the amplifier are matched as closely as practical. Depending on the polarity of the small signal transistor, which is sensitive to extremely low levels, the torquer is driven in the desired direction until full pulse width is reached, if necessary for correction.

The unit consists of 10 low power transistors, 4 power transistors, 4 power diodes, and 12 resistors. These components are on four silicon chips which are mounted in a single power transistor header. Since it requires large amounts of power (approximately 70 watts) to drive the torquer, large heat sinks were needed in the Class B operating circuits. At the time of development this was perhaps the most complex integrated power circuit developed. Complete evaluation has not been accomplished to date. However, results have exceeded expectations in the closed loop performance on a single axis simulator.

Some of the expected advantages of this unit are:

1. Extreme reliability potential
2. Good efficiency (approximately 90-95 percent)
3. Size reduction (approximately 50 percent)
4. A substantial cost reduction
5. Many other applications, such as dc regulators, heater power controls, inverters, etc.

#### SATURN INTEGRATED STATIC INVERTER

The Saturn static inverter represents a new approach utilizing digital techniques and unique transformer connections. This is a completed inverter flown on all Saturn I flights 3 through 10. All logic was accomplished in this inverter.

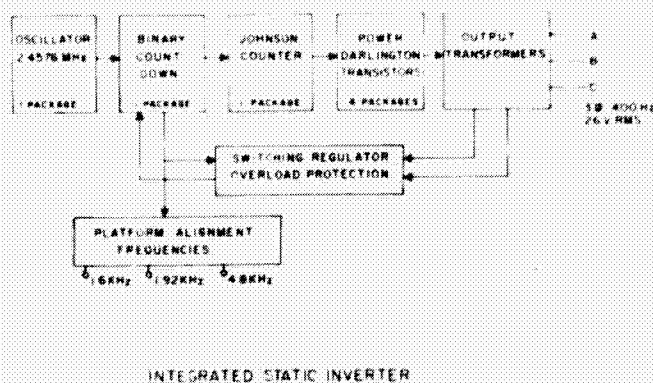
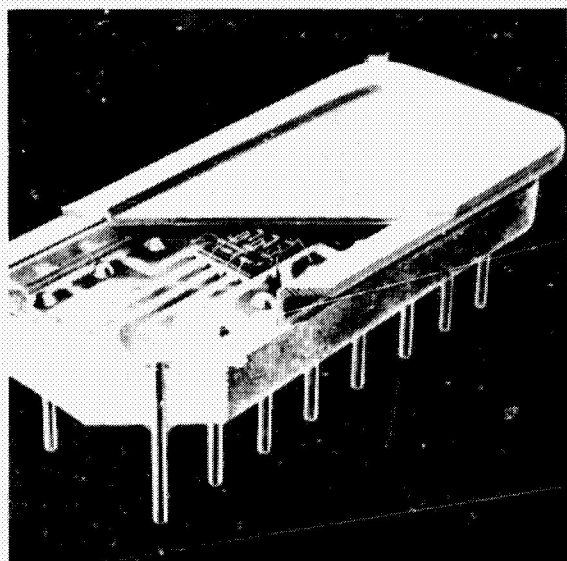


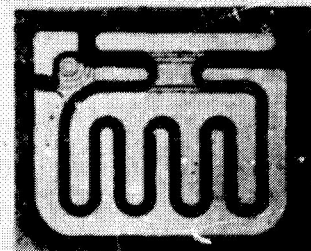
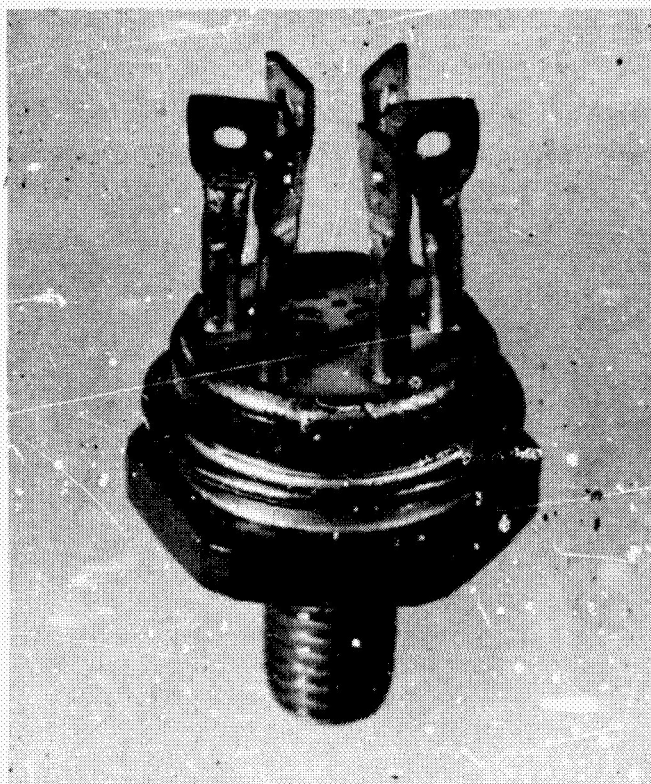
Figure 35-4—Integrated static inverter.



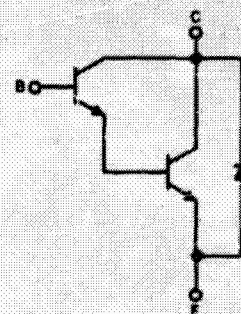
The Saturn 200 flights used a static inverter with all low-level logic accomplished by the series-51 integrated circuits. The system has 34 series-51 circuits that have functioned well from  $-35$  to  $+125^{\circ}\text{C}$ . The logic was followed by preamplifier and power stages with discrete components.

Figure 35-4 shows the high degree of integration achieved in this program. The design goal of a single chip for each ripple counter (divide by 12, divide by 10, count down  $2^8$ , and Johnson counter) was achieved. Also, the dual-chip, single-package, dual-npn Darlington transistors (Figure 35-5) were achieved.

The 2.4576-Mhz temperature compensated crystal oscillator is supplied by the Bendix Corporation. The oscillator is packaged in approximately 16 cubic centimeters. The  $2^8$  ripple counter, divide-by-10 counter, and divide-by-12 counter are all packaged individually in the standard 14-pin welded TO-84 flat pack. The npn transistor, pnp transistor, and npn Darlington all utilize the planar-epitaxial structure. This structure is formed by growing a high-resistivity epitaxial layer of silicon on a polished slice of low-resistivity silicon. The base and emitter are subsequently formed by diffusion into the epitaxial layer. This technique allows the width of the high-resistivity collector region, which needs to be only thick enough to give the desired collector-base avalanche voltage, to be optimized. The planar-epitaxial process results in reduced  $V_{ce(sat)}$  and switching times. In addition, the pnp process includes guard ring and field relief electrode techniques for improved stability on the high resistivity p-type surface. A 2.2 mm-square is used for the pnp



(a) METALLIZED WAFER



(b) DARLINGTON SCHEMATIC

Figure 35-5—Darlington transistor.



while the higher current npn wafer is 5 mm square. This integrated static inverter has been breadboarded and meets all design criteria objectives.

## CONCLUSIONS

The advantages of integrated power systems can be stated, but not necessarily in their order of importance, as follows:

1. The overall size of the system is reduced.
2. The overall weight of the system is reduced.
3. The efficiency of the system may be increased.
4. The reliability of the system can be greatly increased.
5. Inherently better shock and vibration characteristics are obtained.
6. Possibilities for redundant techniques are greater.
7. Radiation resistant qualities are improved.
8. Number of external connections are greatly reduced.

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N67-31598

36. A TEMPORARY SYNCHRONOUS CLOCK SOURCE FOR SPINNING SPACECRAFT

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A laboratory breadboard of a spaceborne synchronous clock pulse generator is described. The generator output may be used, following a short period of synchronization to spacecraft spin-rate, to establish an accurate third reference-axis for approximately 1-hour. This device can simplify the implementation required for arbitrary reorientation of the spacecraft spin-axis. The design, operating characteristics, and physical difficulties during debugging are discussed. The difficulties encountered prompted the development of a flexible, low-priced breadboard technique including all necessary hardware. A thorough exposition of this technique is a major product of the paper.

The Synchronous Clock Source (SCS) breadboard was designed and tested in the summer of 1965 and was the first application of integrated circuits by the Central Computers and Sequencers Section at Jet Propulsion Laboratory (JPL). Because the SCS was simple enough to yield early test results and yet sufficiently complex to illustrate problems that might be typical of larger integrated circuit (IC) systems, it was an effective vehicle for an introduction to IC's.

Debugging experience with the SCS breadboard showed that maximum exploitation of the small IC sizes during early system development phases is inadvisable. Numerous difficulties, traceable to the inaccessibility of closely packed circuits, connectors and wires, were encountered in trouble-shooting and making logic changes on the breadboard. Because of these difficulties, a search was conducted for other breadboard hardware that retained the advantages of easy circuit replacement, expandability, and versatility without the disadvantage of mechanical intricacy, contact unreliability, increased capacitance, and noise sensitivity. Nothing commercially available was found to be suitable. The authors set out, therefore, to develop new breadboard hardware. Originally intended only for use on another SCS breadboard, the technique that evolved is now being used successfully in other applications as well. The description of this breadboard technique is a primary objective of this paper.

The SCS is composed entirely of monolithic elements from the Sylvania SUHL line. A total of 109 IC devices (79 flip-flops and 30 gate elements) are utilized. The power consumption is 4.7 watts from a single 5-volt dc power supply. Mounting of and connection to the IC's was accomplished with AUGAT breadboard sockets from the #8076 series.

The SCS was designed to be used on unmanned spin-stabilized interplanetary spacecraft on planetary missions. It furnishes a temporary attitude reference that enables reorientation of the vehicle's spin-axis to any desired direction. Such a reference is necessary if a spinning spacecraft is to perform trajectory-correcting maneuvers at varying and appreciable distances from the earth. The normal orientation of the spin-axis defines a spacecraft-centered coordinate system. Because it is spinning with the spacecraft and its instantaneous relationship to any convenient set of celestially fixed axes is unknown, this system alone cannot be utilized in maneuvering the spacecraft. An additional reference in time or space is needed. Two means of obtaining this reference are (1) directly from an optical celestial-body sensor, e.g., a sun sensor or planet sensor, and (2) indirectly from the SCS (which also depends temporarily on a simple celestial sensor for synchronization information).

In most applications, a number of advantages accrue from utilizing the SCS rather than relying solely on a celestial sensor to supply the missing directional information. These advantages are derived from the simpler spin-axis pointing systems that are possible. The modes of interplanetary cruise attitude that have been recommended for various missions include spin-axis pointing toward the sun, toward the earth, or perpendicular to the ecliptic. From a systems point of view the simplest of these is probably the sun-oriented mode; the others introduce undesirable system or subsystem complexities. The SCS is intended for use with the desirable sun-oriented mode. The celestial sensor as a direct reference source, on the other hand, is simple only with the less attractive earth-oriented mode; then the sun may be used as the reference celestial body, and its easy distinguishability simplifies the sensor optics and electronics. The need to keep the spin-axis normally pointed toward the earth causes increased complexity in almost all the other spacecraft subsystems and in-flight support operations, thus reducing overall mission reliability.

The direct attitude reference introduces other difficulties when the spacecraft spin-axis is not earth-oriented. Although initial pointing of the spin-axis and cruise attitude control are now simplified, a complicated multi-sensor optical system or two orthogonal velocity corrections for each trajectory change (the latter in case the spin-axis is perpendicular to the ecliptic) will be required. This again adversely affects mission reliability.

In every situation, undesirable penalties are imposed by the use of a direct reference. Incorporation of the SCS reduces these penalties because it leads to simplified spacecraft configurations. The simplest configuration results if the spin-axis is oriented toward the sun. Reference bodies can be chosen from any of the near planets — earth, Jupiter, or any of the bright stars. While these are not as convenient as the sun, they are adequate because of the relatively narrow field-of-view needed for the sensor synchronizing the SCS. In most applications, the sensor can be body-fixed. In others, a single degree of freedom with two or three positions may be desirable.

The SCS provides a source of pulses with frequencies variable over a limited range; yet it exhibits the stability of a crystal-controlled oscillator. Once synchronized with the spin of the vehicle, the output pulses will continue to coincide with a known direction of any predetermined spacecraft axis. The pulses will remain synchronized for more than 1 hour with a total accumulated

effective error of less than 0.5 degree from the original synchronization direction. During this period a programmed set of jet impulses, timed by the SCS output pulses, can rotate the spacecraft spin-axis to any desired direction. Of course, proper system operation depends on an invariant spin-rate and the cancellation of induced wobble during the precession.

A block diagram of the Synchronous Clock Source is shown in Figure 36-1. The system design was based on the assumption that spacecraft spin-rates would be within 5 percent of one revolution/second. It can be adapted to other expected spin-rates and deviations.

The system operates in the following manner. The output divider, composed of two maximal-length linear shift registers, divides the pulses from the summing gates by  $2^{14}$  and  $2^{21}$ . Following synchronization, its outputs 1 ppr and 512 ppr will occur at the rates, respectively, of once and 512 times per spacecraft revolution. The count pulse generator, a 21-stage ripple-through counter, receives 1.975-MHz pulses from the crystal oscillator and squarer. Outputs from the last 18 stages are presented to the summing gates, which are controlled by flip-flops in the memory register. Clock pulses are supplied to the summing gates at 3.95 MHz, twice the counting rate of the count pulse generator. Alternate pulses are automatically passed through to trigger the output divider. Therefore, in the absence of other pulses, the output divider operates at 1.975 MHz. Under these circumstances, the 1 ppr is generated at approximately 5 percent less than 1 pps. The other pulses are selectively passed through the summing gates under control of the 18 count pulse generator stages and memory register flip-flops. Depending on the states of the flip-flops, these pulses will be added at rates from  $1.975/2^4$  MHz (122kHz) down to  $1.975/2^{21}$  MHz (0.94Hz). If all of these pulses are presented to the output divider, it produces 1 ppr outputs approximately 10 percent faster than before. Once per spacecraft revolution, the celestial sensor emits a pulse as the reference body passes its view. During the calibrate period this pulse is compared with the 1 ppr. Depending on which pulse is faster, the memory register is adjusted to bring the two

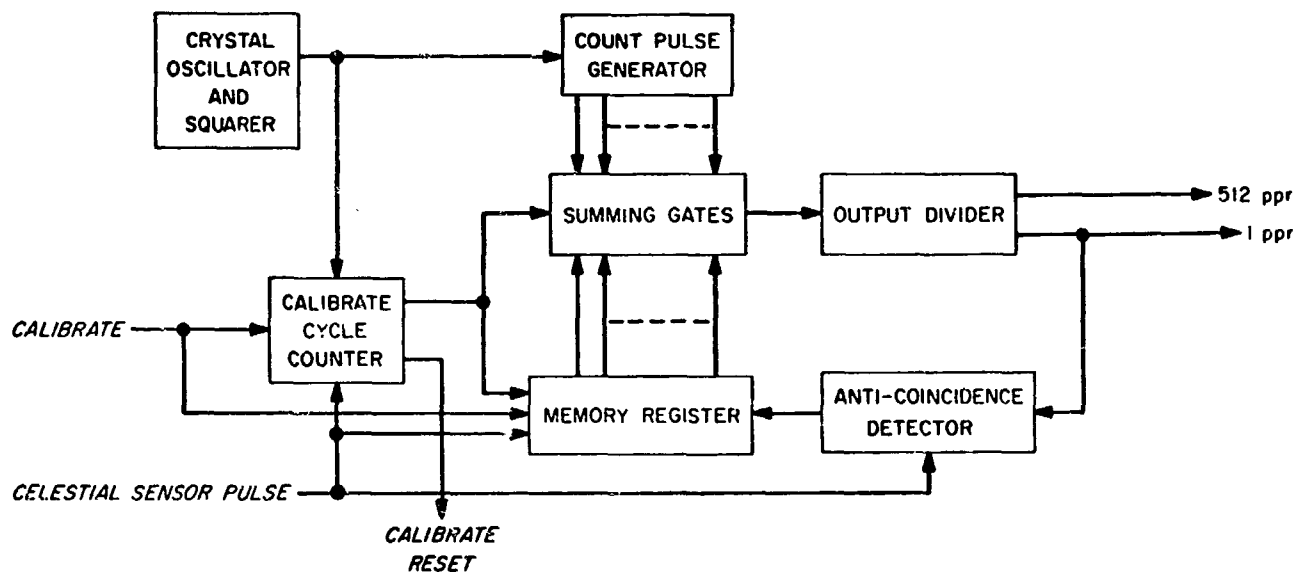


Figure 36-1—Block diagram, synchronous clock source.

rates closer together during the next spacecraft revolution. The nineteenth celestial sensor pulse following the appearance of the calibrate signal causes the calibrate cycle counter to overflow; this generates a calibrate reset pulse, ending the calibrate period. By this time the 1 ppr and the celestial sensor pulse will be synchronized to within one-half microsecond. Because of the occasional aperiodicity of the pulses to the output divider, the 512-ppr pulses divide a spacecraft revolution into segments that are equal or that differ by one-fourth microsecond. This corresponds to an error of less than 0.25 second of arc and is insignificant compared to other error sources.

Testing of the breadboard required simulation of the celestial sensor pulse. A variable, stable 1-pps source was unobtainable, so an available crystal-controlled 1-pps pulse generator was substituted for the celestial sensor, and the oscillator in the crystal oscillator and squarer was replaced with a Hewlett-Packard Company Model 511A frequency synthesizer. This expediency reversed the role of the SCS. Now the SCS pulse source, rather than the pulse from the celestial sensor, was variable. However, the variability of either pulse source merely determines the initial conditions of synchronization; during and after the Calibrate period, both sources are "rock steady." Relative performance of the SCS was therefore unchanged; only the frequency deviation that could be accommodated was somewhat decreased.

The synthesizer, a digital device with up to 10-digit precision, was operated between the limits allowed by the SCS of 3.729 MHz and 4.195 MHz. The center of the range, 3.948 MHz, differs from the design center frequency by 0.05 percent. This small discrepancy is accounted for by the inaccuracy of the crystal oscillators. The frequency deviation that could be accommodated was  $\pm 5.9$  percent, slightly less than the normal theoretical limit of  $\pm 6.25$  percent as expected.

Determining the length of time that the SCS remained in sync\* was accomplished with the help of a circuit that turned an indicator on when the minimum interval between a 1 ppr pulse and a Celestial Sensor Pulse exceeded 3 milliseconds. During a total of 300 hours of actual test time in the laboratory environment, the SCS consistently remained in sync for periods of 3 hours following each calibration. This performance was unchanged by power supply voltage variations between 4.0 v and 5.8 v. At the low end, increased delays in the Summing Gates and in the feedback circuits of the Output Divider caused erratic operation and prevented calibration. The high end was limited by the current capacity of the power supply. Since both excursions exceeded the normally specified  $\pm 10$  percent for spacecraft subsystem supply voltage variations, no effort was made to extend either limit.

Figure 36-2 is a photograph of the SCS breadboard with the 18 Memory Register state indicators in the foreground. Use of the breadboard approach shown was an attempt to approximate flight packaging density as closely as possible and still retain some measure of convenience in making

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\*"In sync" is defined as the condition, following calibration, in which the maximum smallest interval between any 1PPR pulse and Celestial Sensor Pulse is less than 3 milliseconds. This corresponds to an approximate total mean rotation of 1 degree.

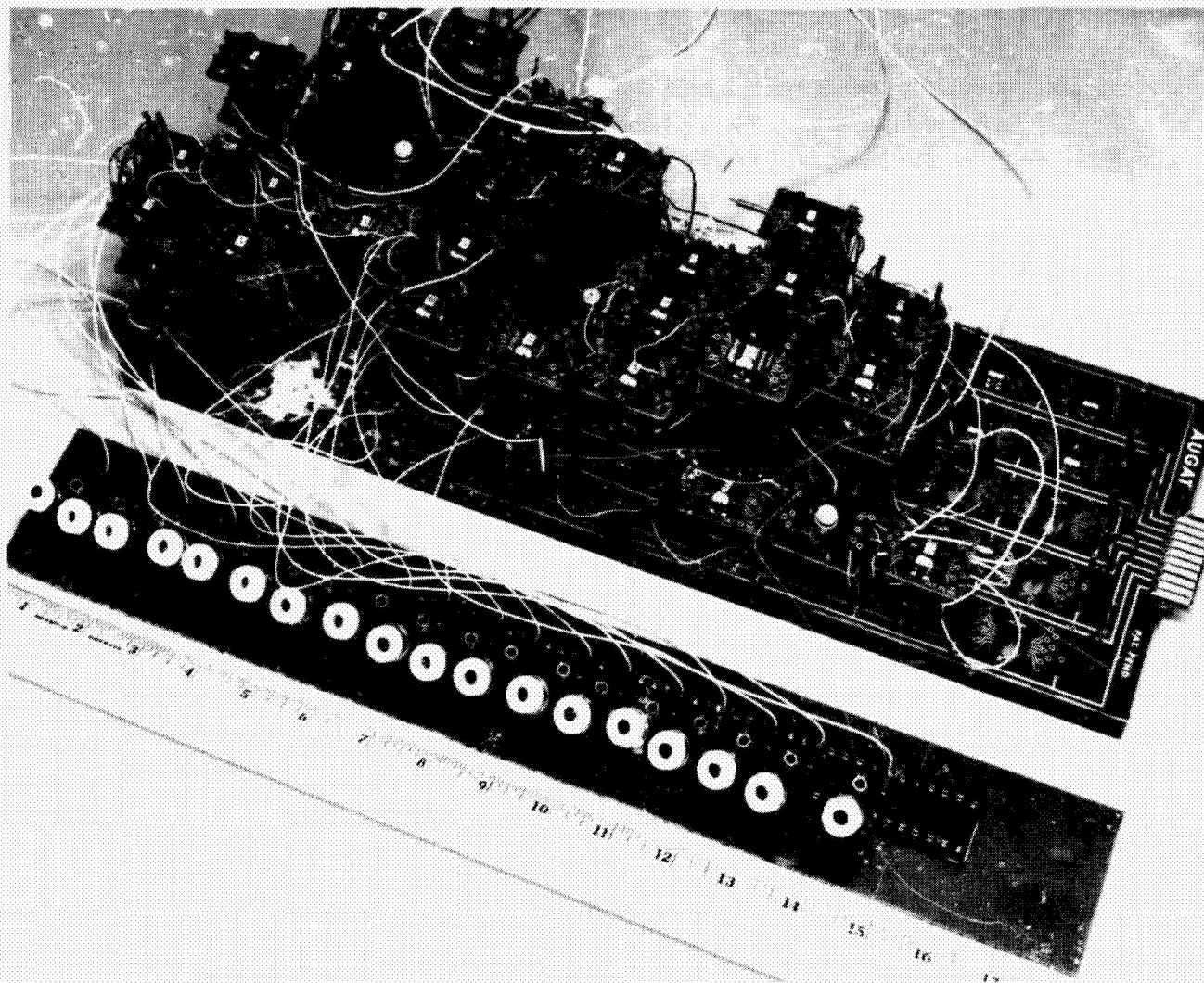


Figure 36-2—Laboratory breadboard, SCS.

changes. Very soon, though, the nature of the problems which this approach generated became evident. By the end of the first day of debugging, it was obvious that this "high-rise" technique was inappropriate for breadboarding IC systems. Although power was initially applied to only one "street" at a time, debugging efforts were soon virtually stalled by numerous intermittents and by the maze of wires and connections that could not be reached or seen. Difficulties were magnified because the entire breadboard had been wired before debugging. This was done because wiring was easiest if a horizontal plane was completed before the next higher level was started. On the other hand, a layout of logic blocks in vertical planes was most practical from the standpoint of shorter lead lengths and higher density. Thus, a sequential process of wiring and debugging was incompatible with either ease in wiring or good electrical practice.

As it turned out, good electrical practice was not good enough. In Figure 36-3, a close-up of the SCS breadboard is shown. Vertical spacing of the device-mounting sockets was obtained by



using unwired jumper-pins as spacers. These also served as convenient vertical feeds for ground and power connections. Additional columns were employed where possible — i.e., at unused terminals — for increased rigidity (and earthquake protection). Two such columns, barely discernible, are in the "building" shown in Figure 36-3. Horizontal distribution of ground and power was provided with jumpers along each "street" from "building" to "building" on the lowest level. "Crosstown" distribution was accomplished at the end of the motherboard. This parallel-series-parallel arrangement was found to produce excessive noise at the ends of the runs. It was necessary in order to achieve consistent operation, to introduce additional ground and power jumpers at "roof-top" levels both in the "uptown-downtown" and "crosstown" directions.

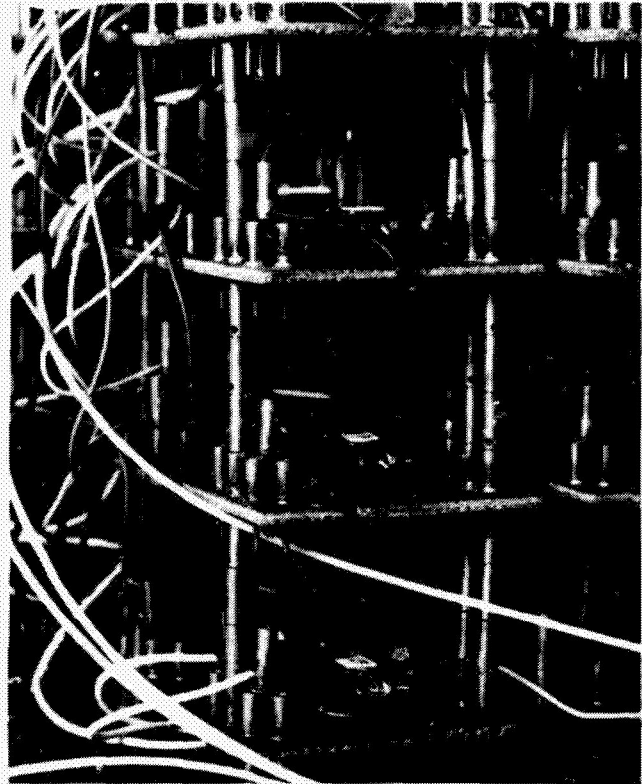


Figure 36-3—Close-up view of breadboard connections.

Debugging of the SCS took approximately 10 weeks. It is estimated that the new SCS breadboard using the technique to be described below will be debugged in one-fifth that time. Most of the savings will be due primarily to the inherent physical convenience of the new technique. As just indicated, the breadboard technique initially used for the SCS had a number of inherent weaknesses. In summary, many devices were mechanically inaccessible, friction contacts did not provide reliable connections, capacity effects were severe, and consequently, the system noise level was high. Experience with this breadboard inspired the search for a better technique.

The initial problem was to set up a number of criteria by which candidate techniques could be evaluated. These criteria were rapid and simple fabrication including easy replacement of logic devices, low cost, and versatility. Considerable effort was expended in attempting to find a commercial breadboarding scheme that met these criteria. Nothing satisfactory was discovered and it was finally decided to develop a technique in-house. The starting point was a commercial technique that most closely met the aforementioned criteria. This included the printed-circuit-card for mounting of the logic devices and the connector on which the interconnection harness is built. The major disadvantage of this commercial technique, and one which was considered overriding, was the inability to obtain the exact line of logic devices required for a given breadboard at a reasonable cost.

The next decision involved the number of IC logic devices to be mounted on the printed-circuit-card. In order to maintain the greatest flexibility in the type of integrated circuit that could be used, it was decided to bring each and every lead of the IC device out to the connector. This meant



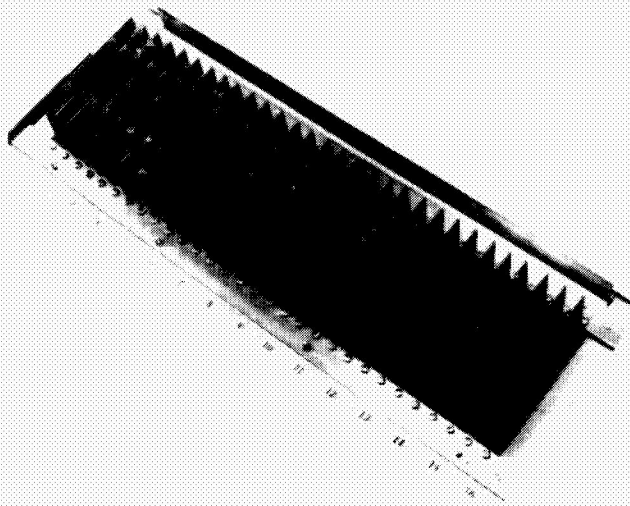


Figure 36-4—SCS breadboard using new technique, top view.

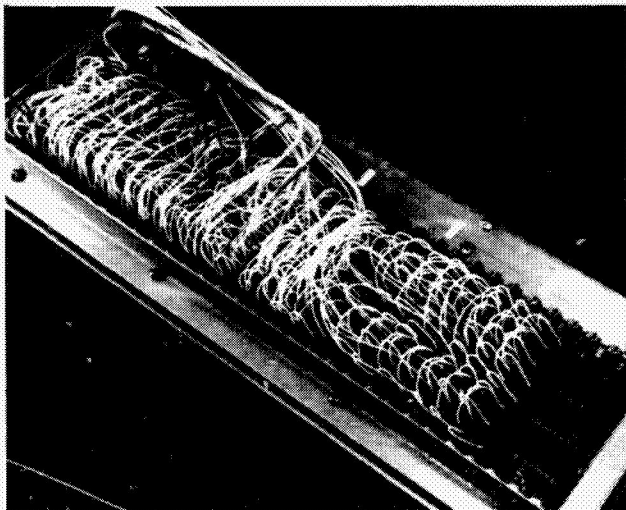


Figure 36-5—SCS breadboard using new technique, bottom view.

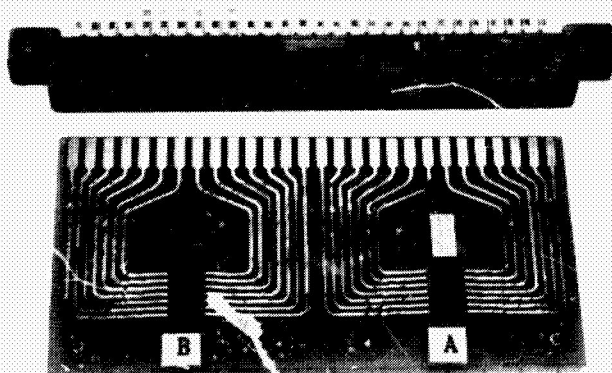


Figure 36-6—Flatpack PC board and connector.

that the connector would be the limiting component in the technique. The connector must have a sufficient number of pins to provide some multiple of fourteen contacts. In order to provide a maximum density, yet maintain ease of fabrication, a double readout connector with a pin spacing of 0.125 inch was used. After searching through the various connector catalogs, it was determined that a 56-pin, double readout connector most closely fit the requirements. With this size connector it was possible to use a double sided printed-circuit-card with two IC devices mounted on each side. This size card was sufficiently small to allow complete replacement of the card at a low cost yet provide a density that would approximate the worst case flight configuration.

Figure 36-4 shows the final result as it applies to the SCS. The connectors are spaced on 5/8-inch centers and occupy an area of approximately 15 by 4-1/2 inches. The total depth of the breadboard, including the harnessing, shown in Figure 36-5, is approximately 3 inches.

Figure 36-6 shows a view of the board and connector. The board is 1/16-inch glass epoxy with dimensions of 3-9/16 by 1-3/4 inches. The pattern shown is repeated on both sides of the card. The connector pads on the edge of the card are spaced on 1/8-inch centers with a width of 0.070 inch. The pads for mounting of the IC device will accommodate any device with a lead spacing of 0.050 inch, which is the industry standard. The printed circuits between the device pads and the connector pads are 0.025 inch wide. The board is gold plated to provide a good surface on the connector pad and to simplify subsequent solder plating. The board is then solder plated to a thickness of approximately 0.003 inch in the mounting area. To reduce cost of the process, the board is masked in a simple manner somewhere in the area between the

mounting pads and the connector pads. This is not critical as long as the mounting pads are solder plated and the connector pads are not.

The connector shown is a Continental device, although several manufacturers make a similar device. The contacts are of the bellows type, with a number of options as to material and plating available. The connector shown also indicates an eyelet termination, again with a number of options available. The connector mounts in a card rack with a spacing of 4.030 inch with a choice of threaded insert, through hole, or bushing available. The spacing between connectors can be as tight as 3/8 inch, but this spacing limits accessibility in making wiring changes.

This particular connector type allows both cards and connectors to be indexed. A slot is required between the connector pads of the board, and a small insert is required in the connector in the provided slots, as shown in Figure 36-6. This of course helps to prevent damage to logic devices especially if several families of logic devices are used in a single breadboard. Mounting of the logic devices on the boards requires that the leads be formed in a manner similar to that used in a flat layout. To accomplish this operation, JPL has developed a lead-forming tool. The IC is positioned in the tool and one simple motion clamps the leads close to the body and forms the leads in the prescribed manner. The tool was originally designed by Darrell Port of JPL and modified by John DeJong of JPL.

The actual soldering of the IC devices to the board was accomplished with a welding-head fitted with a special tip that resistance solders as many as seven leads simultaneously. Figure 36-7 shows a closeup view of the head and tip. The devices can be hand soldered, of course, but use of this machine greatly decreases the time required for this step. This breadboard technique was used on other programs in addition to the SCS. It was used in the operational support equipment of the Mariner Mars '69 Central Computer and Sequencer breadboard. In this system, approximately 120 logic devices were used. Figure 36-8 depicts another advantage of this technique; namely, the flexibility to mix boards of discrete components with the IC boards. The ease with which modifications can be made with this technique was also demonstrated on this particular piece of equipment. A failure in the series regulator of a power supply inadvertently destroyed all the integrated circuits in the rack. It took only five manhours to completely remove and replace all 120 devices on the 30 boards.



Figure 36-7—Combination head solders or welds seven leads simultaneously.

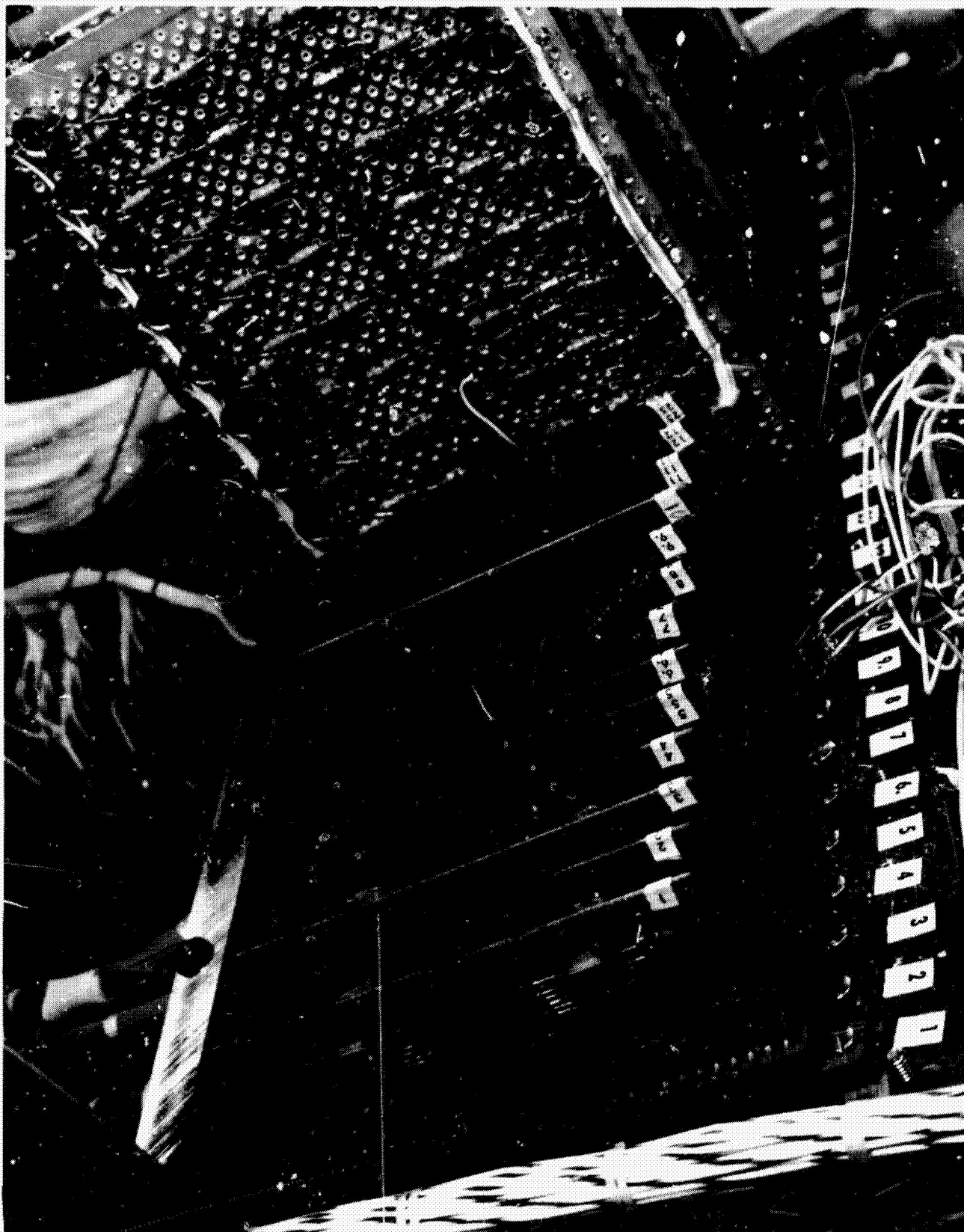


Figure 36-8—Hybrid breadboards technique.

Another much larger system at JPL used this breadboard technique. The program was the Strapdown Electrostatic Aerospace Navigator (SEAN). This breadboard used a total of 700 IC devices from two families. The majority of the components are of the Signetics 100-J series, while a number of 30-MHz counters were included — fabricated from Sylvania's SUHL II family. The 30-MHz counters did not suffer from the worst-case packaging configuration that this breadboard technique imposed on them. This breadboard also points out the fact that different families of IC's with different  $V_{cc}$  and ground pin connections can be mixed easily.

Among the disadvantages is the possibility that very large systems might be subject to increased system noise. Use of a ground plane with this technique is difficult. Isolation of clock lines or other signal lines is also difficult. Experience with the SEAN program indicates, however, that the point where these problems are encountered is well above the 700 IC count level.

Another possible problem area that must be considered is the interconnection complexity of very large systems. If the system to be breadboarded is large and requires many different families of ICs, interconnection of  $V_{cc}$  and ground pins might become a difficulty especially if  $V_{cc}$  and ground pins on the devices themselves are not diametrically opposite. Interconnection of signal wires can also become quite complex with large cable bundles required.

The advantages include versatility as a major item. Any IC family of 14 leads or less that is packaged in a standard flat-pack can be used with no changes in the boards or connectors. Boards with discrete components for input-output buffer functions can be intermingled with the IC boards easily. Probably most important is the fact that the details of this technique can be easily modified to meet a particular requirement. Special boards can be fabricated with different patterns, special connectors with taper pin terminations can be used, or any one of many other possible modifications can be incorporated within the framework of this technique.

Another advantage is the low cost of the hardware required. Standard cards can be built and used on breadboards for many different systems. Both cards and connectors can be indexed to avoid damage, which obviously cuts replacement costs. If desired, the cards are sufficiently small to discard if a device fails or is damaged.

The fabrication convenience is another advantage. Using the aforementioned lead-forming tool and the welding-head to solder seven leads simultaneously makes mounting or replacement of IC's simple and straightforward. Wiring is easily accomplished with or without a wiring list to work from. The technique described also is a simple and fast way to check the noise susceptibility of a flight system design by approximating worst case packaging of a flight configuration.

We feel that we have accomplished our main goal in developing a breadboard technique that is easy to use, easy to modify, and results in a reasonable breadboarding cost. Of course, revisions and updating of this basic technique are anticipated as a wider range of problems are encountered on future programs, but the rudiments of this technique will remain the same.



N67-31599

37. EVALUATION OF SEMICONDUCTOR DEVICES USING THE SCANNING  
ELECTRON MICROSCOPE

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The scanning electron microscope (SEM) developed by the Westinghouse Electric Company has been useful in the detection of failure mechanisms of semiconductor devices. Since integrated circuits are becoming smaller, and hence more difficult to probe, and large circuit arrays are coming into being, the scanning electron microscope will be a useful tool in examining quantitatively integrated circuit parameters. At the present, however, a qualitative examination of integrated circuits is being performed, and relationships are being established between various failure modes and their resulting phenomena as observed with the SEM. In the future, it is anticipated that reliability of devices will be improved on the basis of observations with the SEM.

The original concept for a scanning electron microscope was proposed by M. Knoll in 1935 (Reference 1). Three years later, also in Germany, M. von Ardenne built an instrument which employed mechanical scanning (Reference 2). In 1942, Zworykin, Hillier, and Snyder described a scanning electron microscope which is closely related to our present instrument (Reference 3). This machine used the variation of secondary emission over the surface of the specimen, and was used chiefly for the examination of metal surfaces. The emitted electrons were picked up on the first dynode of an electron multiplier. Prior to the war, the signal-to-noise ratio of these multipliers was very low, causing poor contrast in the resulting images on the screen of CRT tubes. After the war, beryllium-copper dynodes came into general use, enhancing the signal-to-noise ratio. In 1953, at Cambridge, McMullan employed these new electron multipliers, and was able to show that it was unnecessary to rely solely on the variation of secondary emission to provide contrast. He found that the multiplier current depended strongly on the angle between the incident beam and the portion of the surface on which it was falling (Reference 4). As this angle varied, though minutely, from point to point over the surface of the specimen, the final picture built up on the CRT was related to its topographical structure.

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Westinghouse Research Laboratories began building their first scanning microscope around 1960. O. C. Williams and T. E. Everhart, both students of McMullan, collaborated on this machine, in which the secondary electrons were sharply curved and collected on the surface of a scintillator. The primary beam was scanned in a raster similar to that used in TV pictures, and the output of the scintillator, after suitable amplification, was used to control the brightness of the spot on the CRT image. The oscilloscope sweep was synchronized with the beam raster and using long life phosphor on the CRT, the image built up was a magnified view of the surface topography of the sample.

For the past year, the Astrionics Laboratory has had in its possession a scanning electron microscope (Figure 37-1). The instrument was purchased from Westinghouse and has been used as a research tool for investigating failure mechanisms in integrated circuits. Figure 37-2 is a schematic outline of the principal parts of the Micro-Scan. Here, an electron gun accelerates the beam, an electron current of about 200 microamperes, to roughly 25 kilovolts. The acceleration takes place over a fairly short distance, allowing the electrons to drift through the magnetic

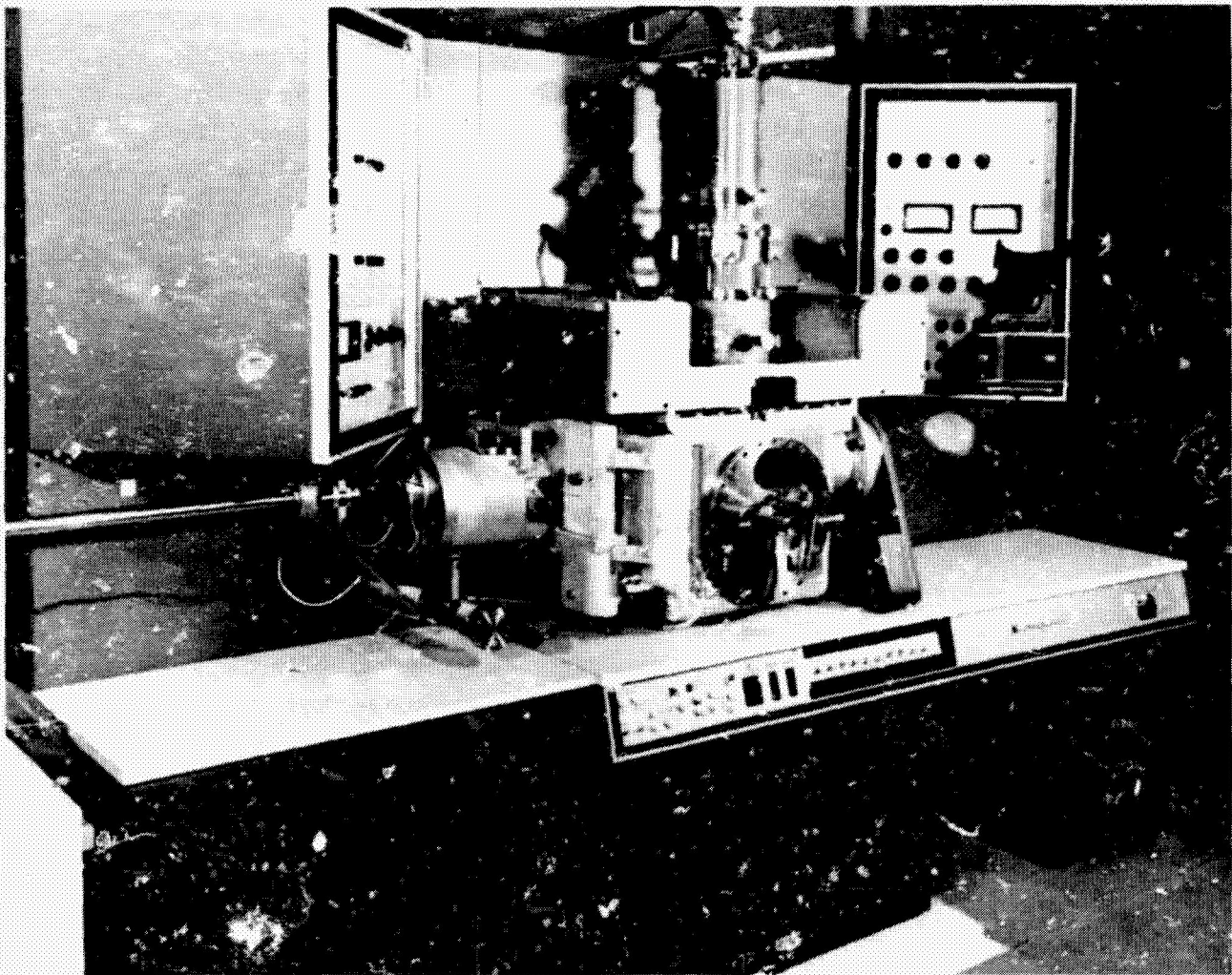
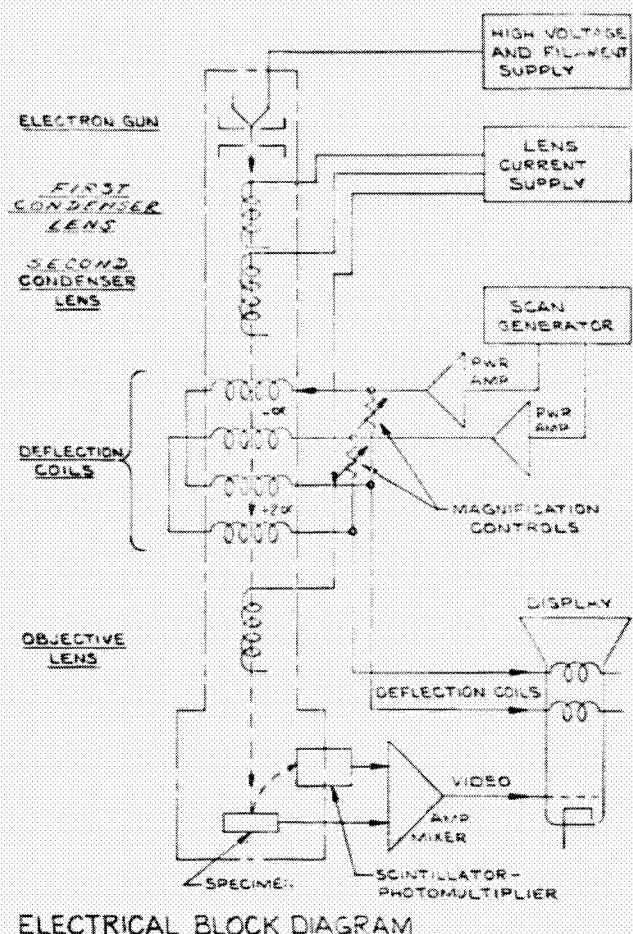


Figure 37-1—Complete view of the scanning electron microscope.



ELECTRICAL BLOCK DIAGRAM

Figure 37-2—Electrical block diagram of the scanning electron microscope.

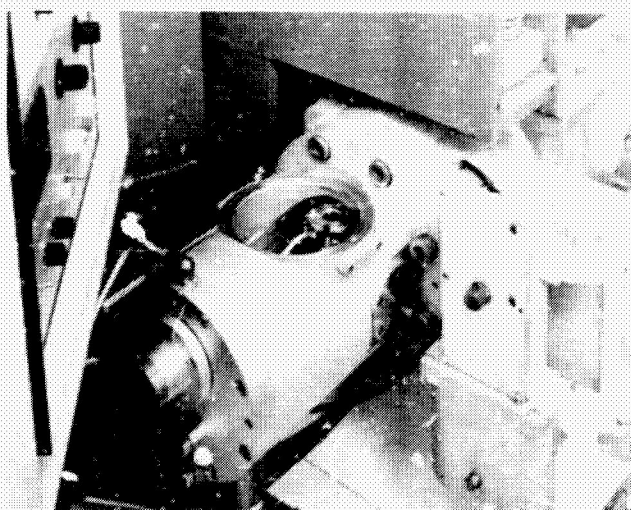


Figure 37-3—Specimen in the preparatory chamber.

lenses as a monochromatic ray. Surrounding the filament is a focusing element, slightly negative with respect to the cathode (the Wehnelt grid). The first two magnetic lenses are condensers demagnifying the source. The final lens, the objective, brings the beam to focus on the target. The current reaching the target ranges between  $10^{-9}$  to  $10^{-12}$  ampere. Stops, apertures, and dispersion bleed off the majority of the beam prior to its reaching the target. A scanning generator produces the raster, the deflection coils being between the last condenser and the objective. The incident electrons strike the target, causing emission from its surface of primary and secondary electrons. The distinction between primary and secondary has arbitrarily been made at 50 electron volts. Secondaries, 0 to 50 ev, have been shown by Professor McMullan (in 1953) to be most sensitive to surface topography (Reference 4). These electrons are attracted to a Faraday cup, which is covered by wire gauze placed 300 volts above the target. At the base of the cup is a scintillator with an aluminized surface 10 kv above the wire gauze. This 10 kv allows all the captured electrons to strike the scintillator, whose output is piped through a light pipe to an electron multiplier. This amplified signal is then used to control the brightness of the spot on the CRT image. As previously mentioned, the CRT sweep is synchronized with the scanning raster, and the resulting image is a point-for-point magnified view of the target surface. The raster on the CRT display is held at a constant size approximately  $56 \text{ cm}^2$ , while the scanning generator allows a raster size of  $2 \text{ mm}^2$  to  $50 \text{ microns}^2$  on the target. This represents a magnification of 40 to 1500 times, respectively. In normal operation, an oscillogram takes from 1 to 4 minutes using polaroid type 57 film. The diameter size of the beam spot can be varied from 2 microns to  $1/4$  micron. With the smallest spot size, the resolution attainable is approximately 0.1 micron. K. C. Smith



and C. W. Oatley (also students of Professor McMullan) have suggested resolutions reaching 100 angstroms, although, for the present state of the art in integrated circuit analysis, the Micro-Scan has more than adequate resolving power. To prevent defocusing of the beam by air molecules scattering the electrons, and to obtain the maximum lifetime of the gun filament, the entire system is operated in the  $10^{-4}$  u./m<sup>2</sup> ( $10^{-6}$  torr, vacuum range. Samples are introduced through an isolated preparation chamber (Figure 37-3), which is an air lock for the specimen chamber. A pneumatically-operated transporter positions the sample onto a three-dimensional micrometer stage in the main chamber. This stage then positions the sample in the beam so that any desired location can be scanned. Electrical connections are made to the circuit under investigation by means of a 19-prong plug, which is available for applying any bias and monitoring any output signal. Final focusing is done by adjusting the focal length of the objective lens.

An immediate advantage of this type of microscope over the transmission or reflection type is its nondestructive, no-replica approach towards looking at surface topographies. Biological specimens with light metallic coatings are good examples of these facts. In the Micro-Scan, the large depth of field which is inherent to electron microscopes is coupled with the scanning raster. The result is an excellent three-dimensional effect. The grasshopper's knee (Figure 37-4) gives



Figure 37-4—Biological specimen — three-dimensional effect.



a good three-dimensional representation. Note that an optical microscope would produce neither the three-dimensional effect nor the good depth of field.

There are essentially two distinct modes in which information can be detected in electron beam scanning of semiconductor junctions. Secondary electron collection with a scintillator has been previously mentioned. In addition, with a reversed biased junction, the photocurrent, which is the induced electron-hole pairs generated due to the incident beam, can be collected and used to control the brightness of the spot on the CRT image. Furthermore, any combination of these modes can supply a suitable output signal for the scope. A bipolar npn transistor (Figure 37-5) gives a composite illustration of the several modes of gathering information. In location I, the primary beam generates both secondary electrons and electron-hole pairs. The electron-hole current can be detected either as electron beam induced current (EBIC) or as electron beam induced target current (EBITC). The two methods give strikingly different visual displays. This photocurrent is a powerful method of obtaining information, since interference with this flow to the collecting junction produces contrast in the display. The other areas indicate regions which give sharply different contrast.

As a demonstration of the Micro-Scan's flexible ability to detect failures in semiconductor junctions, we will begin with an optical view of a double-diffused npn transistor (Figure 37-6). A short between the emitter and base can be clearly seen. Viewing the same transistor via secondary electron emission from its surface (Figure 37-7) shows that the emitter base short is still quite apparent. In the upper portion of the photograph, a dark area can be seen in the proximity of the emitter lead. This is a piece of foreign matter. If the electron beam induced current (EBIC) is

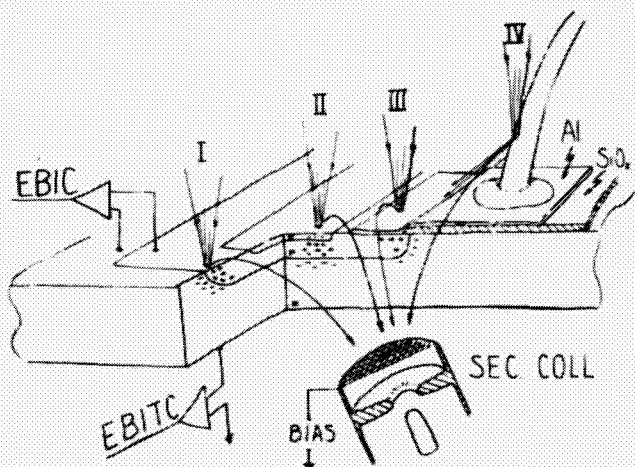


Figure 37-5—Composite view of several modes of detection.

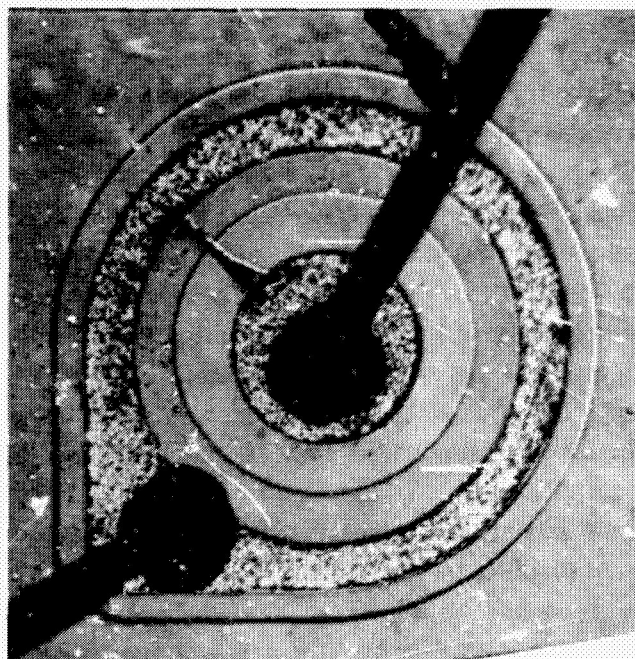


Figure 37-6—Optical view of NPN transistor with base-to-emitter short.

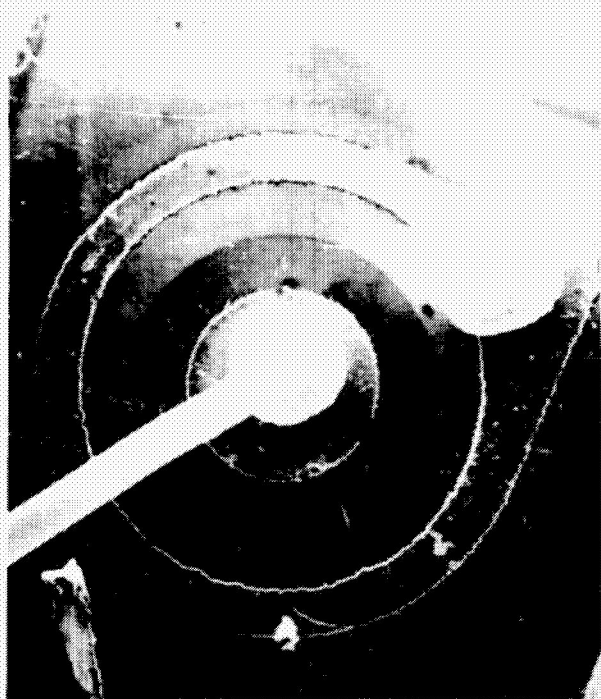


Figure 37-7—NPN Transistor via secondary electron emission.

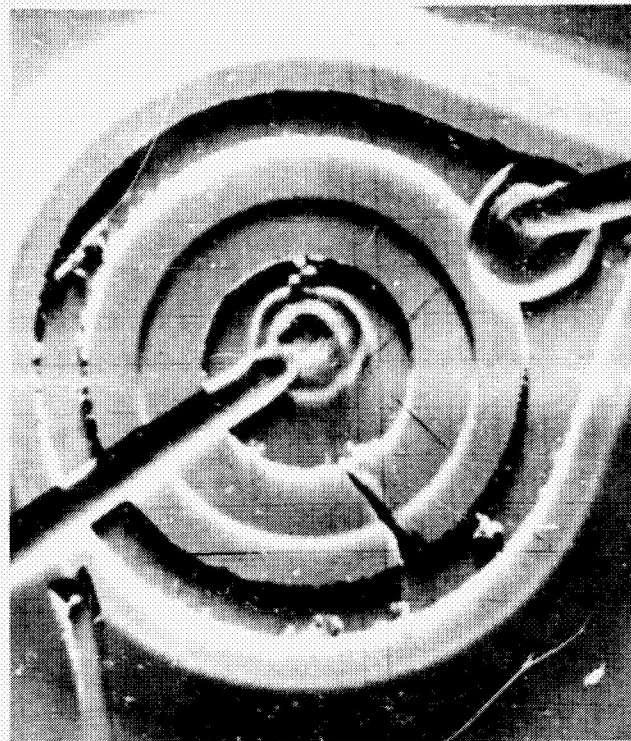


Figure 37-8—Electron beam induced current.

used as the output signal (Figure 37-8), the video display shows exceptional contrast. Again the short is quite apparent. For a three-dimensional effect, the electron beam induced target current (EBITC) (Figure 37-9) shows the relative heights of the various layers on the substrate. In checking cleanliness, the electron beam will charge dust particles on the surface, which will then show up as bright spots (Figure 37-10). The voltage contrast provides a convenient way of checking the continuity and uniformity of the evaporated aluminum leads (Figure 37-11). Notice the sudden change from black to white, which indicates an abrupt voltage change or an open lead. Electrical tests will indicate a malfunction, but no other method will pinpoint the exact location of the trouble as well as the Micro-Scan. Mixing the secondary electron signal with the photovoltage (EBIC) (Figure 37-12) can be used to display a faulty junction. Here, the circular region indicates that the junction is not really planar, but that



Figure 37-9—Electron beam induced target current.



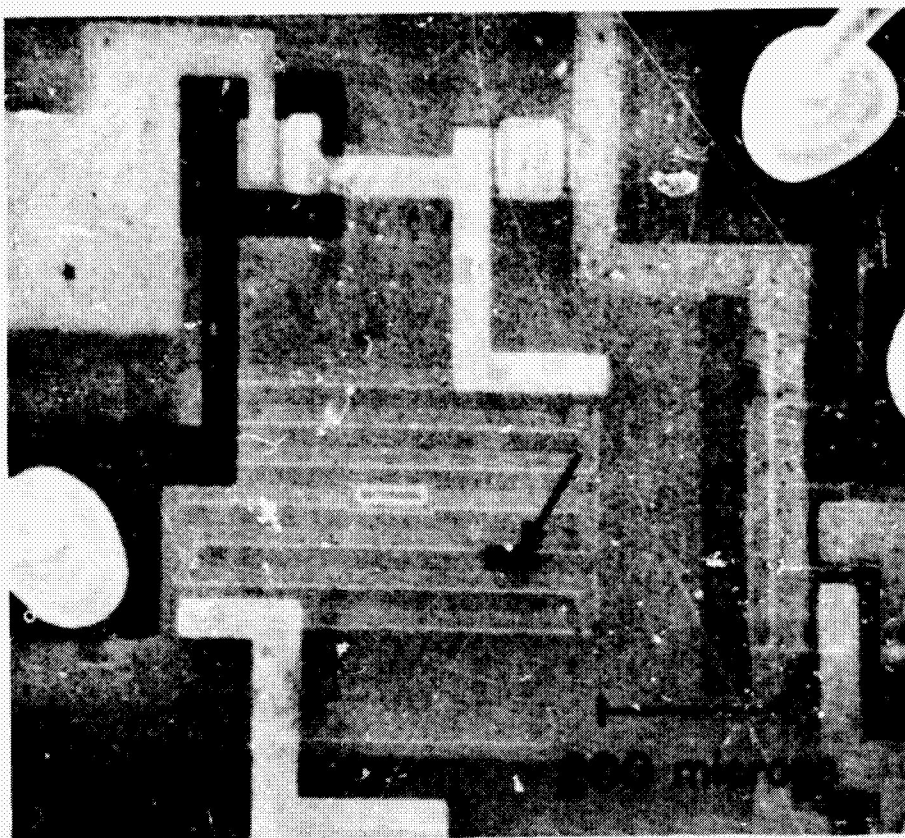


Figure 37-10—Dust particle on surface of specimen.

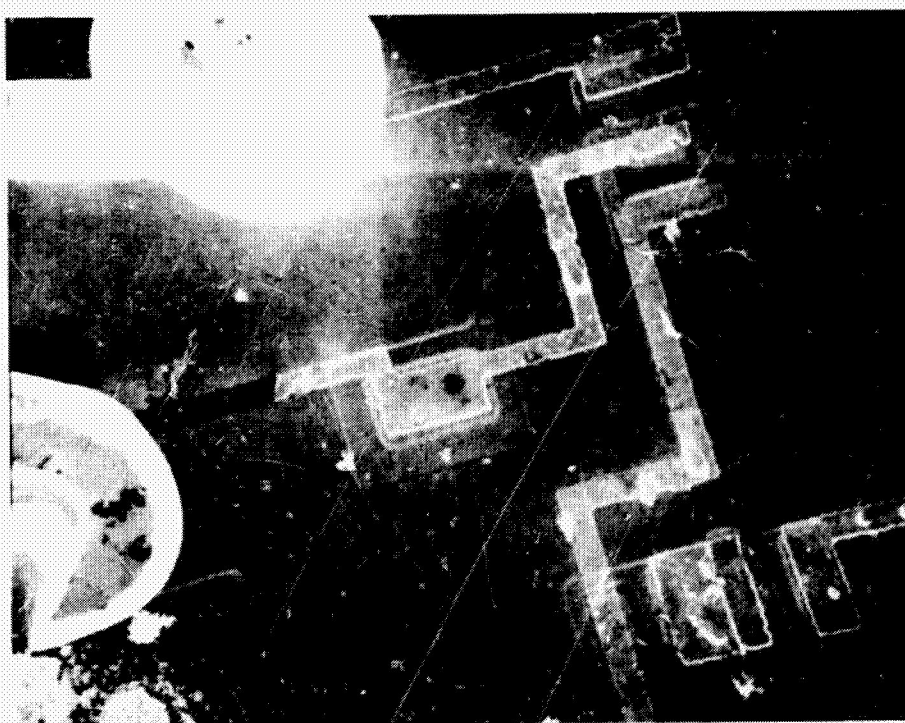


Figure 37-11—Method for locating discontinuities.

impurities have diffused much deeper than was desired. John Gaylord, at the RCA Laboratories in Princeton, recently indicated how their Micro-Scan pinpointed the location of diffusion spikes in an otherwise planar pn junction (Reference 5). Note that the boundaries of all the junctions are clearly defined, even under the passivating oxide layer. If higher magnification is used, previous damage to the crystalline surface can be viewed (Figure 37-13). In this particular case, electrical tests indicated that the device was working properly. However, such a device probably will have a rather short life-time, and the detection of these flaws by the Micro-Scan will definitely lead to their elimination. Such a simple examination as this will lead to higher reliability of "future good devices." During all these examinations, not one device has been destroyed nor have any electrical characteristics been changed. Investigation is completely nondestructive.

In addition to applications pertaining to failure analysis, it has been known for some time that photoresist can be polymerized by bombardment with electrons. The instrument can be turned around and used to trace out integrated circuit patterns on semiconductor chips. All that is needed is an external system to provide for pattern generation and control of the motion of the electron beam on the specimen. With the present instrument, use of a spot size of  $1/4$  micron gives an order of magnitude increase in the number of elements per chip. In addition, the small size of the elements will allow the use of higher frequencies. Westinghouse Research Laboratories has actually fabricated a number of junctions in this fashion.

The Micro-Scan offers some unique advantages when used to study semiconductor junctions. The work of the Astrionics Laboratory is proceeding along two paths. The first

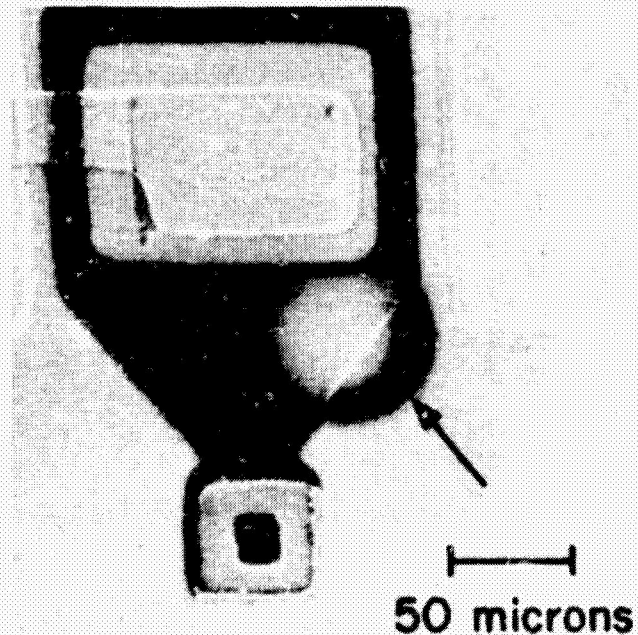


Figure 37-12—Faulty junction.

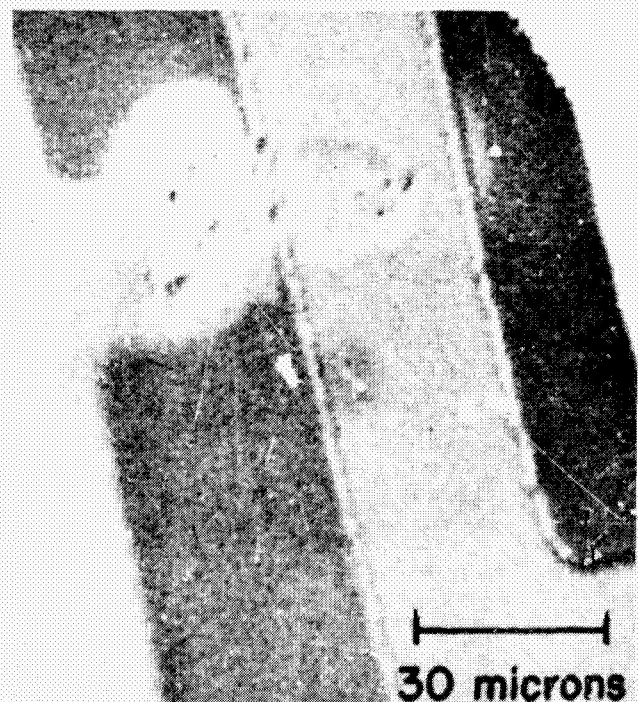


Figure 37-13—Crystalline imperfection illustrated by magnification.

assignment is a routine examination of currently available devices, with emphasis on integrated circuits. The aim of this work is to feed back information to suppliers on commonly occurring faults (which the Micro-Scan can detect), in the hope that reliability of devices used in satellites and missile systems can be improved. The second path leads us to a more fundamental investigation of failure mechanism in pn junctions. Through this work, we hope to shed further light on the cause of secondary breakdown, and, in general, to improve the overall reliability of semiconductor devices, with the major emphasis on integrated circuitry.

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N67-31600

38. FAST SCAN INFRARED MICROSCOPE FOR IMPROVING  
MICROELECTRONIC DEVICE RELIABILITY

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A testing process is presented which uses infrared radiation to measure thermal and electromechanical aspects of elements of a circuit. This method evolved from the incapability of conventional test equipment and processes to measure these parameters, a limitation due mostly to the small size of the elements. A fast-scan infrared microscope has been developed to implement infrared testing; its characteristics and capabilities are described. A study is still in progress to determine other abilities of infrared testing.

Traditionally, technological progress has been a two-step function. First, a new device is created, and second, means are sought to manufacture it in a better and consistent way. In the world of semiconductors, we are now in phase 2, and every day, progress is being made toward better manufacturing methods and processes. A new approach — infrared testing — is presently being developed, as a promising technique capable of yielding large amounts of information on thermal and electromechanical parameters affecting reliability, that conventional test equipment and methods are incapable of measuring.

The cause of this difficulty lies in the physical size of the elements to be tested, and in the minimal value of the majority of the signals to be measured; semiconductor chips have an area in the order of magnitude of  $1 \text{ mm}^2$ , and into this area, some integrated circuits pack dozens of transistors, diodes and resistors (Figure 38-1). The electrical interconnections are often only a few microns in width, and making physical contact with them for test purposes becomes not only extremely difficult, but also dangerous to their mechanical and electrical integrity. On a practical basis, probe measurements can only be made prior to dicing and encapsulation.

Consequently, in most instances, only input and output measurements are obtainable through the use of conventional test equipment. This information is especially inadequate in the case of complex integrated circuitry, because it does not give information about the performance of the individual elements of the network. Because of this, the poor performance of an element could go undetected because of the compensating effect of another element. Furthermore, several design or manufacturing defects that may eventually cause a failure are not detectable by



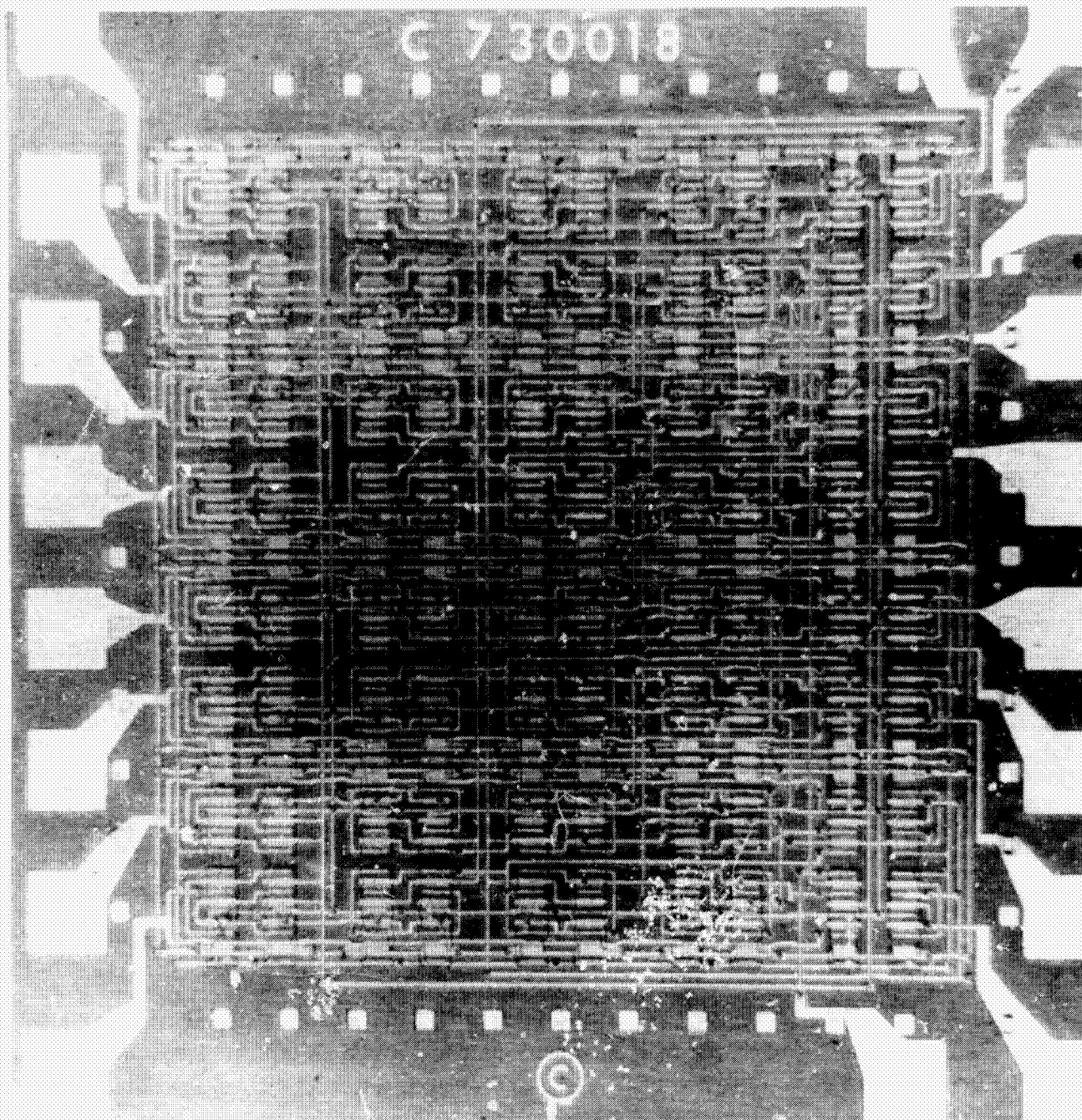


Figure 38-1—Complex microcircuit.

conventional testing. Table 38-1 shows some of the most frequent defective conditions in this class.

Infrared radiation is an electromagnetic oscillation of the same type as the electromagnetic waves that are called "visible light", and it can be thought of as "invisible light." The electromagnetic radiation band, as it is known to us today, goes from the very low frequencies of the ac oscillations to the extremely high frequencies of the gamma rays and cosmic rays produced by



Table 38-1

## Semiconductor Defects

Semiconductor Bulk Material	Resistivity irregularities Dislocations Lattice anomalies Secondary breakdown
Design	Junction proximity Thermal interaction
Surface	Pinholes Contamination Ion migration Channeling
Mechanical	Uneven metal deposition Poor bonding of deposited elements Poor bonding of lead wires Poor die bonding Cracks, voids, and scratches

variations in energy of subatomic particles. All these radiations are of the same nature, travel at the same speed (the speed of light), and have the same characteristics of transporting energy.

The infrared radiation is contained in the area between the visible light and the radio waves. There is even an overlap in the microwave radiowave region, the difference being that the radio waves are usually of the coherent type, while the infrared radiation is normally of the incoherent type. This fact can be easily understood when we think that the infrared radiation is generated by the vibrational and rotational movements of the atoms and molecules of which physical matter is composed. Consequently, the spectrum of the infrared radiation emitted by physical matter is extremely broad and peaks at a frequency that varies with temperature.

A physical body containing atomic and subatomic particles of all possible sizes would emit at all infrared frequencies, on an uninterrupted spectral band. Such a physical body is called a "blackbody," and although it does not exist in nature, very close approximations to it can be made, and all infrared radiation laws are formulated upon it. Although no physical body has the perfect spectrum of the theoretical blackbody, the shape of the radiation band of any physical body will depend upon its temperature and a surface condition called "emissivity". Emissivity can be thought of as the quality that in the visible range is called color.

Besides the infrared radiation emitted by physical matter because of thermal agitation, infrared radiation is also being emitted by semiconductors, independent of the thermal status. This is

called recombination radiation, and it is due to the energy liberated by the current carriers when they step down from the higher energy level of the carrier band to the lower energy level of the valence band. The energy so liberated manifests itself as infrared radiation, called recombination radiation because it takes place when the electron hole pairs recombine. This recombination radiation is of the coherent type. It is directly proportional to, among other things, the amount of current flowing through the semiconductor and the variations in the current flow. Detection and measurement of the recombination radiation should consequently enable us to read, without time delay, modulated operation, and even pulse operation, of semiconductors. The fact that due to thermal effects, the recombination radiation takes place in a different wavelength than the radiation, can allow us, with the use of adequate filters, to read it independently from the thermal variations.

Wherever electrical current flows, a fraction of it turns into heat. This is generally called "power dissipation," and results in a temperature rise of the element through which the current flows. This thermal rise increases the power of the infrared radiation emitted by the surface of the element, and, in turn, this variation can be measured by an adequate infrared detector.

A direct correlation can thus be established between the electrical power dissipation of an electronic part of a given design and the infrared radiation emitted by it. This correlation is the key to the infrared evaluation of electrically energized microelectronic circuits.

The evaluation of passive elements can be achieved by plotting the temperature variation through them when they are subjected to a thermal gradient. This can be achieved by mapping the infrared radiation emitted by each surface point of the target. In this way, physical anomalies such as material discontinuities, lack of proper bonding, and cross-section variations can be detected and evaluated. When the target is a semiconductor chip, the infrared test equipment requirements are set by its physical size, the temperature gradients to be observed and the speed at which thermal flooding of the target takes place.

Figure 38-2 is a photograph of the fast scan infrared microscope that has been developed by Raytheon Company under contract to MSFC. On the left is the pedestal for mounting the device that is under examination. The microscope is for alignment and visual observation of the sample. The upper right area contains the drive mechanism for the helix and the polygon scanning system. Figure 38-3 is a functional block diagram of the instrument. Basically, the unit can be divided into five major sections: optics, scanning system, detector with cryogenic cooling, signal processing, and display system.

1. Optics. — Larger than normal optics with several unique properties were deliberately chosen for the infrared microscope. The detector aperture requirements dictated the use of a magnifying system. A 7.6 to 1 system was used. A diameter of 8 inches was chosen for the primary, and the focal ratio was set at F1.1. This long focal length enables the object to be away from the primary optics in a space of its own. It further permits the use of an off-axis system; the only aberrations from this system occur because the field is spherical rather than flat.



Figure 38-2—Fast-scan infrared microscope.

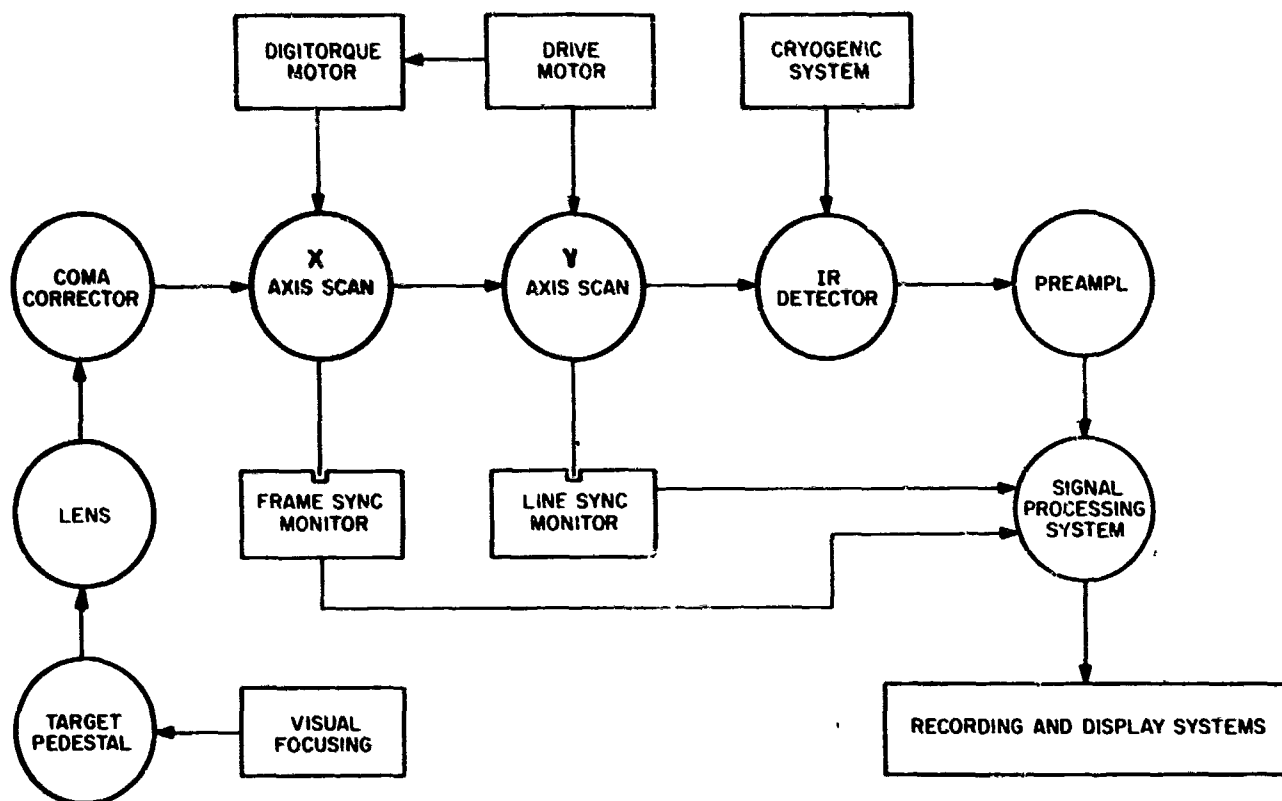


Figure 38-3—Block diagram of fast-scan infrared microscope.

However, for conditions under which this device will be used, these aberrations are of no major importance. Optical resolution of a diffraction-limited characteristic is achieved in a lens system having a concentric, spherical germanium corrector and a spherical primary lens.

2. Scanning System. — The high-speed, infrared, scanning microscope requires a unique scanning system. This requirement was met by the development of a polygon helix scanner in which a polygon, having 64 internal facets and 64 spaces, is rotated for the aperture mask of the detector at a speed of 1,000 lines per second. This scanned beam is relayed to a pair of flat annuli oriented to fold the beam 180 degrees. Only a small segment of the annuli is used each time. The main effect is to provide the system with a corner reflector. This would be the effect if the annuli were flat, doughnut-shaped surfaces of glass; however, they are split, with one end raised 0.15 inch to form a helix. When rotated together, these helixes transversely move the optical image as far as necessary to permit scanning a 1-1/2-millimeter surface at 10 cps with linear speed and 90 percent efficiency.

3. Detector with Cryogenic Cooling. — The detector and the cooling system were chosen to be compatible with the rest of the microscope. The detector has a 0.0003-inch diameter aperture with an aperture limiting mask of 13 degrees on one axis and 6 degrees on the other axis. This aperture will permit the detector to see all areas in the target plane. The detector is mercury-doped germanium with a normal operating temperature of 30° Kelvin. Cooling is provided by a

Malaker Mark 7 closed-cycle cryogenic cooler. The closed-cycle system offers significant convenience advantages over the manually-filled helium system, which was the alternate system.

4. **Signal Processing.** — Signal processing for the infrared microscope was made as simple as possible. The detector amplifier and log post-amplifier have variable gains and a variable bandwidth. To provide x and y drives for the cathode-ray oscilloscope or magnetic tape, sync pulses come from both the polygon wheel and the helix wheels. The net result is an ability to provide, on a continuous basis, a single frame image of the target to be scanned, as well as radiation (or amplitudes) versus time data.

5. **Display System.** — The instrument's output is an analog signal. The signal has a maximum frequency of 100 kc and is indexed like a video signal. Therefore, it can best be recorded by a conventional video tape recorder. This device has framing rates consistent with those held in the microscope, and can record one frame of infrared data on each diagonal line sweep of the rotating head. Information from the video tape recorder can then be reproduced sequentially as video images on an oscilloscope, and line scans can be recorded directly on a strip chart recorder. In addition, information from the video recorder can be used as the input for an A to D converter, whose output proceeds into a buffer unit for storage and future computer processing.

The smallest element of an integrated circuit is the junction, which can be only a few microns wide. Consequently, the area resolution of an adequate infrared system should be able to view them. Possibly, an even finer resolution capability would be useful, but the wavelength of the radiation emitted by the target is the limiting factor. Therefore, the instrument was designed to have the following capabilities:

1. Area resolution — 10 microns.
2. Temperature resolution — 1°C at 25°C ambient.
3. Frame composition — 100 lines/frame.
4. Scan speed — 10 frames/second or 1000 lines/second.
5. Optical magnification — 7.6.
6. Depth of field — 15 microns.
7. System efficiency — 40%.
8. IR wavelength — 2 - 15 microns.

The IR microscope is being developed for use in microelectronic device design evaluation, process quality control, and reliability screening. Once a microelectronic device engineering

prototype has been built and is operating, a thermal map of it will enable the design engineer to verify that the thermoelectric stress is as calculated at every point of the unit. Electrical overstress, resulting in excessive power dissipation, and thermal interaction, causing unwanted heating of sensitive elements, will be apparent. Once the existence of these conditions has been pinpointed, design changes can be implemented and their effects verified on a modified prototype.

Thermal maps of production units can be compared with standards established for each basic device, and any significant variation of the production process will be immediately disclosed. From this information, suitable process changes can be made to correct the defects, or anomalous devices can be discarded.

Figure 38-4 shows the circuit diagram and physical layout of a dual 3-input gate that was evaluated for its thermal design characteristics. The location is shown of every fifth line of scan of the 50 made.

Figure 38-5 is a collection of the scope displays of each scan line. A cutout was made of each of the lines of scan. This cutout was assembled into an IR profile of the circuit (Figure 38-6). By correlating Figures 38-4 and 38-6, the peak infrared emission can be related to resistors and

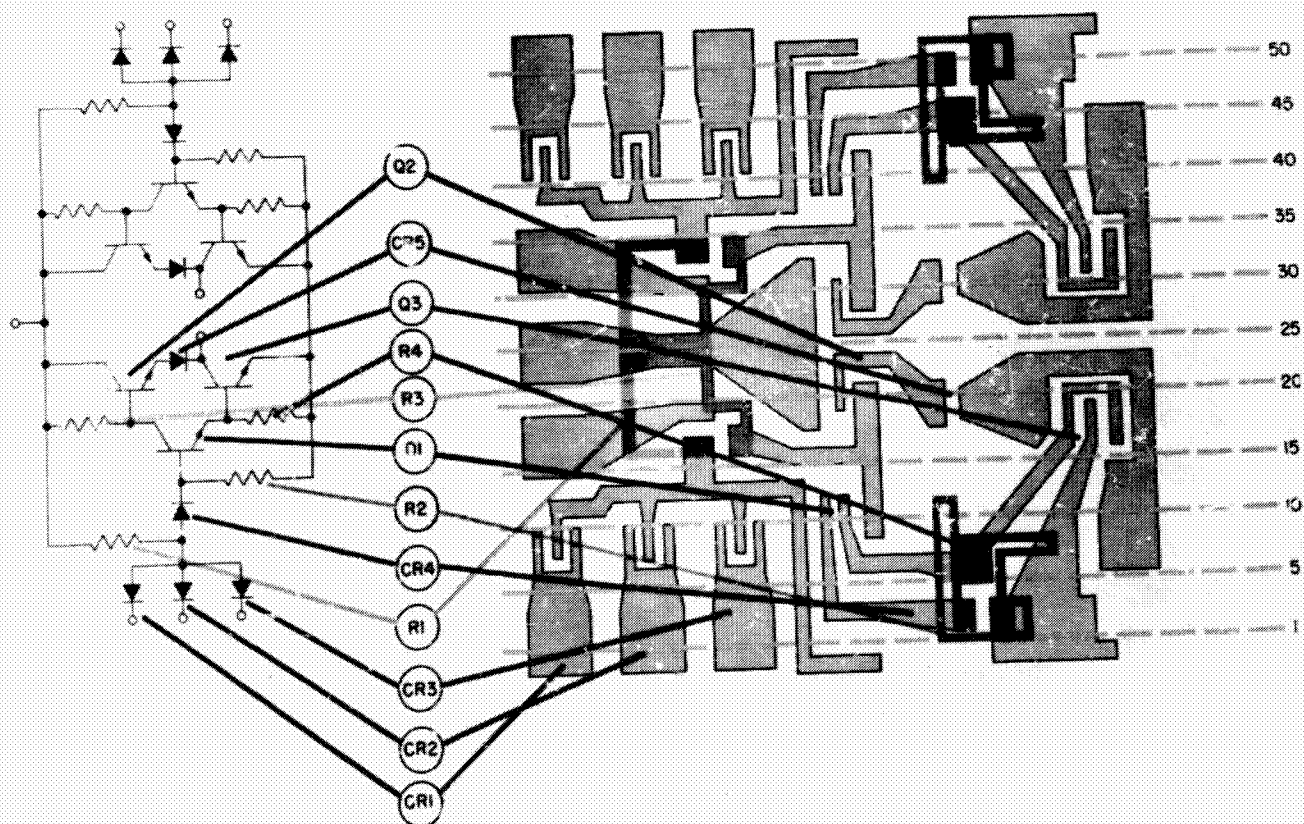


Figure 38-4—Schematic diagram and physical layout of dual gate.



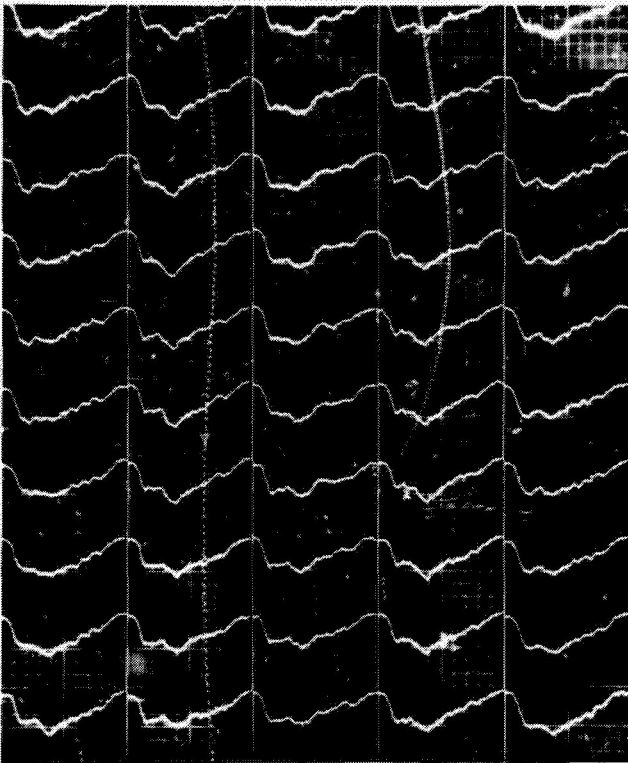


Figure 38-5—Fifty infrared scan lines of microcircuit.

transistors. This analysis shows a maximum temperature rise in the circuit of  $60^{\circ}\text{C}$ , with no major concentrations of heat, an indication that this circuit has a good, uniform thermal design.

Figure 38-7 shows a single line scan of this circuit that was measured every 3.2 seconds during warm-up. The peak of the top scan represents an increase of  $35^{\circ}\text{C}$  in the circuit temperature from the time power was applied. These scan lines are not normal, in that they contain a high noise signal that was induced by the cryogenic cooler. This problem has been corrected. Figure 38-8 shows the same circuit, with a line of scan that was measured every seven seconds during warm-up.

Figure 38-9 depicts the scans made of a circuit containing a crack in the silicon. The scan line labeled "initial warm-up" was made about 10 seconds after power was applied. This scan line shows a large drop in IR in the area of the crack. The scan line made after thermal stabilization shows the same condition, but less pronounced. The defect is readily detectable when initial power is applied, but less easily detected after thermal equilibrium is reached. This is a good example of the need for an instrument to scan at a fast speed and to have a fast response detector.

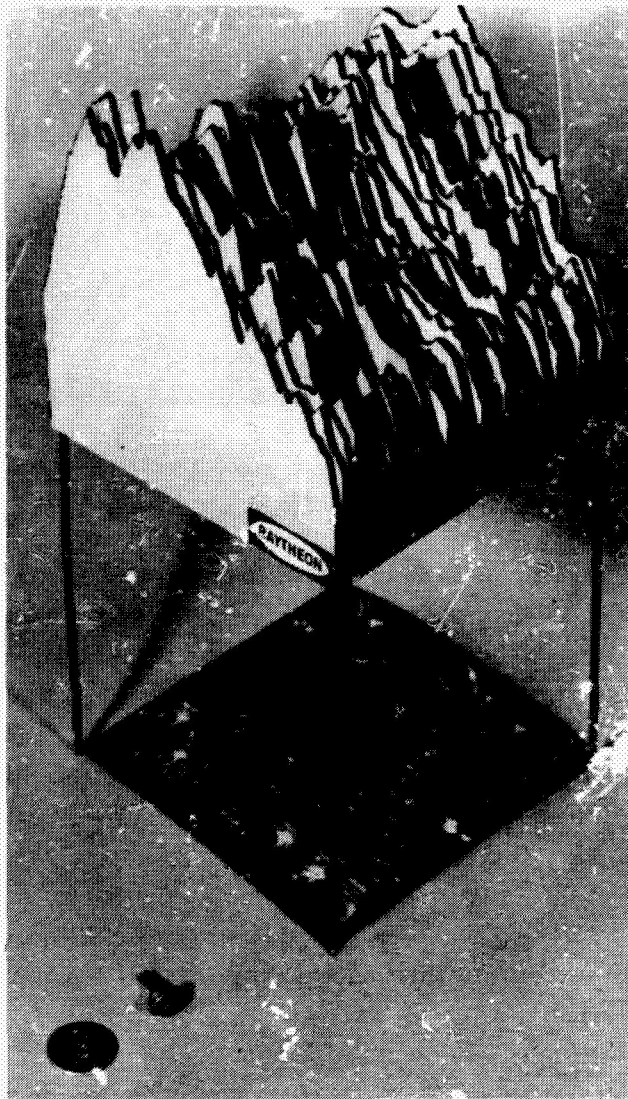


Figure 38-6—Infrared profile and photograph of microcircuit.

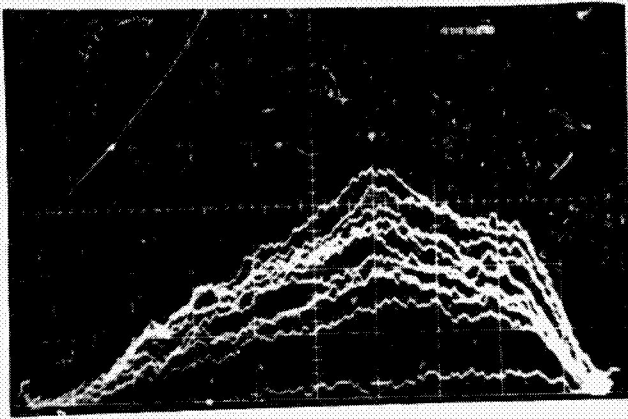


Figure 38-7—IR scan of circuit every 3.5 seconds during warm-up.

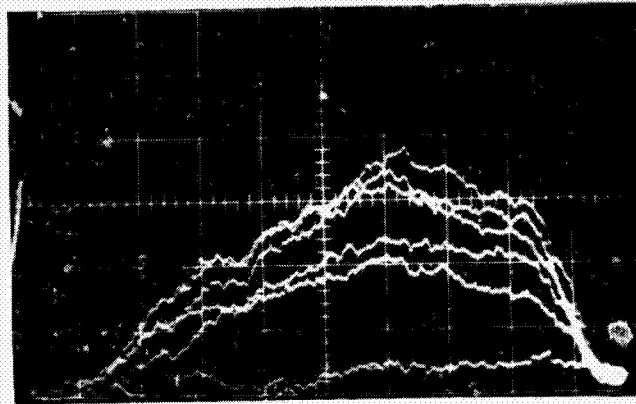


Figure 38-8—IR scan of circuit every seven seconds during warm-up.

A study is in progress to determine the ability to use infrared testing to predict the failure of a transistor because of secondary breakdown, and to show the area where the breakdown will occur. The 2N1722 power transistor used for this study is shown in Figure 38-10. The infrared profile of the transistor was measured just prior to driving it into breakdown, and was found to be uniform and normal throughout the chip. The device was then driven into secondary breakdown and measured with the infrared microscope. The infrared spike shown in Figure 38-11 was found at the point of secondary breakdown. The breakdown occurred at a small point within the 50 mil square (Figure 38-12).

It is anticipated that methods and criteria can be established to detect devices that are prone to secondary breakdown with specified power ratings.

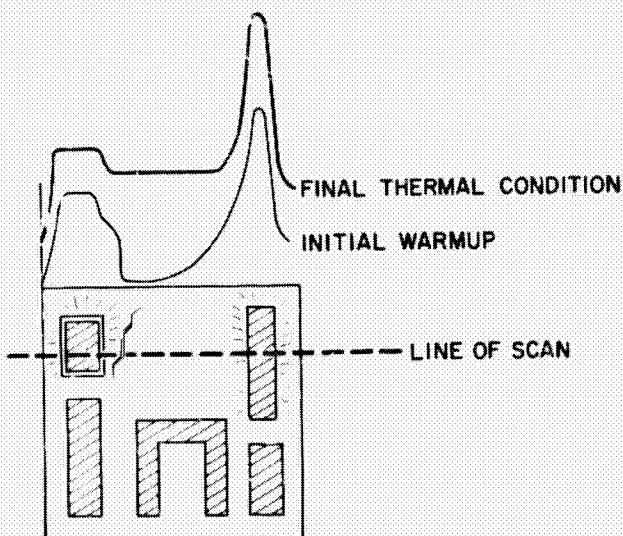


Figure 38-9—IR scan of circuit with a crack.

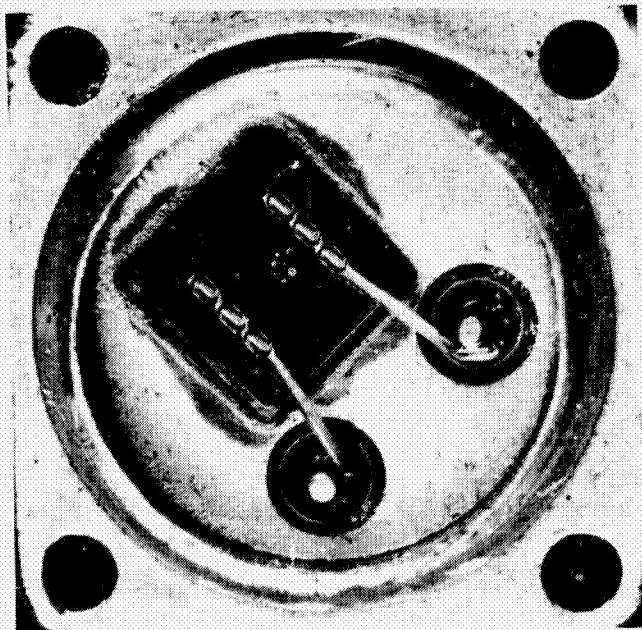


Figure 38-10—Power transistor used for secondary breakdown study.



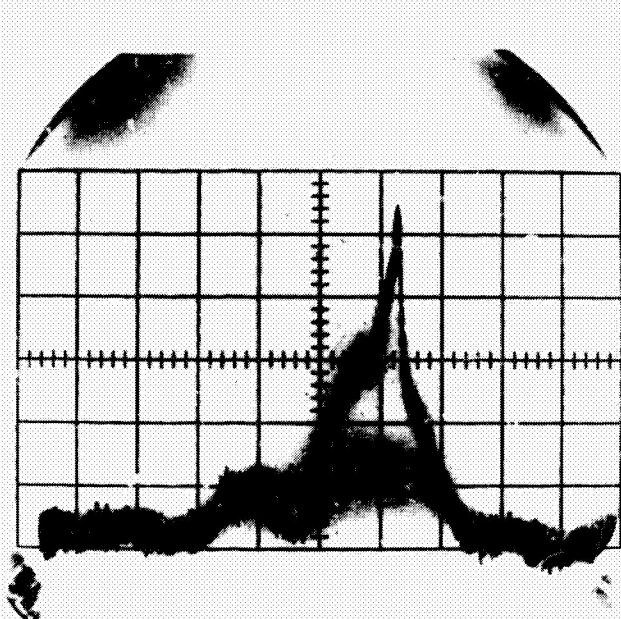


Figure 38-11—Infrared emission of secondary breakdown.

Additional work will be performed to correlate IR profiles to failure mechanisms found in microelectronic devices, so that test methods and acceptance standards can be established for these devices.

The microscope will be placed in a microelectronics manufacturer's plant, for inspection of devices on a production line prior to encapsulation. From this data, the feasibility, practicality and effectiveness of IR testing at this point can be determined.

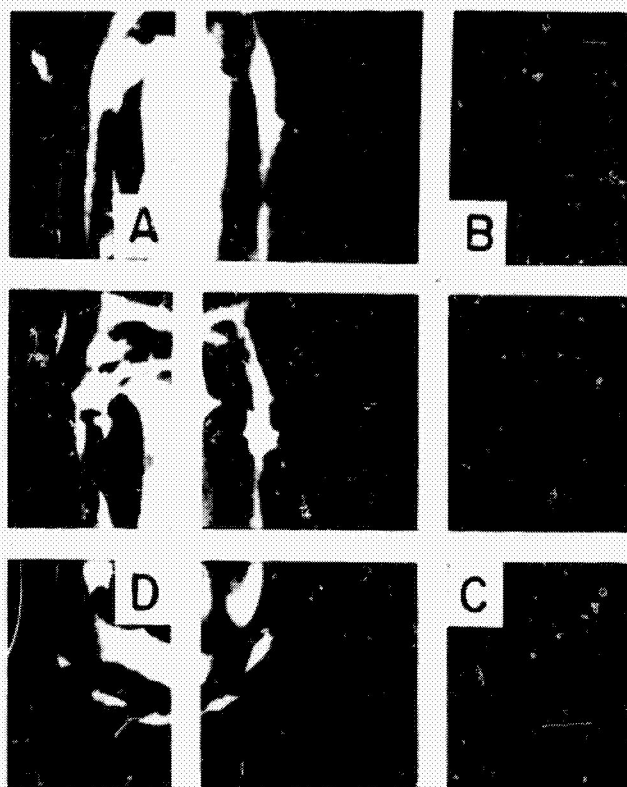


Figure 38-12—Area where secondary breakdown occurred.

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N67-31601

39. PHENOMENOLOGICAL STUDY OF RADIATION DAMAGE AND RECOVERY  
OF METAL-OXIDE FIELD EFFECT TRANSISTORS

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Data for radiation damage by 1.5 Mev electrons to several types of MOSFETs (Metal-Oxide Semiconductor Field Effect Transistors) and the results of two annealing modes are presented. In the passive mode of annealing, completed in 15 to 20 hours, the data showed significant hardening effects. The active mode of annealing yielded a quick recovery to the original threshold or better. In the passive mode of annealing, although the device was radiation hardened, the final gate threshold achieved was higher in comparison to the initial gate threshold.

It has become essential to optimize the weight, size, and power requirements of the electronic hardware for space flight use. Although significant reductions in size and weight were being achieved by conventional integrated circuit technology, insulated gate field effect devices offered the added advantage of a significant reduction in power without loss in the speed of operation. The simplicity of manufacturing insulated gate field-effect transistors was suited to integrated circuit technology. This device offers great promise for application in space electronics except for one major limitation: the electrical characteristics of the available MOS (Metal-Oxide Semiconductor) devices degrade in a radiation environment. This paper reports a study investigating radiation damage and the modes of the recovery process. This phenomenological study of recovery appears to reveal a possible model of the damage mechanism.

This investigation was completed with a limited number of samples made by different manufacturers. Only P-channel enhancement mode devices were investigated by exposing them to a 1.5 Mev electron beam. The following type of devices made by the respective manufacturers were studied:

<u>Type</u>	<u>Manufacturer</u>
SC1128	General Micro-Electronics
MEM 511	General Instrument
MM 2103	Motorola
- - - - -	Autonetics

Figure 39-1—Schematic of SC1128 configuration for irradiation study.

A similar number of MEM 511 type devices manufactured by General Instrument were also studied. The annealing process adopted was slightly different than the one used for the SC1128's. These devices were annealed in an active state in contrast to the previous passive state, where no voltages were applied to the device electrodes. The devices were heated to 280° C, and even at zero gate voltage, the unit was conducting and saturated; the  $I_{DS}$  was limited with external resistance to 100  $\mu$ a. Figure 39-4 shows the transfer characteristic of a sample unit after irradiation and annealing. It also showed a plot of drain-source current as a function of gate voltage.

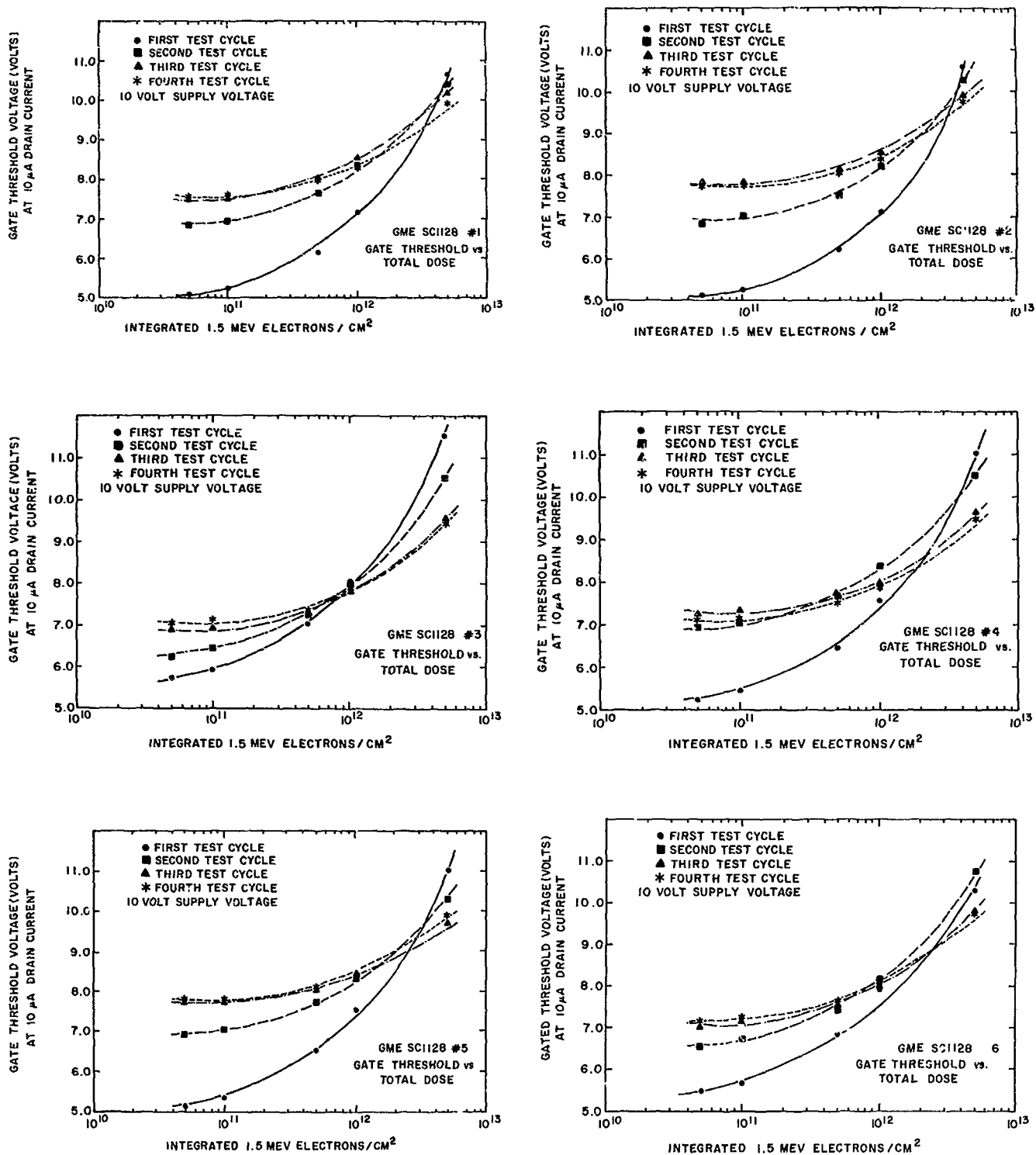


Figure 39-2—The change of gate threshold vs. total dose after repeated irradiation and annealing, for various devices.

- |     |      |        |        |
|-----|------|--------|--------|
| (a) | GM-E | SC1128 | no. 1. |
| (b) | GM-E | SC1128 | no. 2. |
| (c) | GM-E | SC1128 | no. 3. |
| (d) | GM-E | SC1128 | no. 4. |
| (e) | GM-E | SC1128 | no. 5. |
| (f) | GM-E | SC1128 | no. 6. |

A method of recovery to the nearly original gate threshold voltage was achieved within a few minutes (about five). It appeared to be caused by an interaction of current in the bulk material with trapped ions at the interface of the Si-SiO<sub>2</sub>, assuming that most of the ions generated by ionization migrate and are trapped at this interface. Unlike the SC1128's, the rate of degradation of these devices to successive irradiation after quick recovery was not consistent among all the samples. However, some of the samples did show a degree of radiation hardening. All the devices recovered to the original gate threshold or even lower values with quick recovery, and in some of the samples there was a change in the transfer characteristic curve ( $I_{DS}$  vs.  $V_{GS}$ ) after annealing.

The third type of device studied was a P-channel enhancement type MM 2103 made by Motorola. Figure 39-5 gives a plot of transfer characteristic of one of these samples after irradiation and recovery. These devices were also recovered in the active state, and all of the samples of this type showed a closer recovery to the original transfer characteristic after the quick-recovery process.

A sample of "N" channel enhancement mode device made by Motorola (Type MM 2102) was irradiated and went into the depletion mode. Since this was only one sample available for irradiation, no further investigation was conducted.

Most of the observations in this study of degradation and recovery could be explained on the basis that ions are trapped in the surface states at the interface of Si and SiO<sub>2</sub>. These ions generated by the radiation in the SiO<sub>2</sub>, migrate and become trapped in surface states. These ions are relatively immobile and counteract the field applied at the gate electrode which is attempting to form the channel. In the first mode of recovery of prolonged heating and cooling, the trapped ions are excited and allowed to recombine with carriers in the Si

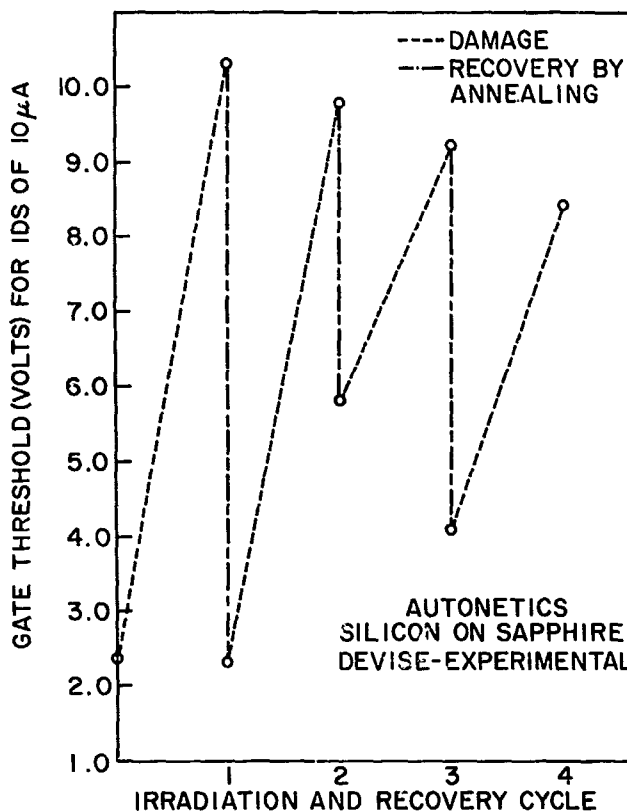


Figure 39-3—Initial and final gate threshold voltages after successive irradiation and annealing on Autonetics experimental sample.

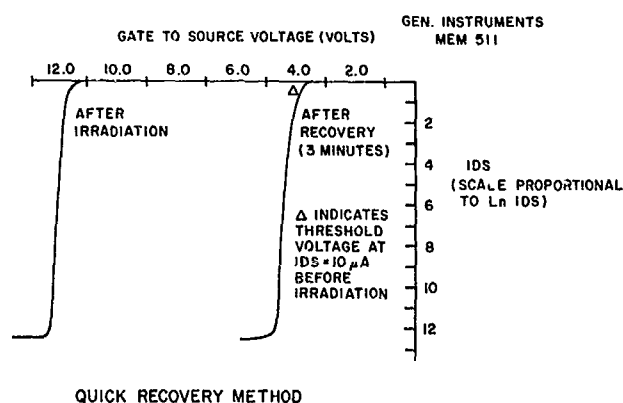


Figure 39-4—Drain current against gate voltage characteristic for General Instrument device type 551.

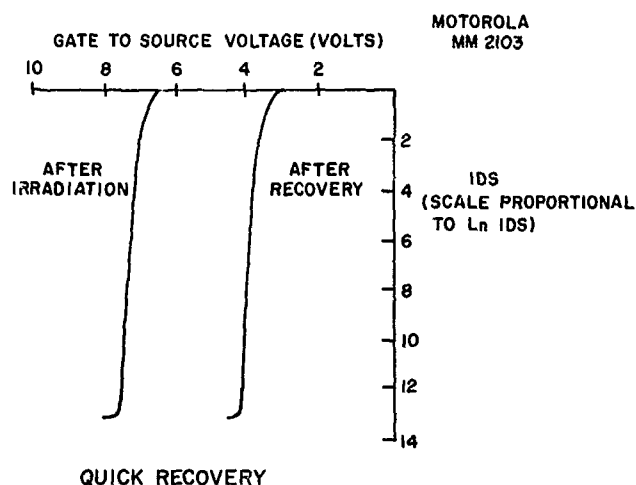


Figure 39-5—Drain current against gate voltage characteristic for Motorola MM2103.

semiconductor region. In addition to the removal of trapped ions, removal of strain at the interface (thermal annealing), appeared to occur. The heating and cooling cycles left fewer surface states and thus made the device less radiation-sensitive. In the quick-recovery mode, one has the interaction of carriers of the bulk material with the trapped ion by recombining at the interface. In this mode of recovery where heat is applied for a few minutes only, significant annealing (i.e., decrease in strain at the interface of Si-SiO<sub>2</sub>) is not achieved. The device does recover to the original characteristic, but it is not significantly radiation-hardened. Future plans are to study the effect of doping SiO<sub>2</sub> with an impurity to enable some of the generated ions to recombine with the free carriers available.

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N67-31602

40. INVESTIGATING THE POTENTIAL RELIABILITY OF INTEGRATED  
CIRCUITS FROM PARAMETER DISTRIBUTIONS

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This paper discusses distribution plots of electrical parameters as a means of investigating the potential reliability of integrated circuits. Data from the Lunar Orbiter project and various Government research programs are examined. Emphasis is placed on leakage current measurements and their conformance or nonconformance to a log normal distribution. The multiple slope log normal distribution is discussed in detail with relation to parts design, product improvements, and potential failure mechanisms. The effect of aging on integrated circuits is correlated with shifts in the electrical parameter distributions. Individual electrical parameters appear to drift almost randomly on the basic distribution curve. This phenomenon is used to show the inadequacy of present methods of power "burn-in" as a screening test. The concept is further used to describe the use of this type of data presentation in analyzing the results of environmental step-stress testing. The advantages and limitations of product-capability testing, and of incorporating this approach into a qualification program for microelectronic devices are also discussed. Attention is devoted to the stresses which appear to be the most effective indicators of integrated-circuit weaknesses.

INTRODUCTION

In an attempt to derive the maximum benefit from the plethora of electronic-parts data generated in reliability programs, it is essential to study parameter distributions. There are many types of distributions and extrapolation techniques being considered in quantitative reliability studies at this time. At Langley Research Center electronic-parts data are plotted for conformance to a normal or log normal distribution in order to perform a rapid qualitative evaluation. Though the results are qualitative, leakage current distributions for a family of integrated circuits used in a major NASA flight program appear significant enough to merit detailed discussion. The significance of this simple curve-plotting technique becomes obvious when these data are contrasted with those of an electronic-parts vendor before and after an integrated-circuit redesign. It follows that normal distributions should be equally valuable in interpreting step-stress data, and it seems

worthwhile to discuss these possibilities in light of the concept of "line qualification" presently being studied by the NASA Subcommittee on Microelectronic Parts.

### GRAPHICAL INTERPRETATION

Before actual integrated-circuit data are discussed, the proposed interpretations of the log normal plots can be described in general terms. Data are plotted on standard probability graph paper. In Figure 40-1 a theoretically perfect Gaussian distribution appears as a straight line as shown by curve A. Curve B shows a double-slope curve, and its counterpart is plotted in the standard manner. This type of curve occurs often in the analysis of data. It is important to note that the double-slope curve on probability paper does not correspond to a double population or to two individual populations. The double-slope curve does represent a unique or systematic deviation from a log normal distribution. The contention of this study is that the multiple-slope log normal distribution indicates a lack of process control or an immature part design and a potential failure mechanism.

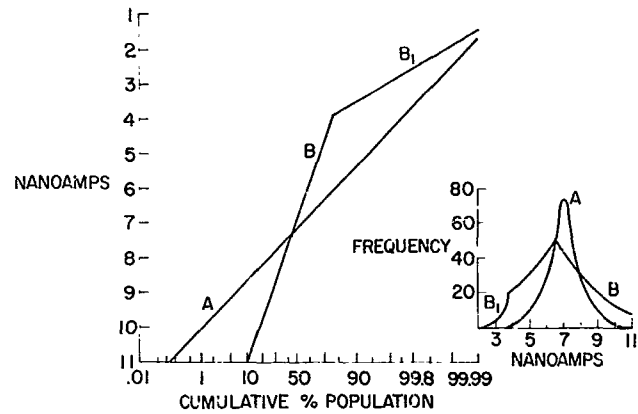


figure 40-1—Simple and double-sloped log normal distributions.

### LUNAR ORBITER INTEGRATED-CIRCUIT DATA

The integrated circuits used in the Lunar Orbiter satellite are a family of diode-transistor logic (DTL) circuits, consisting of a dual NAND gate, a flip-flop, a buffer, and an expander. Since the data to be discussed are similar for all circuits, the dual NAND gate will be taken as representative of the family. This gate is a 14-lead device in a 1/4-inch by 3/16-inch ceramic flat pack. The package outline and schematic diagram are shown in Figure 2. The measurements taken and the forcing conditions are shown in Table 40-1. Testing was performed by the Boeing Company, the prime contractor for the spacecraft.

For the purpose of this discussion, only leakage current parameters will be considered since these values were the only good indicators of device problems. This is not a surprising result since surface problems are the major cause of integrated-circuit failures at the semiconductor chip level.

The leakage current  $I_{RG}$  is presented as a log normal distribution in Figure 40-3, and the double slope is immediately obvious. Increasing leakage current is plotted downward, and thus the undesirable portion of the population is the lower segment of the line. This method is used to make the distribution of electrical parameters consistent with that of stress parameters, to be discussed subsequently. Curve A represents the initial readings, and curve B depicts the leakage

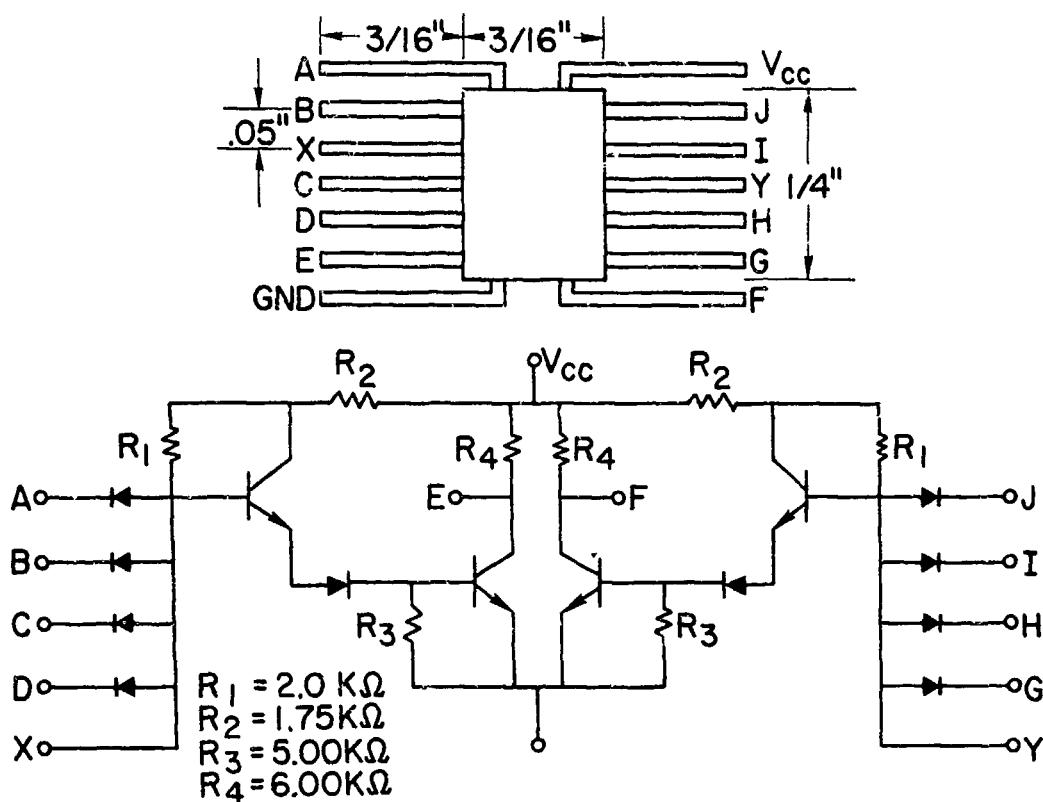


Figure 40-2—Package configuration and schematic diagram for dual NAND gate.

current distribution after 2150 hours of operation as a ring counter at ambient temperature of 125° C. The aging setup is shown in Figure 40-4.

In addition to the double slope, it is important to note the shift in the distribution after aging. It appears that the double distribution is drifting toward a single, more undesirable distribution. A larger percentage of the circuits now lies in the undesirable segment of the population, and the better segment seems to be revolving around the breakpoint to approach the undesirable segment. It is unfortunate that these distributions were not available while the devices were still under test;

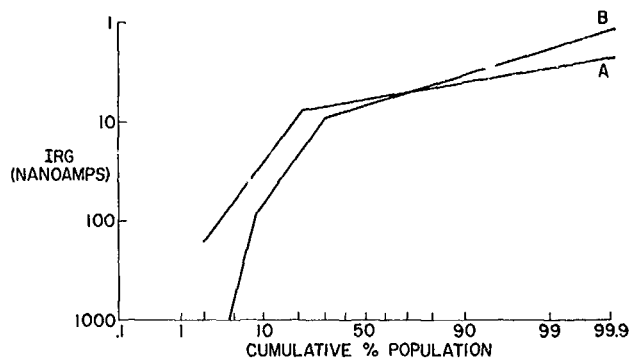


Figure 40-3—Leakage current distributions for Lunar Orbiter integrated circuits.

for the 3000-, 4000-, and 5000-hour data could have been very informative. This double-slope distribution, together with the tendency of the distribution to become degraded, gives a good preview of future problems.

Of the 197-unit test sample, five devices were actually considered leakage current degradation failures according to the reject criteria. These five drift failures can best be discussed with reference to Table 40-2, where the leakage current values for the five failures are given

FORCING CONDITIONS, CONNECTOR F. J

TEST NUMBER	SYMBOL	A	B	D	E	C	L	M	P	R	N	F	K	S	H
		DEVICE PIN													
		A	B	C	D	X	G	H	I	J	Y	E	F	V <sub>CC</sub>	GND
1	IRA	4.5'	GND	GND	GND									4.5'	GND
2	IRB	GND	4.5'	GND	GND										
3	IRC	GND	GND	4.5'	GND										
4	IRD	GND	GND	GND	4.5										
5	IRG						4.5'	GND	GND	GND					
6	IRH						GND	4.5'	GND	GND					
7	IRI						GND	GND	4.5'	GND					
8	IRJ						GND	GND	GND	4.5'					
9	IFA	GND	4.5	4.5	4.5										
10	IFB	4.5	GND	4.5	4.5										
11	IFC	4.5	4.5	GND	4.5										
12	IFD	4.5	4.5	4.5	GND										
13	IFG						GND	4.5	4.5	4.5					
14							4.5	GND	4.5	4.5					
15							4.5	4.5	GND	4.5					
16	IFJ						4.5	4.5	4.5	GND				4.5	
17	IPDN													4.5	
18	IMAX	GND					GND							4.5	
19	ISCE	GND									GND			4.5	
20	ISCF						GND					GND		4.5	

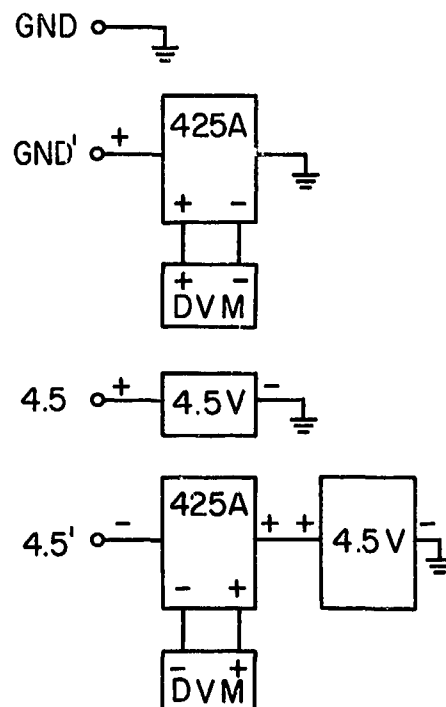


Table 40-1—Forcing conditions for leakage current measurements

for the seven test times. Leakage currents appear to drift almost randomly for the various test times, and it would be impossible to establish any theoretical model to predict this phenomenon. Of particular interest are the three circled values where units that had drifted far out of tolerance fell well back within specifications into the nanoampere region.

Erratic behavior of this type is alarming to the reliability engineer, since these uncertainties make it virtually impossible to screen out defective units. Indeed, the entire population appears to be defective. The prime contractor observed that all of these five failures could have been detected with a 250-hour burn-in, if lenient delta leakage current reject criteria were imposed. This is hardly a solution to the problem since the low readings of units 1 and 4 at 1650 hours could just as well have occurred at 250 hours.

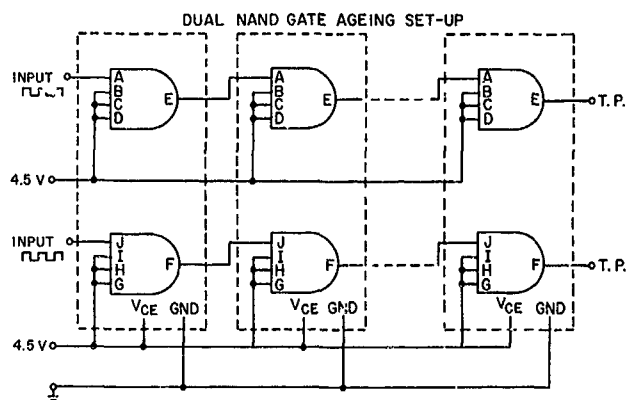


Figure 40-4—Four pairs of dual parallel strings (35 gates per dual string.)

PART NO.	IN-PUT	TEST POINT							MAX. TEST LIMIT	
		INITIAL	250 HR	550 HR	850 HR	1150 HR	1650 HR	2150 HR		
FLIP FLOP										
1 *	SI	27.13 $\mu$ A	27.24 $\mu$ A	27.49 $\mu$ A	13.06 $\mu$ A	27.72 $\mu$ A	27.83 NA	30.02 MA	2 $\mu$ A	
2 *	SI	86.44 $\mu$ A	86.79 $\mu$ A	88.27 $\mu$ A	86.32 $\mu$ A	88.00 $\mu$ A	87.96 $\mu$ A	113.7 $\mu$ A	2 $\mu$ A	
3	CP	11.68 $\mu$ A	46.12 $\mu$ A	42.05 $\mu$ A	32.95 $\mu$ A	29.49 $\mu$ A	29.83 $\mu$ A	44.00 MA	20 $\mu$ A	
DUAL NAND GATE										
4	G	5.36 NA	218.2 $\mu$ A	213.5 $\mu$ A	181.5 $\mu$ A	166.6 $\mu$ A	35.16 NA	204.9 NA	10 $\mu$ A	
5	C	3.145 $\mu$ A	9.140 $\mu$ A	62.09 $\mu$ A	61.91 $\mu$ A	59.90 $\mu$ A	48.86 $\mu$ A	1.077 MA	10 $\mu$ A	

\* THESE WERE UNITS INITIALLY OUT OF SPECIFICATION RETAINED IN THE SAMPLE FOR OBSERVATION PURPOSES

\*\*CATASTROPIC FAILURES

Table 40-2--Parameter values for leakage current failures.

The contention of the Langley reliability group is that the decision could be made from the initial log normal distribution not to use these circuits in a flight project. In addition, it appears that the distributions point out a basic flaw in the manufacturing process and no amount of screening will guarantee a reliable part from an unreliable process. In the future, these distributions will be required before any major procurement.

A surface failure mechanism is suggested from the previously discussed data, and the formation of an inversion layer or channeling was suspected from the erratic drift phenomena. Devices failing by this mechanism usually tend to recover when heated without the presence of an electric field. The five failed units were temperature baked at 200° C for 60 hours, and all tended to recover. The leakage current of three of the units dropped from the milliampere region into the low microampere region, and the leakage current of another unit dropped from 113 microamperes to 83 microamperes. Unit 4 had already mysteriously cured itself and remained within specifications. This recovering trend tends to verify the channeling hypothesis. A physics-of-failure program by the manufacturer of this integrated circuit (in no way related to this evaluation) attributed the formation of channeling in his circuits to the presence of sodium ions at the oxide-silicon interface (Reference 1).

## A SUPERIOR DESIGN

Leakage current data obtained from another vendor for a different integrated circuit, before and after a redesign, illustrate the value of the distribution in estimating the quality of a part design. This integrated circuit is not associated with any NASA flight programs, but the data from Government-sponsored research were supplied by Motorola Semiconductor Products Division. Figure 40-5 shows initial leakage current distribution for a DTL gate and distribution after 1000 hours of operation. The familiar double distribution indicating a surface instability and potential failure mechanism is again present. Also, after 1000 hours of operation the parameter degrades as seen by the larger percentage of units in the undesirable segment of the distribution. This curve is almost identical to that in Figure 40-3, and the same type of problems might well be anticipated. The vendor in an attempt to solve this problem of instability redesigned the device; the results are seen in curves C and D of Figure 40-5. Curve C conforms closely to a single log normal distribution exhibiting a considerably lower value of leakage current. In curve D, it is seen that after 1000 hours of operation, there is only a very small and easily acceptable leakage current drift. The curve remains a good normal distribution, and there is no tendency to shift to a poorer distribution.

Comparison of these curves gives a good indication of the usefulness of these distributions in dictating the choice of an integrated circuit for a major flight program. It shows that a redesign resulting in a product improvement reflects the distribution curves. The redesign of the device consisted of several changes in construction and fabrication, but probably the most significant change relative to the data just presented was the coating of the surface with a borosilicate glass over the aluminized pattern.

## STEP-STRESS TESTING

It has been shown that the log normal distribution can be used to indicate the design quality of the integrated circuit and potential reliability as far as the semiconductor surface is concerned. The same types of distribution are invaluable in describing the results of step-stress testing. In this case, a function of the stress value is plotted against the cumulative percentage of failures.

Figure 40-6 is a good example of temperature step-stress results for integrated circuits from two different vendors. Curves A, B, C, and D show improvements in a Texas Instrument design relative to temperature capability from 1962 to 1964 (Reference 2). Curve D shows

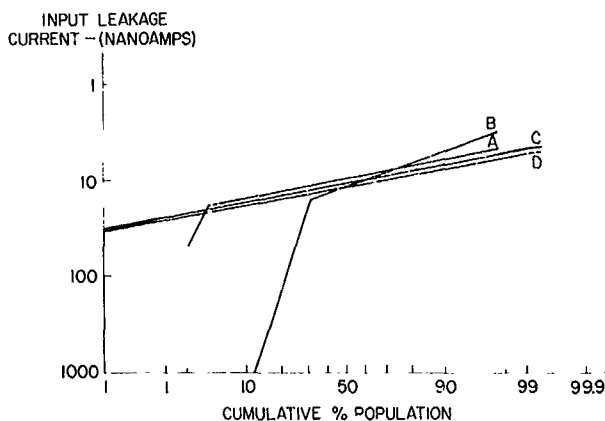


Figure 40-5—Leakage current distributions showing improved integrated-circuit design.

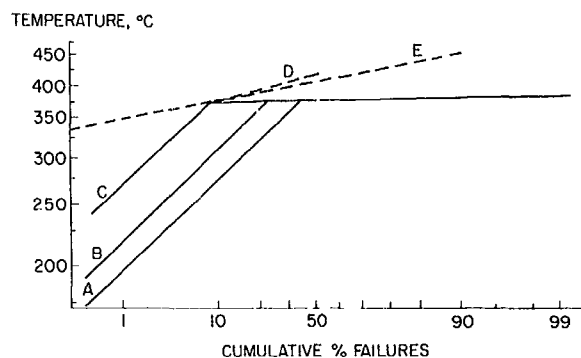


Figure 40-6—Step-stress distribution data showing improved integrated-circuit design.

a capability exceeding the 377° C silicon-gold eutectic point, which had been the limiting value for curves A, B, and C. Curve E is data recently supplied by Motorola Semiconductor Products Division. No comparison should be made between vendors since data are for different circuit functions, taken as much as 2 years apart; and it is questionable if the failure criteria are the same.

Step-stress testing coupled with distribution plots gives a good estimation of product capability. By proper choice of stress, a thorough evaluation of an integrated circuit could be performed. Centrifuge tests, for example, would be valuable in evaluating bonding and chip-to-package attachment techniques. The stresses that appear to be the best indicators of integrated-circuit weaknesses are the following: temperature (non-operating), temperature (operating), steady-state acceleration, thermal shock, and lead bend with hermeticity. Other types of stresses, such as vibration (variable frequency or fatigue), mechanical shock, temperature cycling, and humidity should not be overlooked, but the data seen thus far do not merit their being incorporated into a step-stress program.

The NASA Subcommittee on Microelectronic Parts is investigating the possibility of incorporating step-stress testing into a NASA specification for integrated circuits. Testing must be process-oriented in order to make this concept economically feasible, and devices representative of manufacturing "lines" must be defined. This definition may be the most difficult obstacle to such a program.

## CONCLUSION

Distribution plots can be a valuable method for assessing the quality and potential reliability of integrated circuits, and the use of Gaussian probability paper can contribute greater visibility to any data analysis. In particular, log normal distributions of leakage currents, wherever these currents can be measured, are excellent indicators of possible surface failure mechanisms. The same type of distribution, when used to interpret the results of step-stress testing, can be valuable in comparing part designs between vendors, establishing more effective screening tests, making possible better absolute maximum ratings for designers, and when fed back to the vendor, can possibly result in product improvements.

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N67-31603

41. A HIGH RELIABILITY SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS

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This paper traces the circumstances leading to the writing at Goddard Space Flight Center of a high reliability specification for a specific family of digital integrated circuits. This was Goddard's first specification for integrated circuits which was not basically a supplier-prepared document. Various aspects and details of the specification are discussed which are different in total or in degree from other high reliability specifications. Both tangible and intangible (human engineering) factors were considered and incorporated. Particular emphasis is placed on visual inspection criteria. Varying degrees of failure analysis are called for and have proved to be a valuable source of failure mode information. Although in-system results of units delivered to this specification are limited at this time, available results are discussed. Comparative pricing with some devices built to other specifications is given. Finally, the specification itself is included as an Appendix.

BACKGROUND

Beginning in the third quarter of 1965 and continuing through the end of the year, a significant increase in the number of in-circuit failures of Series 51 type integrated circuits occurred at the Goddard Space Flight Center (GSFC). These failures occurred in both in-house and contracted designs and hardware. Probable time of manufacture of these troublesome units was about the second quarter of 1965. Failure analyses performed on defective units showed the primary mechanisms of failure to be, in descending order of incidence, bad thermal compression bonds (at the gold-aluminum interface), cracked dice, pinholes in the silicon dioxide, and mislabeling of units (leading to "zapping" or inoperability of units). In addition, visual inspection during failure analyses indicated that production and quality assurance inspectors were lax, sometimes grossly so, in applying inspection criteria called out in the manufacturer's own specification. While some failures of indeterminate cause could not be ascribed definitely to various so-called cosmetic defects, these defects often were specifically listed as reject criteria in the procurement specification.

Radiographic pictures also indicated frequent nonconformance to specifications; devices passed which had excessive voids in the pyroceram cementing the die to the header package.

During a series of discussions with the vendor, several interesting things were disclosed. During the time that these units were manufactured, the vendor increased production by a factor of 5 to 10. At the same time, he also was moving the site of manufacture to larger, improved facilities. The resultant overall lowering of the competence of manufacturing and quality assurance (QA) personnel, due to the increase in their numbers, was particularly alarming. This naturally led GSFC to the question of the vendor's total program in training both QA and production personnel. It can be reported that a training program did exist, and not only included the mechanical training one would expect for, as an example, a bonding operation, but also considered motivation of an individual in the resultant learning process. The program did not answer the questions as to why the end product was not better. Some of these questions were answered during an on-site survey of the vendor's integrated circuit line in December, 1965.

As can be seen in GSFC Specification S-711-P1 (Appendix), 100 percent visual precap inspection is considered a major point in the processing of a high-reliability product. A visit to this station in the vendor's plant resulted in the line being closed down immediately. Out of a sample of 10 units passed by the production inspector (the units had not yet been sample inspected by QA), half of them exhibited gross defects. Some units had missing leads. Others had extra wires, "pigtailed", or loose, unattached wires. Some devices contained multiple defects. In analysis, it was concluded that the real cause for the situation was the lack of practical application of human engineering at this station. Subsequently, (some within 12 hours), the inspection platform was gimbal mounted, the lighting was improved, devices carrying trays for incoming, scrap, good, and "rework" units were color-coded, and location and physical separation in the inspection dry box was changed.

Other areas, stations, and processes considered in need of improvement were pyroceram application (its method of application, the amount and criteria for controlling), the wire bonding station, and the mesa package fabrication (its initial manufacturing, tooling, QA inspection). In addition, operator fatigue was questioned.

In view of the foregoing, it was concluded that the need for a Goddard specification was imperative. Previous high reliability specifications were essentially company written, with many inputs by GSFC; however, they were not necessarily interpreted the same way by both parties. In addition, a company-controlled specification can and has been changed without notice to the user.

This background has been presented in order to indicate factors considered by the authors at the outset of writing the GSFC specification for high reliability Series 51 digital integrated circuits. Before good engineering practices can be applied to achieve reliable systems, variables affecting component reliability must be stabilized and controlled. Any specification developed

should (and this one attempts to) assure against known and recognizable potential failure modes. This includes the minimization of human-induced failures.

## SPECIFICATION DEVELOPMENT

The basis for GSFC Specification S-711-P1 was a document already started under a low-priority effort, which contained many of the standard "boiler plate" requirements. The next step was to study device procurement specifications already in use by Goddard, Jet Propulsion Lab, Marshall Space Flight Center, and Autonetics, Minuteman Division. These documents were reviewed with respect to Goddard requirements and their ability to overcome the problems discovered through the failure analysis effort mentioned previously.

In late 1965, during the period of alarm at the increase in numbers of failures, through discussions with the vendor, GSFC learned that, during the past year, Minuteman devices had been fabricated by the vendor using a gold wire-to-gold/molybdenum metallization bonding system. The vendor proposed substituting this system for the gold wire-to-aluminum metallization system used on all versions of Series 51 devices. A subsequent visit to Autonetics, entailing discussions and data study, indeed indicated that the all gold system was superior. Whereas aluminum-gold system lots had had a reject rate of one out of three, 45 consecutive lots with the gold-gold/molybdenum system had been accepted by Autonetics. The vendor indicated that they would continue with the aluminum-gold system on special order, but since the formation of aluminum-gold eutectics was found to be GSFC's most frequently occurring device failure mechanism, the all gold system was selected. This is reflected in the specification, particularly in that section dealing with pre-cap visual inspection and reject criteria.

Specification S-711-P1 represents extensive and concerted efforts on parts of the vendor and the authors to develop a meaningful high-reliability specification. Problems encountered during the discussions were usually not of the stimulating type. Semantics were critical. Negotiations on critical sections were often tedious, but essential. The problem was to determine the degree of fact or fiction in vendor statements, while realistically evaluating Goddard requirements for safeguards.

For example, in previous specifications, a major point of disagreement had always been the reject criteria applicable to scratching the aluminum metallization. Figure 41-1 shows a photo of a scratch across an aluminum interconnect. This and similar scratches are tooling marks caused by lateral movement of microcircuit test probes, tweezers, vacuum chucks, or other test and handling tools. Scratches can also be caused by dice rubbing against each other following or during wafer scribing, breaking, or rinsing. The problem here is that an indeterminate amount of aluminum has been removed. Determination of the depth of such a scratch unfortunately is very difficult even under optimum laboratory conditions of magnification, lighting, and viewing angle. Such determination is virtually impossible on a production line. In specifications referenced in

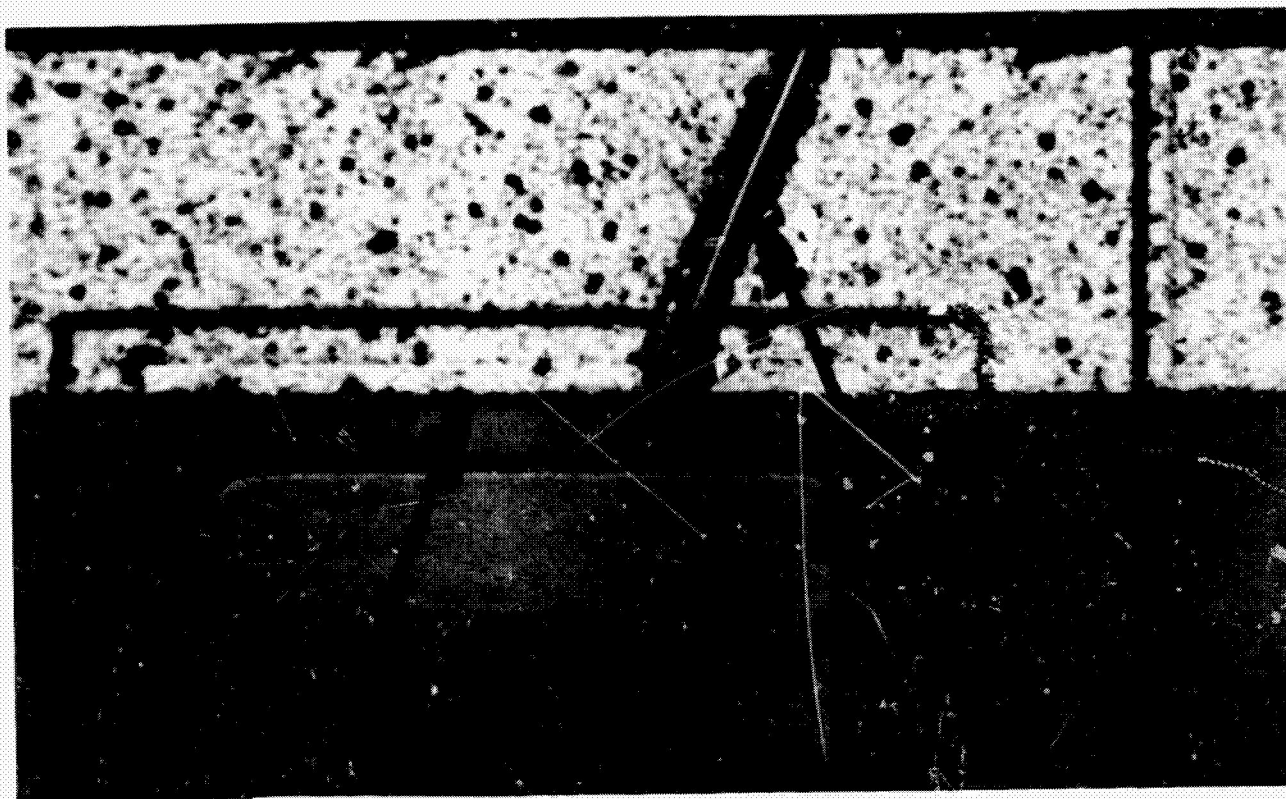


Figure 41-1—Scratch on aluminum interconnect.

procurements prior to the issue of this one, one of the scratch criteria for device rejection reads: "Scratching in metallization which cuts through more than 50% of lead width". Figure 41-2A shows in section a drawing of a scratch whose bottom is just below the top of the interconnect deposition height. Very little aluminum has been removed, and no danger exists of the interconnect opening due to high current concentration at this point. In Figure 41-2B, the bottom of the scratch is almost at the oxide and a good possibility exists that the interconnect could open. Yet both are acceptable under the above criterion. Qualification of the criterion to reject scratches of more than a specified depth is impossible since an inspector, viewing them from above, could not distinguish between them. Another benefit (other than the elimination of gold-aluminum eutectic formations) accrues in this scratch problem if the all-gold

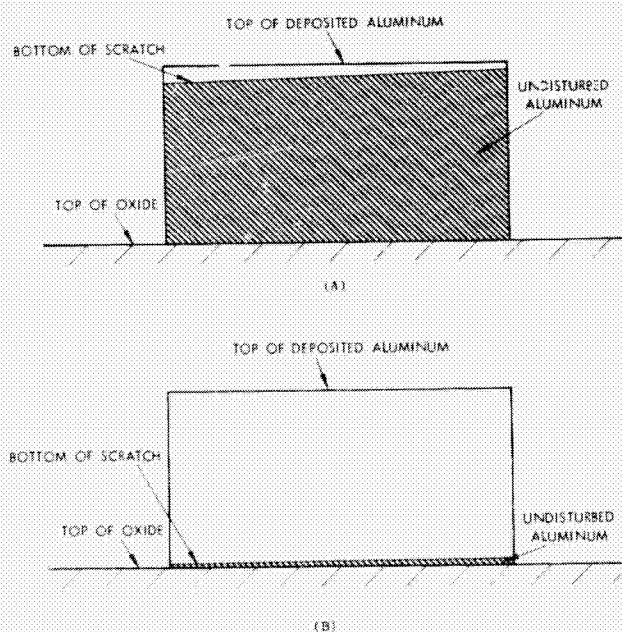


Figure 41-2—Scratch depth examples.

system is used. Under the gold is a layer of molybdenum, which is very hard to scratch, and whose thickness is more than sufficient to carry any currents consistent with device characterization. Thus S-711-P1 calls for rejection if more than half of the gold has been removed. This guarantees a minimum of one-half the molybdenum being present. This criterion would not apply to another process or to the use of aluminum by a vendor. Rewording would be necessary in these cases.

## SPECIFICATION HIGHPOINTS

The specification developed by GSFC in the first part of 1966 for the procurement of Series 51 type integrated circuits is found in the Appendix. It contains most of the standard paragraphs to be found in any electronic component specification, and little or no further comment will be made on those sections. Some of the paragraphs, however, are at least partially new, and are worthy of comment.

Traceability is one of the first requirements cited in order to aid in determining cause of failure on the ground or in orbit.

Intangible factors can have a major effect on device quality, yet are extremely hard to write into a specification. Final device reliability is affected sometimes by machines, but usually by people. This effect begins with material preparation, and continues through diffusion, fabrication, measuring, testing, packing, and shipping. Since device characteristics are determined at diffusion, succeeding steps at the vendor's plant serve to enable its use and then to attempt to weed out the few faults native to the material and those many faults induced by the actions of the very imperfect human element working on it. Operator attitude, training, fatigue, and motivation profoundly affect device reliability and cost. This nebulous area is the major portion of the paragraph entitled "Product Assurance," which requires the manufacturer to:

1. Acquaint all personnel with the intended end use of circuits delivered to the specification.
2. Emphasize utmost care in all phases of manufacturing, testing, and handling circuits.
3. Conduct quality-oriented training programs.
4. Select personnel with superior capabilities for bonding and visual inspection operations.

In addition to handling intangible factors, this paragraph also places severe restrictions on rework of devices and calls for notifying GSFC of process changes.

"Inspections and tests" comprise the bulk of the specification, and the sequence of these, which was mutually acceptable to the vendor and GSFC, is shown in the following flow diagram:

BAR INSPECTION → CIRCUIT INSPECTION → AND → FINAL INSPECTION → FORMATION → MARKING →  
 (4.3.1) (4.3.2) (4.3.3) (4.3.4) (4.3.5) (4.3.6)

FINE GROSS ELECTRICAL HIGH TEMP.  
 LEAK → LEAK → TEST I → X-RAY → TEMP. → CYCLING → CENTRIFUGE →  
 TEST (4.3.6.1) (4.3.6.2) (4.3.6.3) (4.3.6.4) (4.3.6.5) (4.3.6.6) (4.3.6.7)

ELECTRICAL JNMONITORED MONITORED ELECTRICAL ELECTRICAL  
 TEST II → VIBRATION → VIBRATION → TEST III → BURN-IN → TEST IV →  
 (4.3.6.8) (4.3.6.9) (4.3.6.10) (4.3.6.11) (4.3.6.12) (4.3.6.13)

ELECTRICAL LEAD LEAK → FINE GROSS ELECTRICAL ELECTRICAL  
 TEST V → SHEAR → LEAK → LEAK → TEST VI → INSPECTION → SHIP  
 (4.3.6.14) (4.3.6.15) (4.3.6.16) (4.3.6.17) (4.3.6.18) (4.3.6.19)

These 100 percent processing steps for the devices fall into the general categories of in-process inspection, environmental tests, electrical tests, and final inspection.

Under in-process inspection, great emphasis is placed on visual inspections to detect deficient workmanship or processing steps. Magnification values of 40 X and 100 X are specified at inspection stations at the die, circuit, and pre-cap points. The environmental and electrical tests and the final inspection will not be discussed in detail here; though they include some deviation from the norm, they are intended, as are all such tests, to weed out unacceptable devices and to maintain traceability.

The next salient feature of the specification is the paragraph titled ' Lot Shrinkage Analysis'. This requirement was inserted into the document to alert GSFC to possible delivery delays, trouble spots on the line, and potential device failures, while forcing the vendor to look at his own product yield (possibly sooner than he might) and to decrease his corrective action feedback time. Table 41-1 lists the tests at which analyses are to be performed and the level of analysis appropriate to each station. Table 41-2 (and Section 4.3.8, Appendix) defines the different levels. Note that Level I calls for category designation and count per category. Level II includes Level I plus electrical operational tests and case leakage tests prior to device opening, in order to verify failure. After decapping, visual inspection is made only on defective units. Level III was designated an optional requirement, at additional cost, because of the high cost (\$200 or more) of performing a full failure analysis. If full failure analysis were required,

Table 41-1

Lot Shrinkage Analysis

Test	Analysis Level
X-Ray	I
Electrical Test II	II
Monitored Vibration	II
Electrical Test III	II *
Electrical Test IV	II *
Electrical Test V	II *
Fine Leak Test	I
Gross Leak Test	I
Electrical Test VI	II *
Supplemental Tests	III

\* Or III at vendor option or at NASA direction. For bidding purposes, the cost of performing a formal failure analysis at this point shall not be included in the unit cost.

Table 41-2

Levels of Lot Shrinkage Analysis

- I -- Record all failures by category and number per category.
- II -- Perform I plus a cursory Failure Analysis, which shall include:
  - a) Verification of failure on all pieces, including performance of normal electrical operational tests and lead-to-lead and lead-to-case continuity tests.
  - b) Opening of a prescribed number of devices for visual inspection only under appropriate magnification (40X to 200X). For quantities of failed devices of less than 30, open a minimum of 3 devices; for more than 30 failures, open 10 percent.
- III -- Perform I plus a formal, documented Failure Analysis.

cost of any particular order might vary considerably if failures on a given run were unusually high or low. It is certain that if Level III were mandatory in the specification (as Levels I and II are), the vendor would insure that he would not stand a loss by pricing which anticipated a high loss. The method called for here still provides for a full analysis when determined necessary by either the vendor or GSFC, while allowing the vendor to price his bid realistically. It should be noted that Amendment I to S-711-P1 includes modifications to this paragraph which detail how the requirement is to be implemented.

The last comment on the specification itself concerns the paragraph on supplemental tests. As now worded, this paragraph does not require so-called destructive (hot), or Group B testing of units which are from the same diffusion run and processing as those delivered on a specific order. This requirement is extremely desirable, though the additional time (usually 1100 or 1200 hours minimum) necessary for such qualification may be a deterring factor, as it was when this specification was written.

## PRODUCTION RESULTS

Each week, the vendor is required to report, for each "lot", the number of units lost at each test station. Since at this time, processing and records are not complete on a batch of units started in March of this year, precise figures cannot be quoted. However, a sufficient number of devices have been processed and delivered to allow testing for significant points. Over 17,000 capped units were X-rayed, and rejected units were categorized as follows: extraneous matter, defective leads, defective welds, physical damage, inadequate clearance, deformed whisker, misaligned mount, voids (in pyroceram), and nonhomogeneous. The group with the highest incidence was the



first — extraneous matter. While this might be alarming in view of the pre-cap visual inspections, one must remember that the X-ray picture will not tell whether a particle is inside or outside a device, it cannot always differentiate between a mound of pyroceram and a contaminant, etc. Opening of several units rejected due to inclusion of "extraneous" matter disclosed no loose wires or metallic particles. Seventy-six percent of rejected units at X-ray were in this group, while inadequate clearance and voids tied for second, with about 9 percent each. Total rejects at the X-ray station amounted to 4.2 percent of the 17,000 pieces.

Data and percentages at the rest of the lot shrinkage stations are based on about 6800 units out of the 17,000. Except at Electrical Tests V and VI, losses at most stations ran between 0.2 and 0.6 percent. Note that Electrical Test V is not the second (post burn-in) variables data record station, where a high number of rejects was expected. Electrical Test IV is this station, and here the reject rate was an amazing one-half of one percent. In midyear of 1965 (and before), device stability had been a significant problem, and thus the specification states that if more than 25 percent of the units fail to pass the variables test, the lot shall be rejected.

The next highest reject stations were at Electrical Tests V and VI, which had 1.8 and 1.7 percent, respectively. Visual examination (Level II analysis) revealed that the defect noted most often was cracked dice. Sixty percent of the units opened at these stations were in this category. Other defects noted at these two stations were "zotted" leads (11 percent), oxide defects (9 percent), lead touching the die (9 percent), faulty masking or deposition (9 percent), and loose gold particle (2 percent - 1 unit). Cracked dice were also noticed at other stations, but were a much smaller percentages of the noticeable defects. Electrical Test V had about twice as many cracked dice as did Electrical Tests III and IV, but Electrical Test VI had the most, with two and one-half times as many as V.

As yet, the cause for the predominance of this defect has not been ascertained. A year ago, the vendor inferred that GSFC handling and package opening techniques were grossly suspect and were the probable cause of the high number of cracked dice detected by GSFC. The data here referenced certainly indicate that this may not have been the sole reason. The written requirements for lot shrinkage analysis in the specification has thus proved to be quite valuable. The vendor has reacted to this defect and is currently attempting to pin-point the trouble. His tests have included environmental and mechanical stressing, both static and dynamic. This includes temperature cycling, temperature soak, thermal shock, mechanical shock, vibration, and bending moment tests. In his test program, no failures could be induced by the environmental stressing or the "normal" mechanical stressing. The bending moment tests certainly were expected to crack the dice, and they did. These tests were made because, as was noted above, most of the cracked dice were detected at Electrical Test VI. This test follows shear-out of the device from its processing carrier and final leak testing. The bending tests are a start in simulating forces and conditions which might cause the dice to crack. At this time, no specific station has been labeled the culprit. It must also be noted that failure analysis personnel at Goddard have started work on this problem, but here also, it is too early for any conclusions to be drawn.

Although not required by the specification or contract, the vendor also reported the number of units failing at final (external) visual inspection. So far (based on the first 6800 units), this station has the highest number of rejects; 5.5 percent of the units are discarded here. This is more than twice the number of X-ray rejects and three times as many failures as at Electrical Test V. No defect categorization information is yet available.

## DELIVERED UNITS

From May, 1966, to this date, about 5600 pieces produced in accordance with this specification have been delivered to GSFC. Fabrication into flight systems has started. At this time, no failures in systems have been reported. A very small number have been rejected for use on the Radio Astronomy Explorer satellite encoder during incoming screening. Performance on these few was marginal at temperature and/or loading limits. Since no failures have been reported, it was decided to examine accepted units. Fifteen pieces of the type SN4411 (513 reference), were furnished to the Goddard Failure Analysis Section. X-ray pictures were taken, and electrical tests and fine leak tests were conducted on the units prior to opening. No units were found to be "leakers", and all 15 performed within electrical specifications. The X-ray pictures showed some slight misalignment of the die in the packages, but nothing outside specification limits. Following this activity, all 15 units were decapped, and visual inspection at magnifications up to 400X were performed. Some defects were noted; these were due primarily to tooling marks. These included depressions and drag marks due to microprobe use. In addition, there were some other "scratches" due to tweezers, vacuum chucks or (presumably) contact with the edge of another die during the washing operation following wafer scribe and break. It is important to note again that a gold "scratch" differs from a scratch through aluminum. The latter is very soft and can be easily smeared by a tool onto the adjacent oxide. A tool touching a gold metallization pushes it to either side, forming ridges in the gold, but will not make it smear onto or adhere to the oxide. There were, in addition, scattered cosmetic defects, such as spots of photoresist, slight rippling of the oxide, darkened gold spots, and paper scratches on the metallization. The last-mentioned defect is the imprint of fibers in the paper on photoresist when it is wet. The imprint is in turn transferred to the metallization. Comments on these units were generally in a non-critical category, and the units are markedly better in appearance than devices of a year ago.

## COST

A major point not yet discussed is that of price. The authors do not subscribe to the idea of instituting a requirement regardless of cost. For an individual test or criterion, the end purpose, its degree of worth (i.e., how much the reliability of the devices is influenced), and its cost were all considered. Price is of course dependent on quantity. The prices quoted below are for a 5000-piece category, since that was an initial order and these are the only figures available at this time. The basic commercial unit varies in price from \$12.80 to \$17.85 (for a gate to a flip-flop), with an average price of \$15.32. The vendor also markets the line to its own screening specification, which

includes temperature cycling, centrifuge, leak test, and burn-in, and charges an additional \$4 per unit. In 1965, GSFC and some of its contractors had been paying an average price of approximately \$33 for units built to the vendor NAS-51, or high-reliability, specification. Units built to the S-711-P1 specification have an average price of about \$41.50 (\$37 for gates to \$46 for flip-flops) and thus are not substantially higher, considering the protection afforded the procuring activity.

## CONCLUSIONS

As state-of-the-art continues its rapid advance, and the use of integrated circuits continues to rise, the need for meaningful specifications will also grow, both for new specifications for new devices and for frequent updating of existing specifications. While the area of specification writing is generally held in very low esteem by most engineers, it is in fact a task which, if properly and adequately performed, will do much to minimize failures in systems. Engineering judgment and competence in device technology, processes, and testing is no less a requirement here than in circuit design, failure analysis, system design, or analytical studies. What the integrated circuit area presently lacks but demands, is more concerted efforts of both producers and users to achieve an end product worthy of high confidence. Development of the specification discussed here is considered a first step for Goddard Space Flight Center in this direction.

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APPENDIX

GENERAL SPECIFICATION FOR MICROELECTRONIC

CIRCUITS, DIGITAL, SILICON, MONOLITHIC; AND

AMENDMENT NO. 1

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GSFC S-711-P1  
AMENDMENT 1

May 9, 1966

**MICROELECTRONIC CIRCUITS,  
DIGITAL, SILICON, MONOLITHIC,  
GENERAL SPECIFICATION FOR**

- Page 486, Par. 2.4(c) Add to last sentence, "2.2 and 2.3".
- Page 488, Par. 3.7.1 To first sentence add,  
"or in the TI package designated Type 4A".  
Add also  
"If devices are supplied in the type 4A package the contractor shall:
- (a) Submit statistical data indicating for the 4A package's header lead bonding pad to weld ring top dimension the mean value and the standard deviation.
  - (b) Run vibration tests on a number of new chips in the 4A package to test lead-to-lead and lead-to-case isolation. The tests should be designed to determine the adequacy of the bonding pad to lid clearance, interaction (if any) of bonding wires and glass frit on the lid, and should be a dynamic (i.e., monitor electrical isolation under vibration) test. Vibration schedules will be agreed on, and may be representative of various launch vehicles."
- Page 489, Par. 3.9.2 Notification time is changed from 48 hours to 5 working days.
- Page 490, Par. 4.3.1(d) There are 2 sections numbered (3). Delete in its entirety the second section numbered (3). Add a fifth section numbered (5) which shall read, "Scratches which completely remove the gold for more than 50% of the design lead width."

Page 491, Par. 4.3.2(b)(4)	Add — Except overhang onto the interconnect pattern from the bonding pad is permissible within the conditions of (3).
Page 491, Par. 4.3.2(d)	Add at the end the sentence, "Removal of particles is allowed, but the pieces shall subsequently be subject to recleaning and reinspection."
Page 491, Par. 4.3.2(e)	Delete "Presence anywhere" and substitute, "Excessive material . . ."
Page 491, Par. 4.3.2(f)(1)	Add the word, "Excessive" before the word "blistering". Delete the word "scratching".
Page 492, Par. 4.3.4.2(f)	Add at the end the sentence, "Removal of particles is allowed, but the pieces shall subsequently be subject to recleaning and reinspection."
Page 493, Par. 4.3.4.2(g)	This requirement applies only to TI's 4A package.
Page 493, Par. 4.3.4.2(h)	The 80% of bar periphery to have a glass fillet requirement does <u>not</u> apply to the 70 by 200 mil (large geometry) bar, but does apply to the new (small geometry) bars. (There is <u>no</u> fillet requirement for the large geometry bar.)
Page 493, Par. 4.3.5.1(2)	"Significantly differing production processes" refers to processes or material affecting basic electrical characteristics, such as starting material resistivity, doping levels, diffusion time and diffusion temperature.
Page 493, Par. 4.3.6 & Fig. 1	Device marking may be moved in sequence from immediately preceding the first fine leak test (4.3.6.1) to follow electrical test I (4.3.6.3) (a go-no go test) and precede . . . ray (4.3.6.4).
Page 493, Par. 4.3.6.2	Hot ethylene glycol will be used as the gross leak test (full test details in the product processing plan).
Page 494, Par. 4.3.6.3.1	Delete ". . . at +25° C and at -55° C and +125° C.
Page 494, Par. 4.3.6.3.1(a)	In lines 3 and 4, delete ". . . be guaranteed to . . ."  In line 5 delete ". . . guaranteed not to trigger . . ." and substitute ". . . shall not toggle . . ."



Under listed measurement conditions, add:

$$T_a = + 25^{\circ} \text{C}$$

Page 494, Par. 4.3.6.3.1(b)

In line 3, delete "... is guaranteed not to ... ." and substitute "... shall not ... .".

Add at the end "Measurement temperatures shall be  $-55^{\circ} \text{C}$  for  $V_{on}$  and  $+125^{\circ} \text{C}$  for  $V_{off}$ ."

Page 494, Par. 4.3.6.3.2

The test conditions should be changed as follows:

Change Q and  $\bar{Q}$  - 1 ac load

To Q or  $\bar{Q}$  - 1 ac load

Page 495, Par. 4.3.6.5

Insert the words "for a minimum of" before 48 hours.

Page 498, Par. 4.3.6.15

Add the sentence, "If lead forming is required by a specific contract, this operation shall be performed at this point in the flow process."

Page 499, Par. 4.3.6.19

All visual tests are not to be performed at 20X. Part shall be done at 3X and some kept at 20X. The following applies.:

(1) At 3X

- . All of (a)
- . Dented lids of (b)
- . All of (c)
- . All of (e)
- . All of (f)

(2) At 20X

- . Misalignment of lids (weld bead)
- . All of (d)

Page 499, Par. 4.3.6.19(d)

Delete the phrase "... in excess of 25% of the smallest lead dimension ... .", and substitute "... which exposes base material (F-15) ... ." (The gold plating on the F-15 is much less than 25% of the lead thickness.)

Page 499, Par. 4.3.7

The requirement for this paragraph is waived. Instead the contractor may submit data from his standard add-to program (for reliability evaluation), which includes the Table 2 (and other) tests.

Page 502, Par. 4.3.8.2.2

Should be corrected to read 4.3.8.1.2

Page 502, Par. 4.3.8.1.2

Delete ". . . within two weeks of the date that the defect occurred . . ." and substitute ". . . within two weeks after TI or GSFC decision to make a formal failure analysis . . ."

Page 502, Par. 4.3.8.2

Periodic Review of Lot Shrinkage

The procedures for implementing the requirement of this paragraph are as follows:

A. Reporting (Internal)

1. Station by station reporting basis
2. Cumulative weekly lot shrinkage
3. Reporting cannot group different lot date codes
4. No significant ECN\* allowed within a lot date code; a lot with different basic electrical characteristics must have a different lot date code.

B. Analysis

1. By station by calendar week
2. a. Sample size for a week may be determined by adding different LDC's if no significant ECN's have been implemented during LDC times.

Example: (No ECN's)	LDC	# Rejects	Samples/Lot
	610	10	?
	611	40	?
	612	50	?
		<u>100</u>	

\*Significant ECN is defined as ECN's affecting basic electrical characteristics, such as starting material resistivity, doping levels, diffusion time and diffusion temperature.

Requirement of 4.3.8.1 11B shall apply, with distribution of samples from each LDC being proportional to # Rejects per LDC. (In above example 1, 4, 5, pieces are the number of samples from lots 610, 11, 12, respectively.)

- b. Lots cannot be added if significant ECN's have been implemented.

Example:	LDC	# Rejects	Samples/Lot
ECN Implemented	610	10	?
	611	40	?
	612	50	?
		<u>100</u>	

Proportional sampling may be used if there are no intervening significant ECN's. In the above example this means sample three pieces from LDC 610 and add LDC's 611 and 612 to sample four and five (10%) from 611, 612, respectively.

#### C. Reporting (to GSFC)

Review report for level II shall occur two weeks after the production week under review. NASA/GSFC must respond one week after review report (three weeks after production week) to advise if level III will be required of any failed unit.

TI's "Mechpackette" is designated as being an acceptable substitute.

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S-711-P1  
January 18, 1966

APPENDIX

GSFC SPECIFICATION

MICROELECTRONIC CIRCUITS,  
DIGITAL, SILICON, MONOLITHIC,  
GENERAL SPECIFICATION FOR

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

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S-711-P1  
January 18, 1966

**MICROELECTRONIC CIRCUITS,  
DIGITAL, SILICON, MONOLITHIC,  
GENERAL SPECIFICATION FOR**

**1. SCOPE**

This specification covers the minimum general requirements for a compatible set of digital, silicon, monolithic microelectronic circuits. Specific requirements for a particular type of microelectronic circuit are listed in the applicable detail specification.

**2. APPLICABLE DOCUMENTS**

The following documents, of the issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

- 2.1 STANDARDS. MILITARY MIL-STD-750 — Test Methods for Semiconductor Devices.
- 2.2 SPECIFICATIONS. MILITARY MIL-S-19500 — Semiconductor Devices, General Specification For (Copies of military documents required by suppliers in connection with specific procurements should be obtained from the Naval Supply Depot, 5801 Tabor Ave., Philadelphia, Pennsylvania.)
- 2.3 PUBLICATIONS. NASA NPC-200-3 — Inspection System Provisions for Suppliers of Space Materials, Parts, Components, and Services.
- 2.4 DOCUMENT PRECEDENCE. For purposes of interpretation, in case of any conflicts, the following order of document precedence shall apply:
  - (a) Purchase Order or Contract. The purchase order or contract shall have precedence over any referenced document.
  - (b) Detail Specification. The detail specification shall have precedence over this general specification.

- (c) General Specification. This specification shall have precedence over all documents listed in 2.1, 2.2 and 2.3.

### 3. REQUIREMENTS

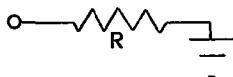
3.1 GENERAL. The individual microelectronic circuit requirements shall be as specified herein and in the applicable detail specification.

3.2 DEFINITIONS, ABBREVIATIONS, AND SYMBOLS. The definitions, abbreviations, and symbols used in this and the detail specifications are given below.

3.2.1 Switching times. The switching times and other AC parameters are defined in the detail specifications.

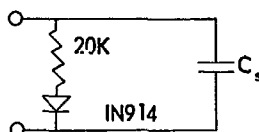
3.2.2 Unit logic load. One unit logic load is equivalent to a single logic input of any circuit described in the detail specifications.

3.2.3 DC test load equivalents. Equivalent worst case loading combinations for DC voltage tests are defined as single resistors having the following values:



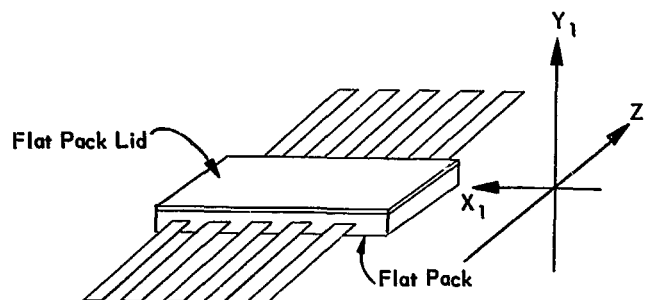
Loading	Resistance Value R ( $\pm 1\%$ )			
	$V_{cc} = +3.0$ VDC		$V_{cc} = +6.0$ VDC	
	$T_A = +125^\circ\text{C}$	$T_A = -55^\circ\text{C}$	$T_A = +125^\circ\text{C}$	$T_A = -55^\circ\text{C}$
N = 4	10.2 K	4.76 K	8.27 K	3.47 K
N = 5	8.16 K	3.81 K	6.62 K	2.78 K
N = 20	1.79 K	0.953 K	1.44 K	0.594 K
N = 25	1.35 K	0.763 K	1.16 K	0.475 K

3.2.4 Switching time test load equivalent. The typical equivalent load for use in the  $+25^\circ\text{C}$  switching time tests is defined as the following circuit:



NOTE:  $C_s$  is selected so that the total capacitance of the test fixture, connectors, scope probe plus  $C_s$  aggregates 50 pf. Exception:  $C_s = 2500$  pf for the Clock Driver Circuit (SN517 or equal)

**3.3 MICROELECTRONIC CIRCUIT ORIENTATION.** Circuit orientation shall be as shown below.



**3.4 ELECTRICAL PERFORMANCE.** The dynamic and steady-state electrical performance requirements of individual microelectronic circuits along with maximum ratings are specified in the detail specifications.

**3.4.1 Compatibility.** Input-output impedances, switching times, and voltage shall be compatible for all individual circuits such that any one circuit output shall be capable of driving the inputs of any combination of other circuits as described in the Fan-Out provisions of the detail specifications.

**3.5 MATERIALS.** Microelectronic circuit materials shall be inherently non-nutrient to fungus. Materials shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage operation, or environmental capabilities of circuits delivered to this specification.

**3.6 DESIGN AND CONSTRUCTION.** Circuit design and construction shall be in accordance with the requirements specified herein and in the detail specification.

**3.6.1 Circuit.** Each device shall be a complete electronic circuit fabricated within a single piece of silicon material. Circuits made to this specification shall be made in a continuous manufacturing process using planar diffusion fabrication techniques.

**3.6.2 Electrical Interconnections.** Interconnections within the circuit package consisting of jumper lead wire shall be minimized with preference being given to deposited metallic conductors. Either method shall be arranged so that no crossovers are present.

**3.6.3 Internal Construction.** No lacquer, grease, paste, dessicant or other similar encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the circuit assembly.

### 3.7 LEADS AND PACKAGE

3.7.1 Package. Each circuit shall be securely mounted and hermetically sealed within a package as shown in Figures 2 and 3 of this specification. The package exterior shall be gold-plated F-15 alloy\*, or equivalent, except in the vicinity of the leads. The circuit shall be electrically isolated from the package.

3.7.2 Leads. Circuit leads shall be gold-plated F-15 alloy\*, or equivalent. Leads shall be metallurgically consistent with soldering and resistance welding; they shall be uniform in quality and condition, and delivered clear of oil and grease films.

### 3.8 MARKING. The following markings shall be placed on each microelectronic circuit:

- (a) Terminal identifiers, orientation key and polarity markers as applicable.
- (b) Manufacturer's type designation.
- (c) Name, initials, or trademark of manufacturer.
- (d) Lot-date code.
- (e) Serial number.

#### 3.8.1 Restrictions on Markings

3.8.1.1 The date portion of the lot-date code shall reflect the production week during which the circuit was lidded.

3.8.1.2 For a given lot-date code, no serial number shall ever be repeated.

3.8.2 Legibility. All markings shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements.

### 3.9 PRODUCT ASSURANCE. Each microelectronic circuit delivered shall be free of any defect in design, material, manufacturing process, testing, and handling, which could degrade or otherwise limit its performance when used as specified. The manufacturer shall acquaint his personnel with the intended end use of circuits delivered to this specification, shall emphasize that utmost care be exercised throughout all phases of manufacturing, testing, and handling of these circuits, conduct quality-oriented training programs, select persons

\*F-15 is the ASTM designation for an alloy (containing nominally 29% nickel, 17% cobalt, and 53% iron) used primarily for sealing to glass in electronic application.

with superior capabilities for bonding, and utilize his best personnel at the second (100X) and third (40X) visual inspection.

3.9.1 Rework Provisions. No rework, except recleaning, of any circuit or portion thereof after bar inspection (paragraph 4.3.1) shall be allowed for devices delivered to this specification.

3.9.2 Control of Engineering Changes. The manufacturer shall not implement, in any production to this specification, any change in design, materials, processes, or controls without notification of the procuring activity. Said notification shall occur no later than 48 hours after implementation of change. Changes and notification shall apply only to designs, materials, processing, or controls not specifically covered by this specification. Any changes in the areas which are covered by this specification are subject to the provisions of paragraph 4.4.8 of this specification.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 **GENERAL.** The manufacturer is responsible for the performance of all inspections and tests specified herein and in the applicable detail specification unless otherwise specified. GSFC reserves the right to reinspect circuits for any requirements deemed necessary and to designate, at any time, representatives for in-plant surveillance and acceptance functions in connection with procurement of circuits to this specification.

4.1.1 The manufacturer is required to submit to GSFC, as a part of his bid response, a Quality Program Plan which is in accordance with NPC-200-3 and a Product Processing Plan that reflects compliance with the requirements specified herein. Changes to the approved Quality Program Plan and Product Processing Plan after contract or order award shall be in accordance with the requirements of paragraphs 3.9.2 and 4.4.8.

4.2 **CONDITIONS AND METHODS OF TEST.** Conditions and methods of test shall be in accordance with MIL-STD-750.

4.2.1 Alternate Test Methods. Other test methods or circuits may be substituted for those specified provided it is demonstrated to GSFC that such a substitution in no way relaxes the requirements of this specification. Written approval of alternate test methods must be received from GSFC prior to substitution for those specified herein.

4.3 **INSPECTIONS AND TESTS.** Each microelectronic circuit built to this specification shall undergo all inspections and tests in the sequence indicated in Figure-1. Circuits failing to meet the requirements specified herein shall not be shipped on the purchase order of contract.

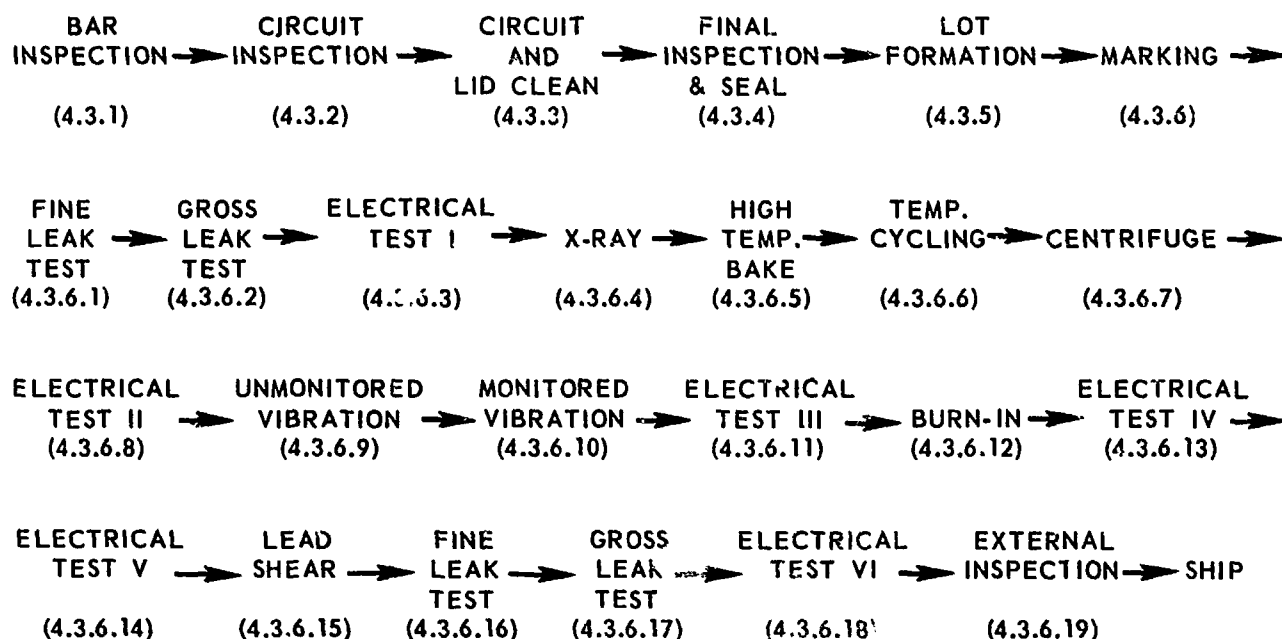


Figure 41-A1—Process flow diagram.

Any other processing steps, tests, measurements, and inspections conducted by the manufacturer, regardless of their nature or purpose, are subject to prior written approval by GSFC and should be delineated in the Product Processing Plan (See paragraph 4.1.1).

**ANY UNITS WHICH ARE QUESTIONABLE OR MARGINAL WITH RESPECT TO THE DEFECT OR REJECT CRITERIA SPECIFIED SHALL BE REJECTED.**

**4.3.1 Bar Inspection.** After scribing, each circuit bar shall be inspected under 100X magnification minimum using a metallurgical microscope with collimated light source and rejected for the following defects:

- (a) Scribe Defects. A scribe line, chip, crack or fracture which extends within 1 mil of an electrically active P-N junction, lead or bonding pad; cracks 1 mil in length or greater which point toward the active circuit metallization or bonds.
- (b) Metallization Voids. Lead width reduced to less than 50% of design lead width.
- (c) Shorted Metallization & Undercutting. Leads or contacts shorted by metallization. Where applicable, excessive gold overlap at edge of lead which indicates nonadherence of gold to interface material.
- (d) Metallization Defects (Other). (1) Excessive peeling or bubbles; (2) Corrosion (chemical reaction); (3) Metallization with less than two thirds coverage of electrically active contact areas; (3) Scratching of the metallization which



reduces the width of the undisturbed metallization to less than 50% of design width and which exposes silicon dioxide anywhere along the scratch; (4) Any smear of metallization extending contiguously more than one lead width from the design lead path or which reduces the spacing between adjacent leads to less than 50% of the design lead spacing.

- (e) Oxide Damage. Oxide voids exposing an electrically active junction area or exposing a silicon surface to an electrically active lead which is not, by design, already in contact with the same surface.

4.3.2 Circuit Inspection. Prior to cleaning and insertion in the Dry-Box, each circuit assembly shall be inspected under magnification of 100X minimum using a metallurgical microscope with collimated light source and rejected for the following defects:

- (a) All of the defect criteria listed in 4.3.1 above.
- (b) Ball Bonding Defects (Viewed directly from above). (1) Any bond which is placed such that silicon dioxide is not visible between the outer periphery of the ball area and any other metal or non-oxidized silicon; (2) Any bond which is placed such that the metal of the bonding pad is obviously pulled laterally; (3) Any bond which has the edge of the wire above the ball outside the boundaries of the bonding pad; (4) Any bond contact area made on the interconnecting metallization; (5) Ball diameter less than twice or more than five times the original wire diameter.
- (c) Wire Damage. Any lead which exhibits nicks, cuts, crimps, or scoring which cut into or deform the wire by more than 25% of its diameter.
- (d) Conducting Particles. Any device which contains loose or attached electrically conducting segments of material which are not part of the device design. Electrically conducting material shall include any material of sufficient conductance to cause device failure of any electrical specification by shorting contacts.
- (e) Bar Mounting Material. Presence anywhere on top surface of bar, package internal bonding pads, or package lid mounting surface.
- (f) Other. (1) Blistering, scratching or peeling of the gold plating at the internal lead post or lid mounting surface; (2) Broken glass around header leads; (3) Mechanical damage extending across the lid mounting surface which exposes Kovar; (4) Darkened or discolored header which may indicate insufficient gold plating; (5) Any unspecified or extra bonding wires, attached or unattached.

4.3.3 Following the visual inspection of 4.3.2 above, all acceptable devices shall be subjected to a cleaning process which shall be performed in the immediate vicinity of a dry-box. The cleaned units shall be immediately put into a dry-box containing a dry nitrogen atmosphere controlled to less than 20 ppm water content and not removed from that atmosphere until lidded. Device lids shall also be cleaned and immediately placed in the dry-box with the devices to be lidded.

4.3.4 Final Inspection and Seal

4.3.4.1 Inspection Options. The manufacturer shall indicate in his bid response which of the following inspection options he intends to utilize for a specific procurement action:

Option 1 — 100% by Production followed by  
100% by Quality Assurance.

Option 2 — 100% by Quality Assurance followed by  
25% sample inspection by Quality Assurance.  
If any units are rejected at the 25% sample inspection, the entire lot  
shall be resubmitted to Quality Assurance for 100% inspection.

4.3.4.2 Circuit Inspection. Each circuit assembly shall be inspected under magnification of 40X minimum using a collimated light source. Resolution of questionable defects shall be at 80X magnification. Defect criteria shall include the following:

- (a) All of the defect criteria listed in 4.3.2 above.
- (b) Broken or shorted bonding wires.
- (c) (1) Bar tilted; (2) Bonding wires positioned so that the wires protrude above the header ring; (3) Bonding wires of insufficient length; bonding wires which exhibit sufficient excess length so as to allow shorting to another wire, edge or surface of the bar, or to the bottom or top of the package; (4) Bar loose in header.
- (d) When viewed from directly above, wires which cross one another.
- (e) Bonding wire material greater in length than 2 wire diameters that is fixed only on one end, as for example, "pigtails".
- (f) Any extraneous particle of any composition either loose or attached to the circuit bar or any other part of the interior of the package.

(g) Bar tilted such that any part of the bar extends above the top of the internal lead plane.

(h) Glass fillet less than 80% of the periphery of the bar.

4.3.4.3 Lid Inspection. Each lid shall be inspected under 20X minimum magnification in the dry-box for damage, contamination, corrosion, or improper processing. All acceptable lids shall be identified and stored permanently in the dry-box until used.

4.3.4.4 Seal. Each acceptable circuit assembly and lid shall be sealed in the dry-box atmosphere.

4.3.5 Lot Formation

4.3.5.1 Definition. A lot shall consist of:

(1) Units lidded in a maximum of one week, and

(2) Units representative of a continuous production run with no lot containing units produced under two significantly differing production process, nor units previously rejected to this specification.

4.3.5.2 Identity. Lot identity shall be maintained throughout subsequent operations.

4.3.6 Marking and Circuit Screening Tests. Each microelectronic circuit shall be marked as specified in 3.8 before being subjected to the following electrical and environmental tests. The manufacturer's Quality Assurance personnel shall monitor the marking and test operations.

4.3.6.1 Fine Leak Test. Each circuit shall be subjected to a leak detection test having a sensitivity of at least  $50 \times 10^{-8}$  atm. cc/sec. Circuits exhibiting a leak rate in excess of  $50 \times 10^{-8}$  atm. cc/sec shall be rejected. The manufacturer shall submit his procedures for this fine leak test for GSFC written approval.

4.3.6.2 Gross Leak Test. Each circuit passing the fine leak test (4.3.6.1) shall be subjected to a gross leak test having a sensitivity of at least  $1 \times 10^{-5}$  atm. cc/sec. The manufacturer shall submit his Gross Leak Test procedure for GSFC written approval. Circuits not meeting approved inspection requirements shall be removed from the lot.

4.3.6.3 Electrical Test I. Each circuit shall be subjected to all of the electrical go-nogo DC tests described in the detail specifications at  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  before experiencing succeeding steps.

4.3.6.3.1 The following additional tests shall be performed at +25° C and at -55° C and +125° C on R-S Flip-Flop Counters (SN510 and SN511 or equal):

- (a) With a waveform of the type shown below applied to the clock pulse terminal of a flip-flop connected in the toggle configuration, the flip-flop shall be guaranteed to toggle with a clock amplitude of from 0.8 v. to 2.8 v. and guaranteed not to trigger with a voltage amplitude of 0.4 v. The following conditions apply to the measurements:

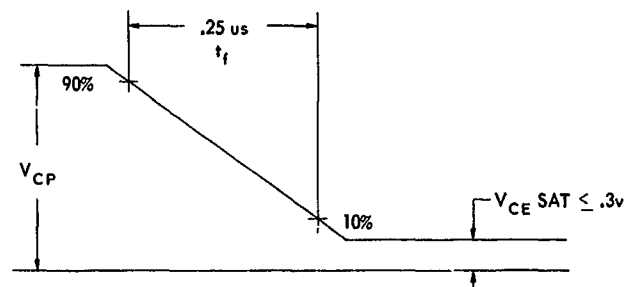
$$V_{cc} = 3 \text{ v.}$$

$$f = 200 \text{ kc.}$$

$$PW = 2 \text{ usec.}$$

$$t_r = 250 \text{ nsec.}$$

$$V_{ce \text{ sat}} \leq 0.3 \text{ v.}$$



- (b) With a minimum  $V_{off}$  applied to the preset terminal and the collector on the opposite side grounded, the collector of the preset transistor is guaranteed not to exceed the maximum  $V_{on}$ . Worst case loading is applied in each case — maximum loading when  $V_{off}$  is being measured, and no loading when  $V_{on}$  is being measured.

4.3.6.3.2 An additional test shall be performed on Ripple Counter Flip-Flops (SN 5112 or SN 5113 or equal). Under the conditions listed below and with a waveform of the type shown in paragraph 4.3.6.3.1 applied to the clock pulse terminal of the flip-flop connected in the toggle configuration, the flip-flop shall be guaranteed to toggle with a clock amplitude of from 2.0 v. to 3.3 v. for a SN 5112 and 2.5 v. to 4.4 v. for a SN 5113.

$$T_a = -55^\circ \text{ C}$$

$$V_{cc} = 3 \text{ v. (SN5112)}$$

$$= 4 \text{ v. (SN5113)}$$

$$Q^* \text{ \& } \bar{Q}^* = 16 \text{ dc loads}$$

$\bar{Q} \ \& \ \bar{Q} = 1 \text{ ac load}$

$f = 100 \text{ kc}$

$PW = 5 \text{ usec.}$

$t_r = 500 \text{ nsec.}$

$V_{ce \text{ sat}} \leq 0.3 \text{ v.}$

- 4.3.6.4 X-ray. Each circuit shall be radiographically inspected. The manufacturer shall submit his X-ray procedure and inspection criteria for GSFC written approval. Circuits not meeting approved inspection criteria shall be removed from the lot.
- 4.3.6.5 High Temperature Bake. Each circuit shall be stored at  $200^\circ \text{ C} \pm 5^\circ \text{ C}$  for 48 hours.
- 4.3.6.6 Temperature Cycle. Each circuit shall be subjected to 10 temperature cycles. One cycle shall consist of 15 minutes each at  $150^\circ \text{ C} \pm 5^\circ \text{ C}$  and  $-55^\circ \text{ C} \pm 5^\circ \text{ C}$  with a maximum transfer time between temperature extremes of 5 minutes. A cycle may begin at either temperature. The liquid immersion method of temperature cycling shall not be employed for this test.
- 4.3.6.7 Centrifuge. Each circuit shall be subjected to 20,000 G constant acceleration in the  $Y_1$  direction.
- 4.3.6.8 Electrical Test II. Each circuit shall be subjected to a package to lead isolation test. Each lead of the circuit shall be checked to determine isolation with respect to the circuit package.
- 4.3.6.9 Unmonitored Vibration. Each circuit shall be subjected to a swept frequency vibration while unmonitored with no applied voltages. Vibration will be run in each of the X, Y, and Z directions at 30G peak minimum with frequency sweeping from 120 cps to 2000 cps at a rate of  $1\frac{1}{2}$  octaves per minute.
- 4.3.6.10 Monitored Vibration. Each Circuit will be subjected to a monitored vibration in the Y direction at 30 G peak minimum at  $120 \pm 10\%$  cps. Voltage will be monitored, and the rejection criterion will be the detection of noise 100 mv p-p or greater occurring at frequencies greater than 60 cps. Suitable detection circuits will be utilized to detect noise of at least 100 mv p-p above the output low voltage level and frequencies of 60 cps. or greater.
- 4.3.6.11 Electrical Test III

4.3.6.11.1 Pre-Variables Data Record. Each circuit in the lot shall be subjected to a dc go-r test at  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$  as indicated in Table 1 below. Circuits not within the limit specified shall be removed from the lot.

4.3.6.11.2 First Variables Data Record (VDR). Variables data for  $V_{on}$ ,  $V_{off}$ , and  $I_{in}$  shall be recorded on all circuits in the lot with  $V_{cc} = 6\text{ v.}$  at  $T_a = 25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ . Loading conditions for measurement shall be as follows:

Table 1

Equivalent Device Type	$V_{on}$	$V_{off}$ Loaded Col. Output	$V_{off}$ Loaded E.F. Output	$V_{off}$ Unloaded Col. Output	Current Drain ID	$V_{off}$ Clamped	$V_{off}$ Unclamped
SN510	0.3V.Max.	2.OV.Min.		4.OV.Min.	100 $\mu\text{ a}$ Max.		
SN511	0.3V.Max.	2.OV.Min.	4.OV.Min.	4.OV.Min.	100 $\mu\text{ a}$ Max.		
SN512	0.3V.Max.	2.OV.Min.		5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN513	0.3V.Max.	2.OV.Min.	4.OV.Min.	5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN514	0.3V.Max.	2.OV.Min.		5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN515	0.3V.Max.	{ Pins 6 & 10 2.OV.Min. Pin 8 2.OV.Min.		{ Pins 6 & 10 4.OV.Min. Pin 8 5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN516	0.3V.Max.	2.OV.Min.	4.OV.Min.	5.OV.Min.	100 $\mu\text{ a}$ Max.	1.45V.Min. 2.5V.Max.	5.OV.Min.
SN517	0.3V.Max.				100 $\mu\text{ a}$ Max.		
SN518	0.3V.Max.	2.OV.Min.		5.OV.Min.	100 $\mu\text{ a}$ Max.	1.35V.Min. 2.5V.Max.	
SN5191	0.3V.Max.	2.OV.Min.		5.OV.Max.	100 $\mu\text{ a}$ Max.		
SN893	0.3V.Max.	2.OV.Min.	4.OV.Min.	4.OV.Min.	100 $\mu\text{ a}$ Max.		
SN5161	0.3V.Max.	2.OV.Min.		5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN 5162	0.3V.Max.	2.OV.Min.	4.OV.Min.	5.OV.Min.	100 $\mu\text{ a}$ Max.		
SN5111	0.3V.Max.	2.OV.Min.	4.OV.Min.	4.OV.Min.	100 $\mu\text{ a}$ Max.		
SN5112	0.3V.Max.	{ E.F. Loaded 4.OV.Min. Col. Loaded 2.OV.Min.	3.6V.Min.		100 $\mu\text{ a}$ Max.		
SN5113	0.3V.Max.	{ E.F. Loaded 4.OV.Min. Col. Loaded 2.OV.Min.	3.6V.Min.		100 $\mu\text{ a}$ Max.		

NOTE:  $V_{cc} = 6.0\text{ Volts}$  in all cases.

For gates:

For Q (collector outputs),  $R_Q = 6.62\text{ Kohms}$

For Q\* (emitter-follower outputs),  $R_{Q*} = 1.16\text{ Kohms}$

For flip-flops:

For Q (collector outputs),  $R_Q = 8.27$  Kohms

For Q\* (emitter follower outputs),  $R_{Q^*} = 1.44$  Kohms

Since the authenticity of these data can affect future processing of the lot, data verification must be accomplished at the time of the readings. Either Method A or Method B below may be employed.

**4.3.6.11.2.1 Method A (correlation method)** A correlation sample of a minimum of 5 pieces of the device being tested will be retained by manufacturers' Quality Assurance personnel. A history log will be kept on this sample by recording the values obtained when the sample is read for the appropriate parameters being verified. Statistical methods will be employed to ascertain if the readings indicate the test equipment is functioning properly. The correlation sample will be read immediately prior to commencing VDR for the lot. The correlation sample will be read at least once an hour, and at the end of the lot VDR.

If the correlation sample readings indicate the test equipment is malfunctioning or inaccurate, all data on devices read since the last satisfactory correlation will be destroyed, and new data will be taken after suitable corrective action has removed the test equipment fault.

**4.3.6.11.2.2 Method B (duplication method)** The entire lot will be submitted to VDR. Upon completion of VDR, the lot will be withheld from further processing pending verification by a Quality Assurance inspection.

A sample of 10% of the lot (25 piece minimum; 100 piece maximum) will be re-read by Quality Assurance and readings compared to those obtained in the VDR. The equipment used for VDR will not be used for this verification.

- (a) If readings are duplicated within the tolerance of the equipments, the lot may be released for the next processing step.
- (b) If the readings are not duplicated within the tolerance of the equipments, suitable corrective action will be taken and the lot reprocessed through VDR and this verification until the validity of the data is established.

**4.3.6.12 Burn-In** — Each circuit shall be operated at  $+125^{\circ}\text{C} \pm 5^{\circ}\text{C}$  for 300 hours minimum with  $V_{cc} = 6$  v. During the period switching voltages with a frequency of 50 cps to 100 kcps shall be applied such that the outputs of the device are switching between the logical "one" and logical "zero" states at a corresponding frequency.

#### 4.3.6.13 Electrical Test IV —

4.3.6.13.1 Second Variables Data Record. Post Burn-In variables data shall be recorded per the tests and procedures of par. 4.3.6.11.2. These data must be verified by the same method (A or B) used to verify the data of 4.3.6.11.2.

4.3.6.13.2 The data of par. 4.3.6.11.2 and par. 4.3.6.13.1 shall be compared. Any unit exhibiting a change greater than the following limits shall be considered a reject.

$$(a) \Delta V_{on} = \pm 10\% V_{on} \text{ (initial) (paragraph 4.3.6.11.2). (See Note )}$$

$$(b) \Delta V_{off} = \pm 10\% V_{off} \text{ (initial) (paragraph 4.3.6.11.2)}$$

$$(c) \Delta I_{in} = \pm 10\% I_{in} \text{ (initial) (paragraph 4.3.6.11.2)}$$

Note: For devices with emitter-follower outputs, the reject criterion for  $\Delta V_{on}$  shall be that it not exceed 20 mv.

4.3.6.13.2.1 If the number of rejects determined in 4.3.6.13.2 is greater than 25% of the lot, the lot will be disqualified for use on this specification except that GSFC reserves the right to accept any lot with excess failures.

4.3.6.13.2.2 If the number of rejects determined in 4.3.6.13.2 is less than 25% of the lot, the rejects will be removed from the lot and disqualified for use on this specification. The remainder of the lot will proceed to the next processing step.

4.3.6.14 Electrical Test V — Each circuit shall be resubjected to and pass all of the DC tests specified in 4.3.6.3 before experiencing succeeding steps.

4.3.6.14.1 In addition, R-S Flip-Flop Counters (SN510 and SN511 or equal) and Ripple Counter Flip-Flops (SN5112 and SN5113 or equal) shall be resubjected to and pass the tests specified in 4.3.6.3.1 and 4.3.6.3.2.

4.3.6.15 Lead Shear — Where applicable, each circuit shall be removed from its individual test transporter or carrier.

4.3.6.16 Fine Leak Test — Each circuit shall be subjected to a leak detection test having a sensitivity of at least  $1 \times 10^{-8}$  atm. cc./sec. Circuits exhibiting a leak rate in excess of  $1 \times 10^{-8}$  atm. cc/sec. shall be rejected. The manufacturer shall submit his procedures for this fine leak test for GSFC written approval.

NOTE: The sensitivity of the fine leak test at this point differs from that specified in paragraph 4.3.6.1



4.3.6.17 Gross Leak Test -- Each circuit shall be resubjected to and pass the gross leak detection test specified in 4.3.6.2.

4.3.6.18 Electric Test VI -- An electrical test shall be conducted on each circuit to insure the capability of performing the logical function for which it was designed. The test will consist of the 6-volt-A-C switching time parameter measurements specified in the detail specifications. Any device not meeting the limits specified will be rejected from the lot and disqualified for use on the specification. In addition, the lot accept/reject decision shall be in accordance with 4.3.6.13.2.1.

4.3.6.19 External Inspection -- Each circuit shall be examined by the manufacturer's Quality Assurance personnel under a minimum of 20X magnification and rejected for the following defects.

- (a) Smeared, illegible, or insufficient marking.
- (b) Dented or misaligned lids.
- (c) Discolored header.
- (d) Lead damage such as nicks, cuts, or scratches in excess of 25% of the smallest lead dimension, improper finish, missing leads, and similar defects.
- (e) Package cracks, chipping, blistering and similar anomalies.
- (f) Lead or package contamination such as grease, film or paint on leads.

4.3.7 Supplemental Tests -- Circuits delivered to this specification shall be capable of meeting the requirements specified below in addition to those previously specified. The manufacturer need not perform testing specifically for any purchase under this specification but shall comply with the documentation requirements of 4.4.

4.3.7.1 Data Limitations --

4.3.7.1.1 Only data on circuits of identical design and construction made by identical fabrication processes are considered acceptable for purposes of this specification.

4.3.7.1.2 Data used for demonstrating conformance to the specified supplemental tests shall be that most recently accumulated by the manufacturer but in any case shall not predate a specific bid response date.

4.3.7.2 Test Requirements -- The tests shown in Table 2 shall apply.

Table 2

Examination or Test	MIL-STD-750 Method	Specific Conditions	LTPD
Physical Dimensions	2066		20
Soldering Heat	2031.1	1 cycle	15
Thermal Shock	1056.1	Test Condition A	15
Shock	2016.1	4 blows each in X <sub>1</sub> , Y <sub>1</sub> , Z <sub>1</sub> Planes	15
Constant Acceleration	2006	20,000 G for 1 minute ea. orientation, X <sub>1</sub> , Y <sub>1</sub> , Z <sub>1</sub>	15
Terminal Strength	2006.1	Test Condition E 1 arc; +45° from normal return to 0, -45° C from normal return to 0; 2 oz. weight	15
High Temperature Storage Life	1031.1	T <sub>A</sub> = +200° C min. ±5° C t = 1000 hrs.	λ = 10%
Operating Life	1026.1	T <sub>A</sub> = +125° C ± 5° C t = 1000 hrs. 50 cps < f < 100 kcps	λ = 10%

4.3.7.3 Statistical Sampling and Life Test Procedures — The statistical sampling and life test procedures of Appendix C of MIL-S-19500 shall apply to the supplemental tests specified in 4.3.7.2.

4.3.8 Lot Shrinkage Analysis — At each step specified below, lot shrinkage analysis shall be performed as indicated:

<u>TEST</u>	<u>ANALYSIS LEVEL</u>
X-Ray	I
Electrical Test II	II
Monitored Vibration	II
Electrical Test III	II (or III at vendor's option or at NASA's direction*)
Electrical Test IV	II (or III at vendor's option or at NASA's direction*)
Electrical Test V	II (or III at vendor's option or at NASA's direction*)
Fine Leak Test (4.3.6.16)	I
Gross Leak Test (4.3.6.17)	I
Electrical Test VI	II (or III at vendor's option or at NASA's direction*)
Supplemental Tests	III

\*For bidding purposes the cost of performing a formal failure analysis at this point shall not be included in the unit cost.

**4.3.8.1 Levels of Lot Shrinkage Analysis — The following levels of lot shrinkage analysis shall apply:**

- I — Record all failures by category and number per category.**
- II — Perform I plus a cursory Failure Analysis, which shall include:**
  - a) Verification of failure on all pieces, including performance of normal electrical operational tests and lead-to-lead and lead-to-case continuity tests.
  - b) Opening of a prescribed number of devices for visual inspection only under appropriate magnification (40X to 200X). For quantities of failed devices of less than 30, open a minimum of 3 devices; for more than 30 failures, open 10%.

... as a formal, documented Failure Analysis.

4.3.8.1.1 Failure Analysis Requirements — Whether cursory or formal in nature, any failure analysis conducted shall be designed to isolate the cause (s) of failure and yield adequate conclusions to initiate a plan for corrective action to eliminate the cause and prevent reoccurrence of the type failure-mode reported.

4.3.8.2.2 When a formal failure analysis is conducted, two reproducible copies of the Failure Analysis Report shall be submitted within two weeks of the date that the defect occurred to the GSFC Technical Representative. The report shall include, as a minimum, the following information:

- (a) Date defect occurred
- (b) Lot Identification, Date Code, and Size of Lot
- (c) Device Type and Serial Number(s) of Failed Circuits(s)
- (d) Test and/or Inspection at which defect was first noted
- (e) Failure-Mode Category
- (f) Actual Mode of Failure
- (g) Cause of Failure
- (h) Corrective action taken or to be taken
- (i) Effect on other devices in the lot
- (j) Purchase orders or contracts affected

4.3.3.2 Periodic Review of Lot Shrinkage — GSFC will conduct, with the manufacturer, periodic reviews of lot shrinkage at each step indicated in 4 3.8 as specified in the individual Purchase Order or Contract.

#### 4.4 DOCUMENTATION AND DATA SUBMITTAL

4.4.1 General. Each microelectronic circuit furnished under this specification shall be accompanied by suitable records showing compliance with specified requirements. Test and inspection results must be concurred in by the manufacturer's Quality Assurance personnel and so indicated on a devices' record. Records shall be linked to specific circuits by lot-date code, serial number, and manufacturer's identification.

- 4.4.2 Certification. The manufacturer shall certify that each device meets all applicable specification requirements, including the requirements of 4.3.7.
- 4.4.3 Parameter Data. Recorded parameter data for individual circuits, (paras. 4.3.6.11.2 and 4.3.6.13.1) shall be furnished in a format requiring minimum interpretation.
- 4.4.4 Inspection and Test List. Documentation shall be furnished showing clearly that both lot screening and supplemental inspections and tests were conducted in accordance with specified requirements and shall reference pertinent Failure Analysis reports. In addition, lot shrinkage shall be recorded at each test or inspection step shown in Figure-A1 beginning with, and including X-Ray inspection (4.3.6.4).
- 4.4.5 Document Copies. The manufacturer shall prepare all documentation, except X-rays, in duplicate and process it as follows:
- (a) Original — retained by manufacturer.
  - (b) Reproducible copy — ship with device(s).
- 4.4.6 Document Cross-Reference. All documentation, whether retained or submitted by the manufacturer, shall be cross-referenced to the applicable Contract or Purchase Order.
- 4.4.7 Record Retention. All records, excluding X-rays, pertinent to a specific circuit shall be retained by the manufacturer for a minimum of 3 years.
- 4.4.8 Deviations. Three (3) copies of all deviation or change requests shall be submitted to the GSFC Contracting Officer and one (1) copy to the Cognizant GSFC Technical Representative referencing the purchase order or contract to which it applies. Requests must make specific reference to the portion of device detail specification, this specification, or referenced documents to which the request applies and may be submitted by telegram; then confirmed by letter. All deviations or changes must have GSFC Contracting Officer approval before devices affected can be accepted for use by GSFC.

## 5. PREPARATION FOR DELIVERY

- 5.1 GENERAL. Unless otherwise specified, the manufacturer shall be responsible for packaging each circuit furnished under this specification in such a manner as to prevent degradation, corrosion, deterioration or physical damage, and insure safe delivery in good condition. The manufacturer shall be responsible for any damage to circuits resulting from faulty packing,

preservation or packaging, and shall replace such circuits with acceptable circuits without cost to GSFC.

5.2 PRESERVATION AND PACKAGING. Each circuit furnished under this specification shall be protected and packaged to afford protection at all handling points between manufacturer's final inspection and user's final installation. Each circuit shall be packaged in a transparent rigid-plastic container using flexible foam inserts for cushioning, or the equivalent thereof, as to allow viewing the circuit markings without opening the container.

5.3 PACKING. Containers enclosing the packaged circuits to be furnished under this specification shall be packed in an exterior container, using cushioning on all sides to prevent movement. Required documentation (4.4.5b) shall be enclosed in this exterior container. As a minimum, units packaged as specified shall be packed in containers of the type, size, and kind commonly used for the purpose, in a manner that will assure acceptance by common carrier and safe delivery at destination. Shipping containers shall comply with the Uniform Freight Classification Rules or regulations of other carriers as applicable to the mode of transportation.

## 6. NOTES

6.1 NOTICE. When GSFC drawings, specifications, or other data are used for any purpose other than in connection with a definitely related GSFC procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that GSFC might have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Custodian:  
NASA - Goddard Space Flight Center

Preparing Activity:  
Goddard Space Flight Center

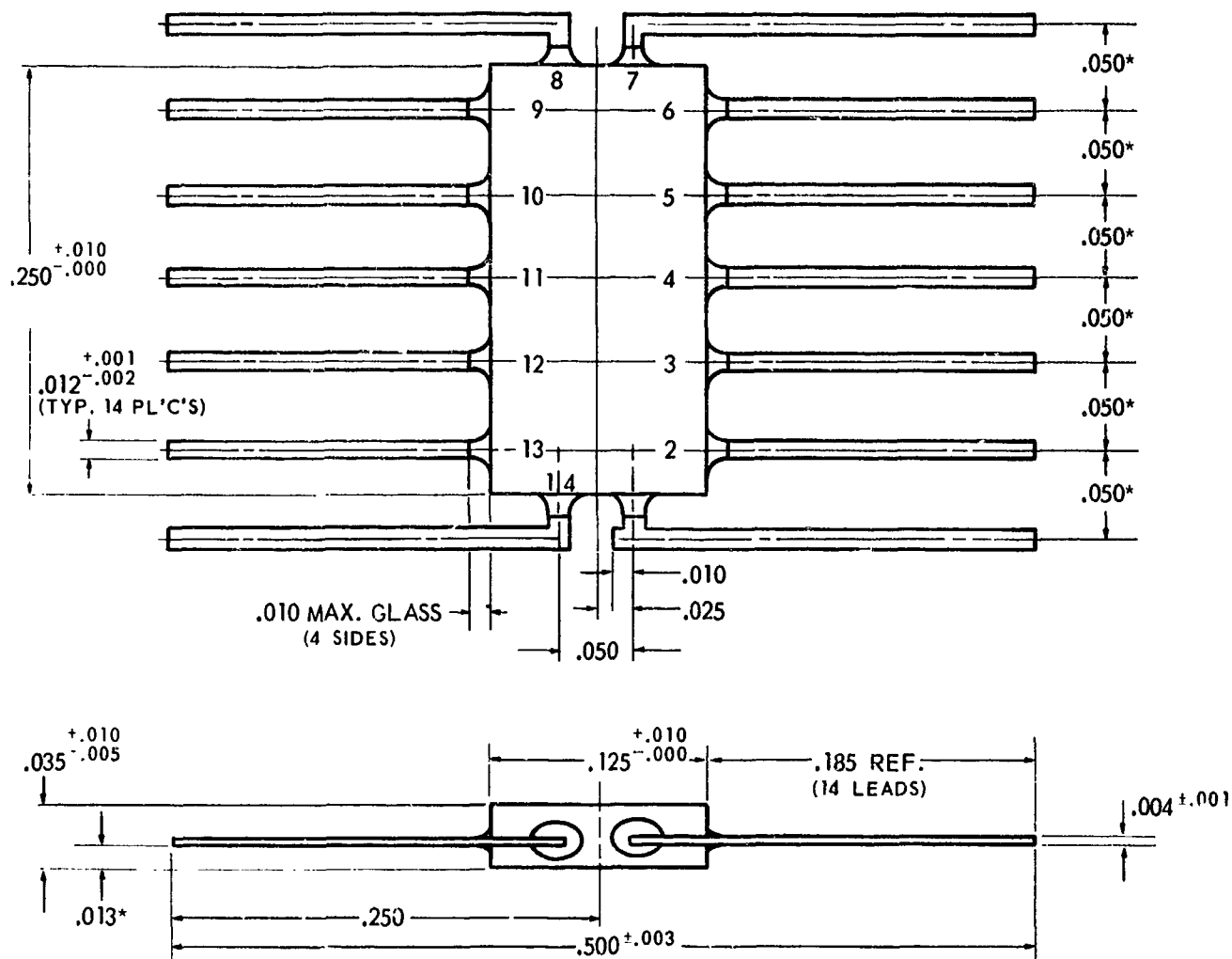
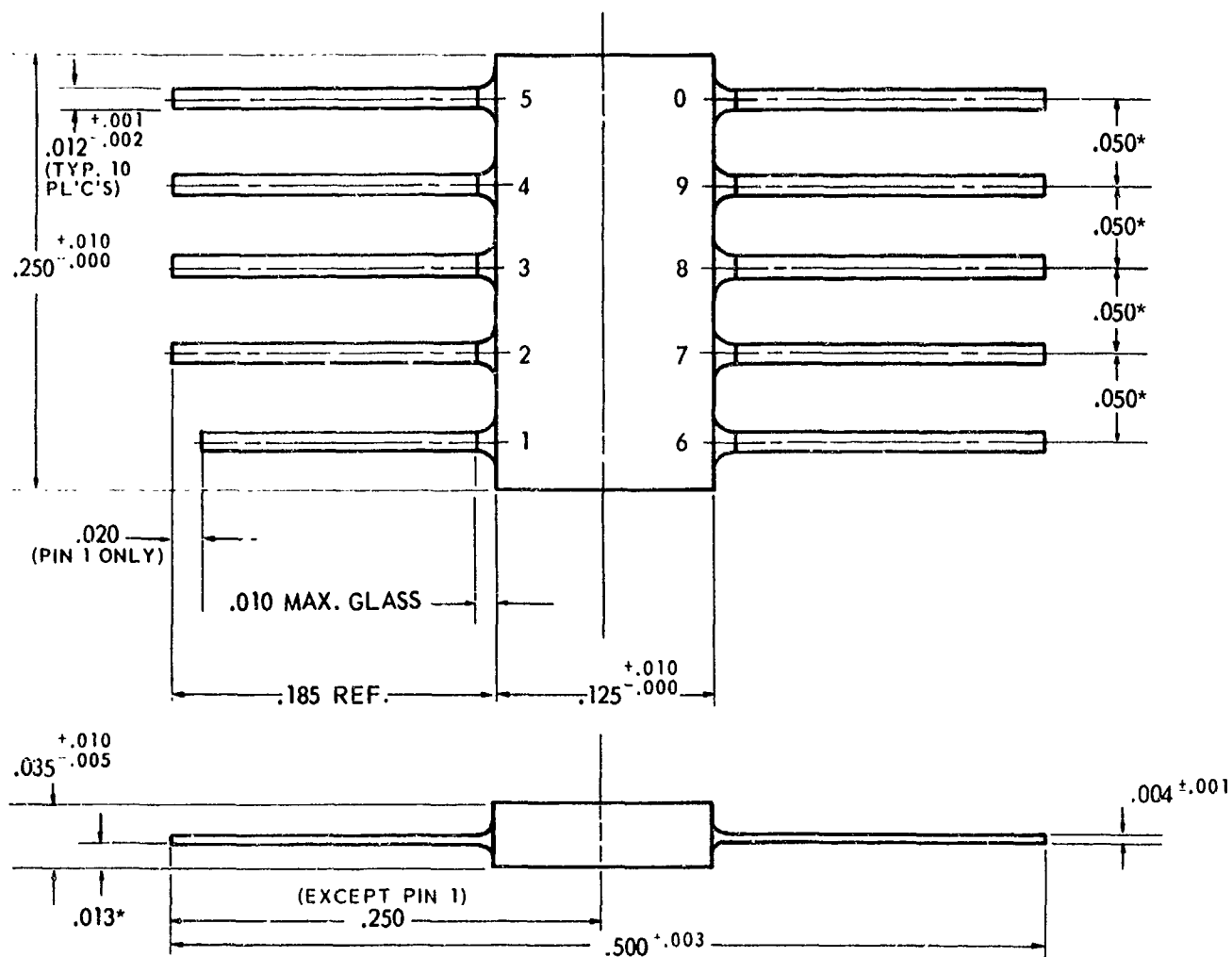


Figure 41-A2—Case outline drawing.



NOTES:

Lead centerlines located in true position within  $\pm.005$  of body centerline.

\* Measured at point of emergency from package non-cumulative.

Weight: 0.12 gram max.

Figure 41-A3—Case outline drawing.



N67-31604

## 42. DIGITAL MICROCIRCUIT STERILIZATION TEST PROGRAM

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Several integrated circuits from various manufacturers were subjected to qualification tests consisting of heat sterilization, vibration, shock, acceleration, temperature cycling and operating long life. This paper discusses the relative merits of each as determined by these tests. The various environments, life test equipment designs, and automatic measurement equipment are described. The parameters, statistical analyses, and results are presented, along with detailed failure analyses of catastrophic and degradation failures. A final test report will be prepared at the conclusion of the 10,000-hour life test.

### INTRODUCTION

It is a firm policy of the National Aeronautics and Space Administration that all spacecraft with a possibility of planetary impact must be sterilized. In compliance with this policy, the Jet Propulsion Laboratory presently requires thermal sterilization of such flight equipment at  $135 \pm 4^\circ\text{C}$  for a period of 24 hours in an inert atmosphere. Because of this requirement, the Parts Reliability Staff has initiated an extensive electronic component sterilization test program. This report is an account of the Digital Microcircuit Sterilization Test Program. It summarizes the environmental and life test results through 8,000 hours of "life test," which is a portion of the overall component sterilization test program designed to assess the effects of heat sterilization on electronic components. The initial phases of the program have been completed.

The primary objective of this program is to establish a Sterilization Parts List (JPL Specification No. ZPP-2010-SPL) that tabulates the electronic component parts capable of withstanding several 36-hour periods of nonoperational storage at  $145 \pm 2^\circ\text{C}$  without significant degradation, in accordance with JPL Specification No. XSO-30275-TST-A. Secondary objectives are the use of the test results to compare vendor quality and the analysis of long-term failure modes.

### THE TEST PROGRAM

A total of 665 microcircuits, representing seven distinct part types (codes), (Figure 42-1) were selected for this program (Table 42-1); 95 of each code were ordered

for the test. The purchase orders for these parts stated that the parts would be subjected to a Reliability Sterilization Test. It was intended that all parts of each part type be of the same date code, but codes 4 and 7 were each mixes of two date codes. There was no evidence that any manufacturer selected premium microcircuits.

Each of the part types was divided into five groups, as follows:

1. Group A. No temperature cycling (control group).
2. Group C. Six cycles of temperature sterilization, each cycle consisting of 36 hours at 145°C followed by 24 hours at 25°C.
3. Group D. Same as Group C, except that these parts operate continuously during the life test without being removed for measurement.
4. Group E. Same as Group C, except that these parts are nonoperational during the life test.
5. Groups F and G. The parts comprising Group F are measured prior to the electrical tests of the other groups, and again after the tests, when they are labeled Group G; this group of parts is used for equipment checks, and is never subjected to environmental tests.

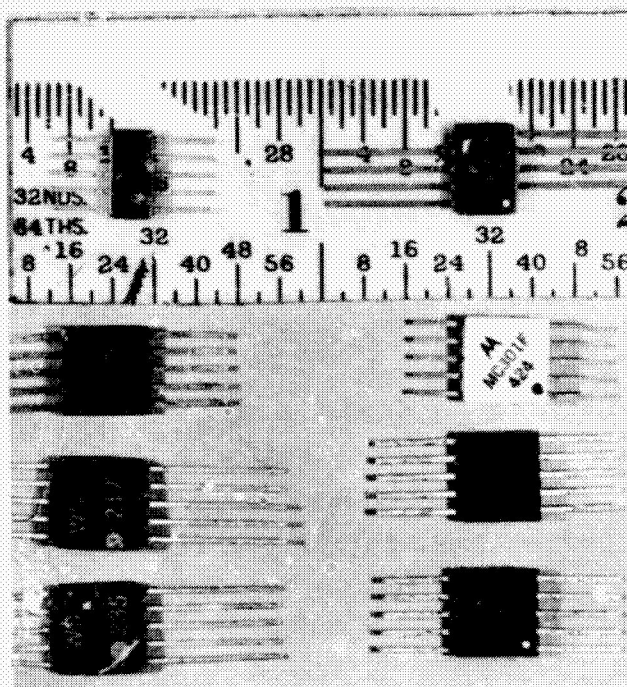


Figure 42-1—The seven parts subjected to the test.

Table 42-1

Description of Test Items

Code number	Manufacturer	Manufacturer part designation number	Function
1	Motorola	MC301F	Gate
2	Signetics	SE101G	Gate
3	Westinghouse	WS217 (WM201)	Gate
4	Fairchild	913	Flip-flop
5	Signetics	SE124G	Flip-flop
6	Texas Instruments	SN530	Flip-flop
7	Westinghouse	WS235 (WM202)	Flip-flop

After sterilization temperature cycling, parametric measurements are compared with the initial test results and analyzed for significant changes. All of the test groups are then subjected to the spacecraft component qualification environments of vibration, shock, acceleration, and temperature cycling. A 10,000-hour life test is then applied to the groups to simulate the long flight periods of planetary missions. During this life test, Groups A, C, and D are operated at maximum rated temperature. Nonoperational Group E parts are stored at the same temperature. Group A (no cycles) and Group C (six cycles) are compared at specific points during the test to detect significant differences due to sterilization.

Upon completion of the 10,000-hour life test, Group E parts are removed from temperature storage, and, in conjunction with Group D, are subjected to an additional 250-hours of operating life at maximum rated temperature. The tests of Group E simulate conditions of an extended non-operational mission in which the equipment is turned on remotely at or near its destination. Group D is included as a control group operated at maximum temperature, to simulate an extended operational mission.

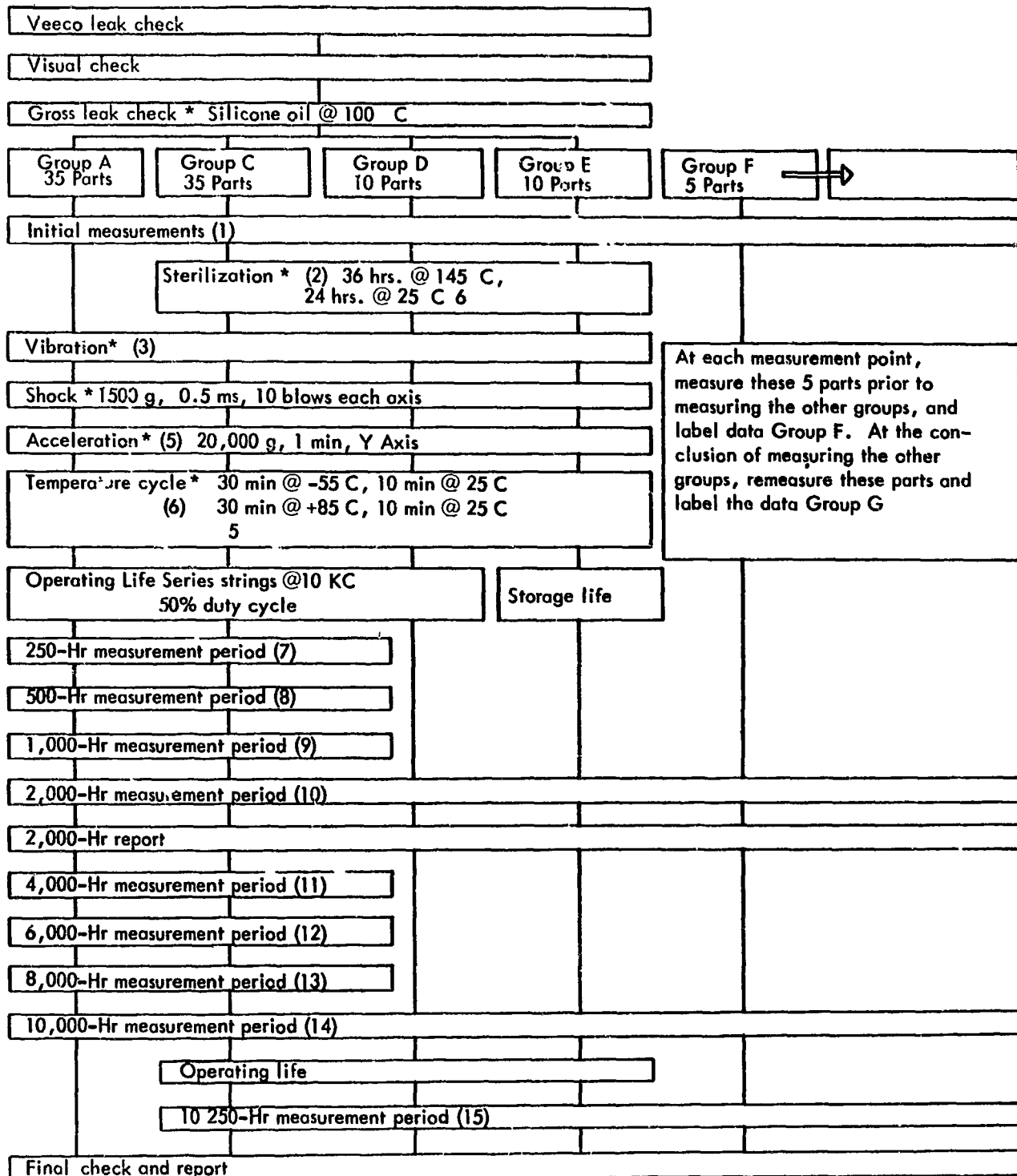
The goal of this test program is to determine the reliability of each part type in respect to the JPL Hi-Rel performance level, which is a failure rate of less than 1 percent per 1,000 hours of operation at 90 percent confidence, when operated at maximum rated stress conditions. In most instances, this level of proven reliability corresponds to a typical failure rate of 0.01 percent per 1,000 hours when operating in circuits designed with proper derating of stress levels and allowable parameter drift.

The test procedure for this microcircuit program, summarized in the flow diagram of Figure 42-2, is as shown in JPL Specification ZPP-2121-GEN., Rev. A.

Figure 42-3 shows a Texas Instrument Automatic Component Tester with a JPL built interface for adaption to integrated circuits. Tektronix digital oscilloscope (Figure 42-4) formed the heart of the automatic switching time tester used for the dynamic measurements.

All dc parameters were measured and recorded automatically on IBM cards. The switching time measurements were performed semiautomatically; that is, once a specific test, such as rise time, was set up by push button, the operator tripped a switch to record the reading automatically on an IBM card. Dc or switching time measurements for a given code were completed in a single day. The proper test setup was verified by measuring the Groups F and G equipment check parts both immediately before and immediately after measurement of the remaining test groups.

The data cards were edited on an IBM 1620 II Computer for completeness and gross errors, such as over-punches. Because of the extreme difficulties in re-running measurements, suspect data were coded as temporary failures and excluded from the statistics for that measurement period. Data analysis of the microcircuit program was handled by contract to Motorola Semiconductor, Inc.



\*Measure and record data for all groups at conclusion of step.

Figure 42-2—Test sequence flow chart.



Figure 42-3—The Texas Instrument component tester with JPL interface for integrated circuit..

## TEST RESULTS AND ANALYSIS

An average of 20 parameters recorded for each code yielded a grand total of approximately 14,000 readings for each measurement period. Since the statistics were performed off-lab, they necessarily had to be formulated early in the program, and, consequently, the statistical results were designed to answer the primary questions of the effects of sterilization on the components and the longevity of operating parts versus nonoperating parts. There is a great deal of engineering information yet to be gained, and that will be provided in the final report. The analysis performed thus far, however, does estimate reliability, the behavior of microcircuits under stress, and the relative performance of vendor products.

Definitions of catastrophic failures for the environmental and life tests are as follows:



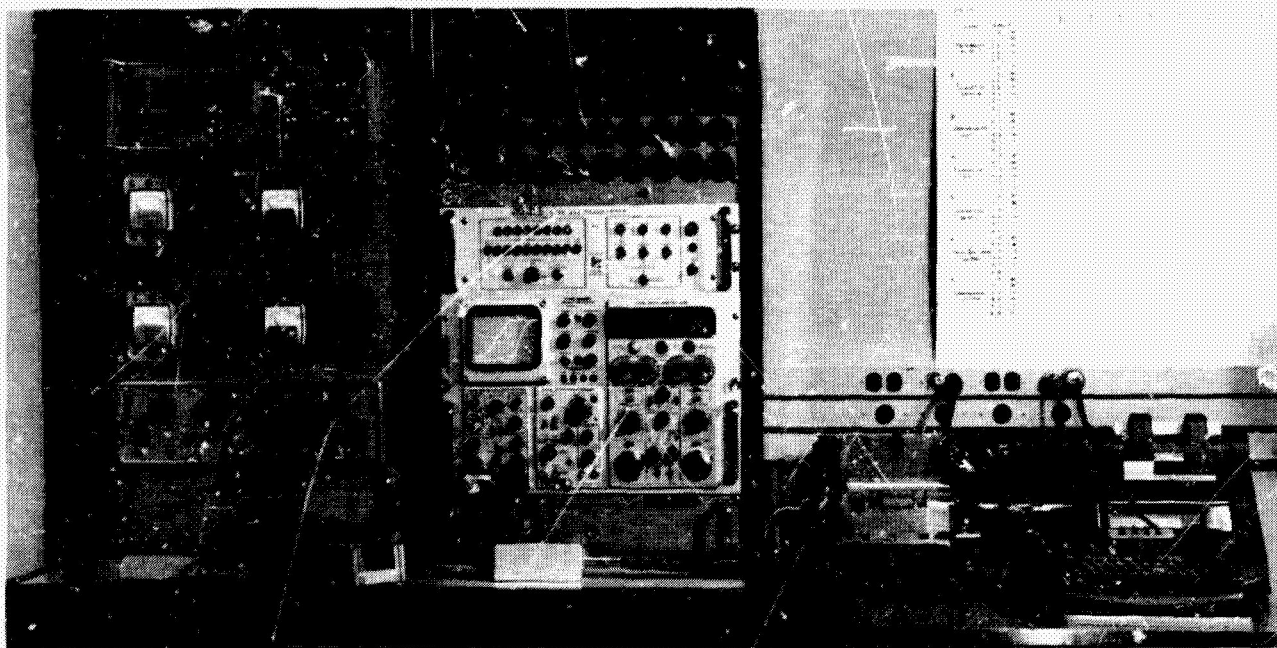


Figure 42-4—Switching time test equipment.

1. Environmental catastrophic failure is the inability of a microcircuit to generate an output waveform during the switching time test that follows an environmental test. Note that the microcircuits were not electrically monitored during the environmental tests.
2. Life test catastrophic failure is the failure of a microcircuit to operate the life test strings.

A parametric failure is defined as the failure of a microcircuit to meet any specified parametric limit. Parametric failures are not removed from a test for failure analysis, and may, in fact, be considered as a failure for statistical purposes at one measurement step and not at the next, having gone out of limits and then returned. The limits specified, some of which were unrealistic and had to be changed, are those supplied by the manufacturer. The 10,000-hour life test results will provide valuable data in selecting end-of-life limits.

The Veeco and gross leak tests showed that Motorola had the least problem with hermeticity, and that Westinghouse was at the other end of the spectrum. The main faults uncovered with the 20X visual examination were the following:

1. Lids off center.
2. Leads bent close to case.
3. Leads twisted.
4. Chipped cases.

5. Bubbles in the case.
6. Discolored internal leads.
7. Foreign material within the glass walls of case.
8. Lid overhang or not enough sealant.
9. Too much sealant.

The performance of the microcircuits under environmental and life tests (Table 42-2) allows the effects of sterilization, environment, and life testing on Groups A, C, D, and E to be readily assessed. Detailed parametric behavior in the form of graphs will be prepared for the final report. Analyses have been performed by JPL on most of the microcircuits that failed catastrophically during environmental or life testing, to discover the underlying physical causes of failure and the necessary corrective action. Table 42-3 is a list of all components that failed catastrophically during the environmental tests and the first 8,000 hours of life tests.

Table 42-2

Catastrophic Failures by Test Steps

	Non Sterilized Group A							Sterilized Group C							Operating Group D							Non Operating Group E							Total							
Code	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	1	2	3	4	5	6	7	
Initial			3			1				1	1						2							1							7	1		1	1	
Sterilization														1						1	1												1	2		
Vibration														1																				1		
Shock															1														1							
Acceleration	1		1					3		3				1			1								1				4		4	2			1	
Temperature Cycle						1	1	2		2					1														3		2			1	1	
250 Hours Life	2					2		1		1			1																3		1			3		
500 Hours Life			2					1			1																		1		2	1				
1,000 Hours Life	1						1			2			1																1		2			1	1	
2,000 Hours Life							1							1													1								3	
4,000 Hours Life			1					1																				1			1					
6,000 Hours Life	1		1			1				1																		1			2			1		
8,000 Hours Life	1					1																						1						1		
10,000 Hours Life																																				
10,250 Hours Life																																				
TOTAL	6	0	8	0	0	6	3	8	0	10	2	0	2	4	2	0	2	1	0	1	1	0	0	1	1	0	0	2	16	0	2	1	4	0	9	10

Table 42-3

## Failure Analysis Summary

Code	Group	Ser. no.	Step part failed	Description of Failure
1	A	3	12	Analysis not complete
1	A	10	7	Cured by storage at 150°C
1	A	13	9	Analysis not complete
1	A	26	7	Cured by storage at 150°C
1	A	27	5	Die off header; broken bonds
1	A	33	13	Analysis not complete
1	C	2	6	Die off header; burned wire
1	C	14	7	Wire broken at bond; wire deformed at bonding
1	C	17	8	External solder joints defective
1	C	19	5	Analysis not complete; poor bonds and workmanship
1	C	21	11	Analysis not complete
1	C	26	6	External solder joints defective
1	C	29	5	Die off header
1	C	33	5	Broken wires
1	D	1	6	Die off header; broken wires; poor bonds
1	D	5	4	Die off header
2	F-G	2	10	(Overvoltage during test set-up) no analysis
3	A	1	12	Analysis not complete
3	A	5	11	Analysis not complete
3	A	8	8	Poor bond 5
3	A	10	5	Pin hole in SiO <sub>2</sub> under pad 4
3	A	20	1	Introduced water caused aluminum to disappear
3	A	26	1	Corrosion near pad 5
3	A	30	8	Bond 5 lifted; poor workmanship
3	A	35	1	Leadaway from pad 5 corroded and open
3	C	4	5	*
3	C	6	6	*
3	C	7	7	*
3	C	10	9	*
3	C	11	5	*
3	C	12	9	Pin hole in SiO <sub>2</sub> under pad 2
3	C	14	5	Broken wire to pin 10; poor workmanship



Table 42-3 (Continued)

## Failure Analysis Summary

Code	Group	Ser. no.	Step part failed	Description of Failure
3	C	16	12	Analysis not complete
3	C	21	1	Severely corroded aluminum bonds intact
3	C	24	6	*
3	D	4	1	Pin hole in SiO <sub>2</sub> under lead 4, aluminum
3	D	7	1	Introduced water caused aluminum to disappear
3	E	2	1	Pin hole in SiO <sub>2</sub> under pad 9
4	C	6	8	Scratched aluminum disabling 3 transistors
4	C	26	1	Bond to post defective
4	D	9	5	Damaged in shipment to failure analysis
4	E	7	5	Pin 3 lead shorted to metalization
5				No failures
6	A	4	1	Isolation connection diffusion missing
6	A	5	6	Poor bond to pad 5
6	A	9	13	Analysis not complete
6	A	20	7	Cracked die shorting pins 4, 5, and 6 to ground
6	A	31	12	Analysis not complete
6	A	35	7	Poor bond to ground pad 8
6	C	14	7	Analysis not complete
6	C	23	9	Bond to pad 1 loose
6	D	3	2	Analysis not complete
7	A	3	9	*
7	A	5	10	*
7	A	7	6	Bond at pad 5 lifted; corroded aluminum
7	C	7	12	Analysis not complete
7	C	11	3	Lid broken from package; broken wire
7	C	13	2	Bond to pad 7 loose; corroded aluminum
7	C	19	5	*
7	D	6	2	Corroded aluminum
7	E	2	1	External solder joint defective
7	E	5	10	*
7	F-G	1	5	(Overvoltage during test set-up); no analysis

\* Failure analyzed by Westinghouse as follows:

Code 3: 3 units - Corroded aluminum; 1 unit - Unconfirmed; 1 unit - Pin hole short; 1 unit - Undetermined

Code 7: 4 units - Corroded aluminum

## CONCLUSIONS AND RECOMMENDATIONS

This test program has been successful in determining the effect of heat sterilization on microcircuits, information which has been helpful in the selection of those microcircuits suitable for inclusion in the Sterilization Parts List. It should be remembered that this Report covers results up to 8,000 hours of life test, and that there remain 2,000 hours of life testing, plus a complete computer data analysis.

The t comparison statistic essentially tests the hypothesis that a change in the mean of a control group minus the change in the mean of a test group is zero. Table 42-4 is a tally of those parameters that showed a significant t at the 0.05, 0.01, and 0.005 levels. Consequently, the parameters shown overlap; the 0.05 level includes the 0.01 level parameters, and the 0.01 level parameters include the 0.005 level parameters. The columns are headed by two letters, separated with a slash (/), that indicate the groups being compared. Note the statistically significant differences between groups C/D and D/E through temperature cycling. All three of these groups have seen exactly the same environments up to this point of the test program. The number of statistically significant parameter differences through life test shows that sterilization had little or no effect on the microcircuits. Table 42-2 shows the catastrophic failures by test steps for Groups A and C. Again, the totals are not sufficiently different to say that sterilization affects monolithic silicon integrated circuits.

The best vendor performances were exhibited by Signetics, Fairchild, and Texas Instruments, in that order. Motorola and Westinghouse have changed quality assurance procedures enough to

Table 42-4

Number of Parameters, Out of 142 Total, Showing a Significant Difference at the Level Indicated

Significance of $\Delta M_C - \Delta M_T^*$	$\leq .05$			$\leq .01$			$\leq .005$		
Groups compared	A/C	C/D	D/E	A/C	C/D	D/E	A/C	C/D	D/E
Temperature Cycle	37	52	24	24	28	15	20	25	9
250 hours life	54			26			23		
500 hours life	68			35			29		
1,000 hours life	50			27			20		
2,000 hours life	56	108	41	35	80	12	27	71	8
4,000 hours life	34			20			18		
6,000 hours life	76			52			44		
8,000 hours life									
10,000 hours life									
10,250 hours life									

\* Parameter level = Change in mean of control group ( $\Delta M_C$ ) minus change in mean of test group ( $\Delta M_T$ ).

warrant consideration for re-testing. Fairchild and Texas Instruments were qualified for the Preferred Parts List by a previous qualification test. Signetics, by virtue of the results of this test program, has been added to the list.

With only the 2,000-hour test point data on Groups D and E, it is too premature to answer the question of operational life versus nonoperational life.

The parametric behavior will be presented in the 10,000-hour report, which will include percentile graphs that permit a better engineering presentation of the data. The manufacturers' limits were met for the most part. The parameters that caused the most difficulty were the switching times, although the readings do remain somewhat constant through the test. They are strongly dependent on stray capacitance, however, and the test jigs used do not necessarily match those of the vendors. Failure rate calculations will be reserved for the Final Report.

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#### 43. MICROELECTRONICS ON ATS

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Power and weight limitations on the Applications Technology Satellite (ATS) spacecraft called for maximum use of microelectronics in the Environmental Measurements Experiment (EME) encoder by the Aerospace Division of Westinghouse Electric Company, the spacecraft integration contractor. Texas Instruments series 51 flat-pack circuits were selected for use after study of qualified sources. Up to 110 submodules are used in each ATS spacecraft, with up to 16 flat-packs per submodule. Good mechanical security and excellent heat dissipation are achieved by mounting the submodules on a fluidized aluminum "cookie sheet" split panel with the submodule leads extending through precisely positioned holes for all electrical connections on the underside of the sheet. A relatively high rate of circuit failure during initial electrical inspection over a -20 to +80°C temperature range was completely eliminated in later devices by using gold-gold ball-bonds in place of the original aluminum-gold bonds. However, reliability has been good during qualification tests of all four presently completed EME encoders, three of which use circuits with the aluminum-gold bonds.

#### INTRODUCTION

The EME is the scientific experimental package scheduled to fly on each of the three major variations of the Applications Technology Satellite. These three satellite types are: (1) a synchronous-altitude spin-stabilized satellite, (2) a 6000 mile gravity-gradient stabilized satellite, and (3) a synchronous-altitude gravity-gradient stabilized satellite. Each EME package consists of seven or eight different scientific experiments supplied by universities, NASA, and private contractors. The individual experiments have been chosen to measure the spacecraft environment systematically for damaging effects from radiation and energetic particles, and at the same time obtain additional scientific information about magnetic and electric fields. On the gravity-gradient stabilized satellite it is planned to take advantage of the 130-foot booms as antennae for a radio astronomy experiment.

The individual experiments in each EME contain certain microelectronics. However, the greatest number by far are found in the PFM telemetry encoder used to handle information from the various scientific experiments in the EME package. Encoder specifications are presented in Appendix A.

This paper describes the reliability aspects, method of handling, packaging, and general comments concerning the use of Texas Instruments series 51 integrated circuits in the EME packages.

## BACKGROUND

The Aerospace Division of Westinghouse Electric Co. in Baltimore, Maryland, was awarded a contract to integrate the various scientific experiments in the EME package and to support the spacecraft contractor in the integration of EME into the ATS spacecraft. In addition, Westinghouse was given the responsibility to design the EME structure, telemetry encoder, power supplies, and the command control interfaces between the spacecraft command receiver and the individual experiments. Figure 43-1 shows the configuration of the EME package to be flown on the first ATS mission in a synchronous orbit aboard a spinning spacecraft.

The package mounts cantilevered from the thrust tube. Its overall dimensions are approximately 18 by 10 by 13 inches. All the experiments which must be exposed to the outside of the spacecraft are grouped to view through an aperture 8 by 12 inches to minimize the loss in solar cells which encase the spacecraft. The telemetry encoder, shown in the expanded view in Figure 43-2, is fabricated in a single sheet to simplify interconnections and to eliminate all connectors except those required as interfaces external to the encoder. Because of severe weight and power limitations, the design specification called for the maximum use of microelectronics.

The design study got underway in October 1964, with a close scrutiny of the qualified sources of integrated circuits available at that time. After much discussion and specification manipulation Westinghouse, to insure a tight delivery schedule, was forced to use the existing GSFC specification NAS-51, which was then in use at Texas Instruments. The chief elements of this specification

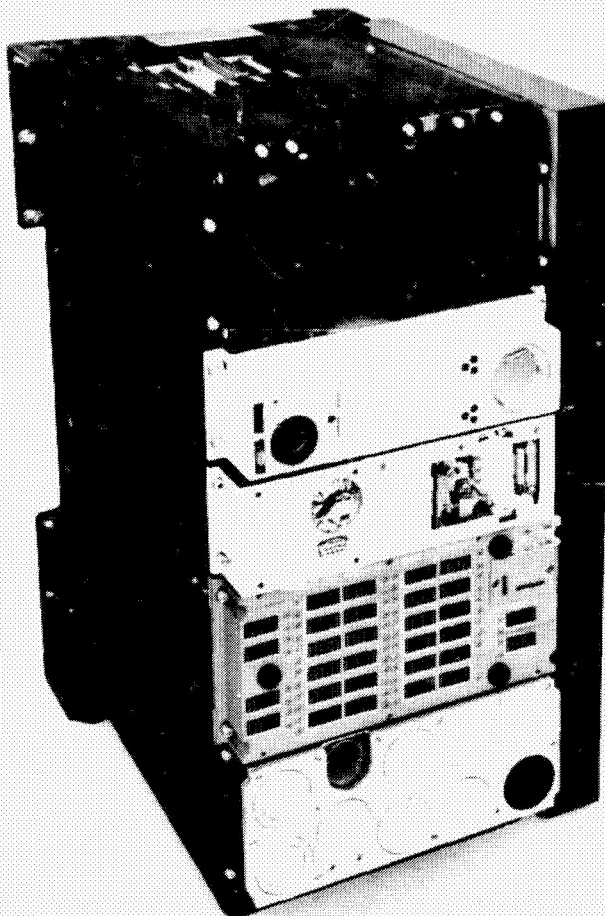


Figure 43-1—ATS-B environmental measurements experiment.

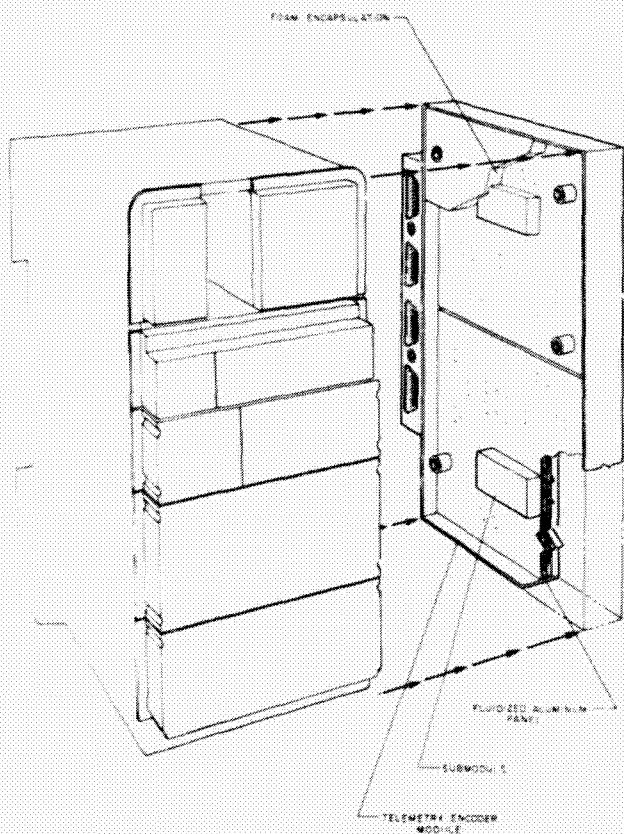


Figure 43-2--Telemetry encoder frame as mounted on EME.

through to a welded-wire interconnection matrix on the reverse side. Figure 43-3 shows the technique with which the pins are connected to the welded-wire matrix. The pins are purposely left long so that, in the event of rework, the module may be cut out and returned several times without extending the submodule or matrix leads. Insulation is provided to the aluminum base plate by first an anodizing coat and then a fluidized epoxy dip approximately 0.01 inch thick. This coating tends to fill all the holes in the plate, necessitating a redrilling with an undersized drill. Indexing is kept to a close tolerance of  $\pm 0.001$  inch by drilling with a tape programmed drilling machine.

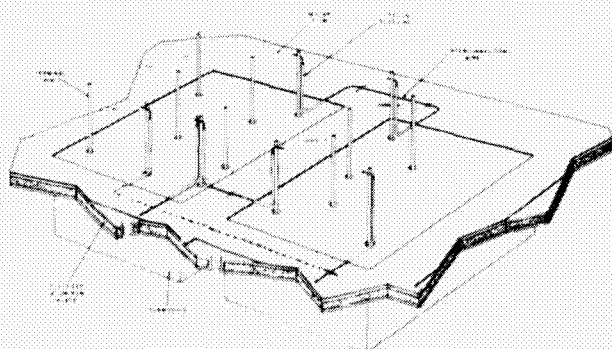


Figure 43-3--Backwiring of submodules on the encoder frame.

were a low-power (X40) visual inspection, centrifuge, variables data recorded before and after a 300-hour burn-in, x-ray, and leak tests. It was felt that a more rigorous specification should be imposed to include features such as monitored vibration, closer visual inspections, serialization, etc. However, this could not be realized until some time later, when the new GSFC General Microelectronics Specification S-711-P1 was issued.

Minor considerations such as delivery schedule and the number of nodes per package made the final choice in favor of Texas Instruments series 51 integrated circuits over Fairchild milliwatt micrologic.

## DESCRIPTION

The single "cookie sheet" encoder is fabricated from 0.030-inch sheet aluminum with a wrap-around frame. Holes are drilled in the base plate to pass the pins from the submodules

The close mounting of each integrated circuit submodule to the aluminum base plate, plus the number of pins through the plate, provides an excellent heat sink. Although the series 51 devices do not dissipate much heat, the reliability is improved by keeping the temperature as low as possible. This technique should prove valuable in other applications, especially where submodules are more densely packed and where heat dissipation is higher in the individual integrated circuits than in the series 51 circuits.



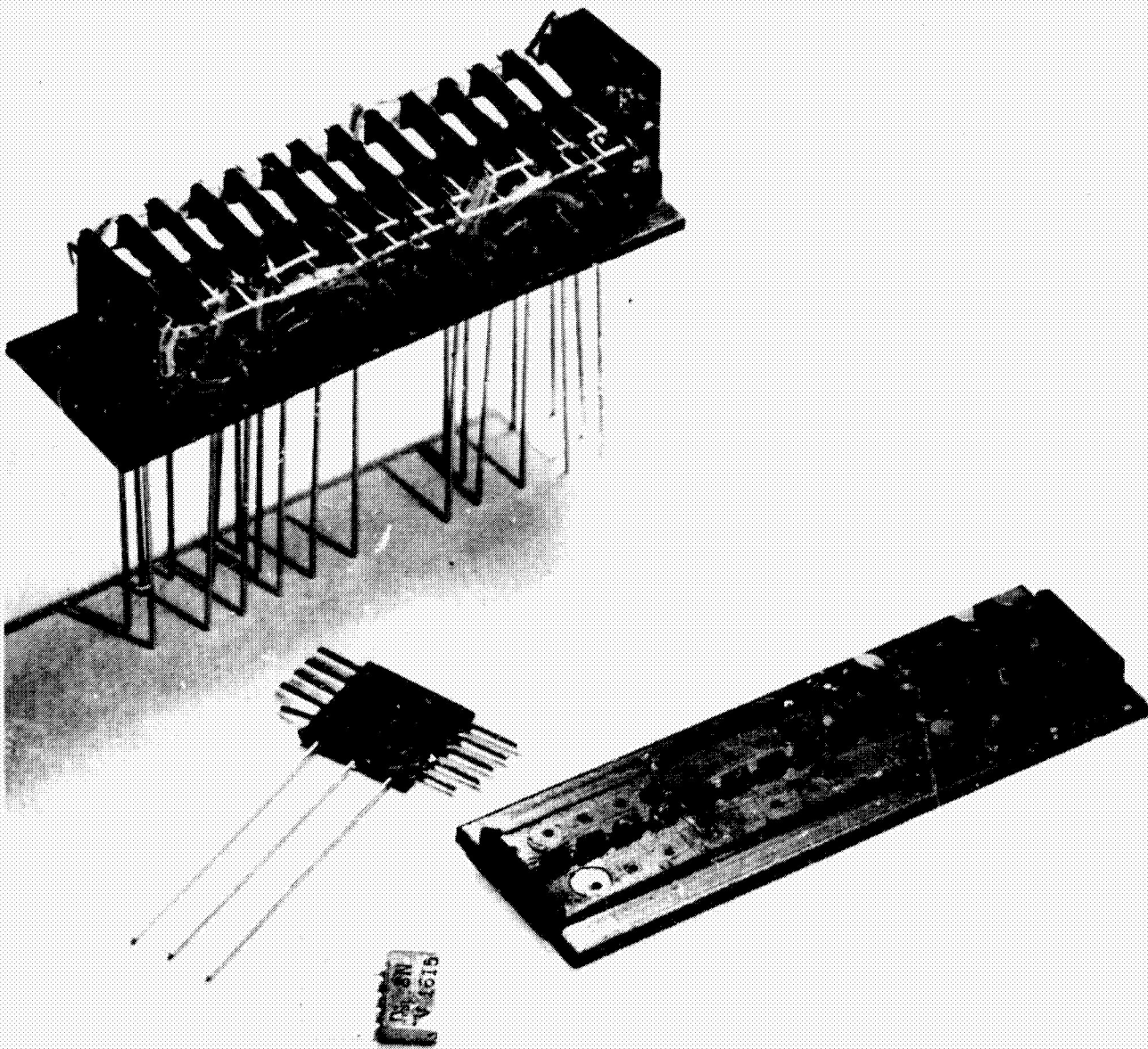


Figure 43-4—Flat-pack submodule.

#### FLAT PACK SUBMODULE

The integrated circuits (flat-packs) are mounted in 24 different types of digital submodules with a maximum of 16 flat-packs per submodule. In a single encoder, as many as 71 flat-pack submodules are used along with 39 cordwood submodules of discrete components for a total of 110 submodules in ATS-A and a total of 89 in ATS-B.

Assembly of the flat-pack submodules is shown in Figures 43-4, 43-5, and 43-6. The individual flat packs are cemented to the spacers with acrylic cement. Spacers and base are made of black phenolic type MFH. Unused connectors in the spacers and flat-packs are cut off and leads are





Included in each flat-pack submodule is one 0.1-mfd filter capacitor for the power bus. This capacitor bypasses noise pulses within each submodule to reduce cross talk between submodules and to provide a distributed filter for the entire network.

The individual submodules are mounted on the main frame as shown in Figure 43-7. The smaller rectangular modules are the flat-packs and the larger square modules are cordwood groups of discrete components. There is no evidence of crowding since the distribution is determined by the welded wire interconnection matrix on the reverse side. For ease and speed of fabrication, the

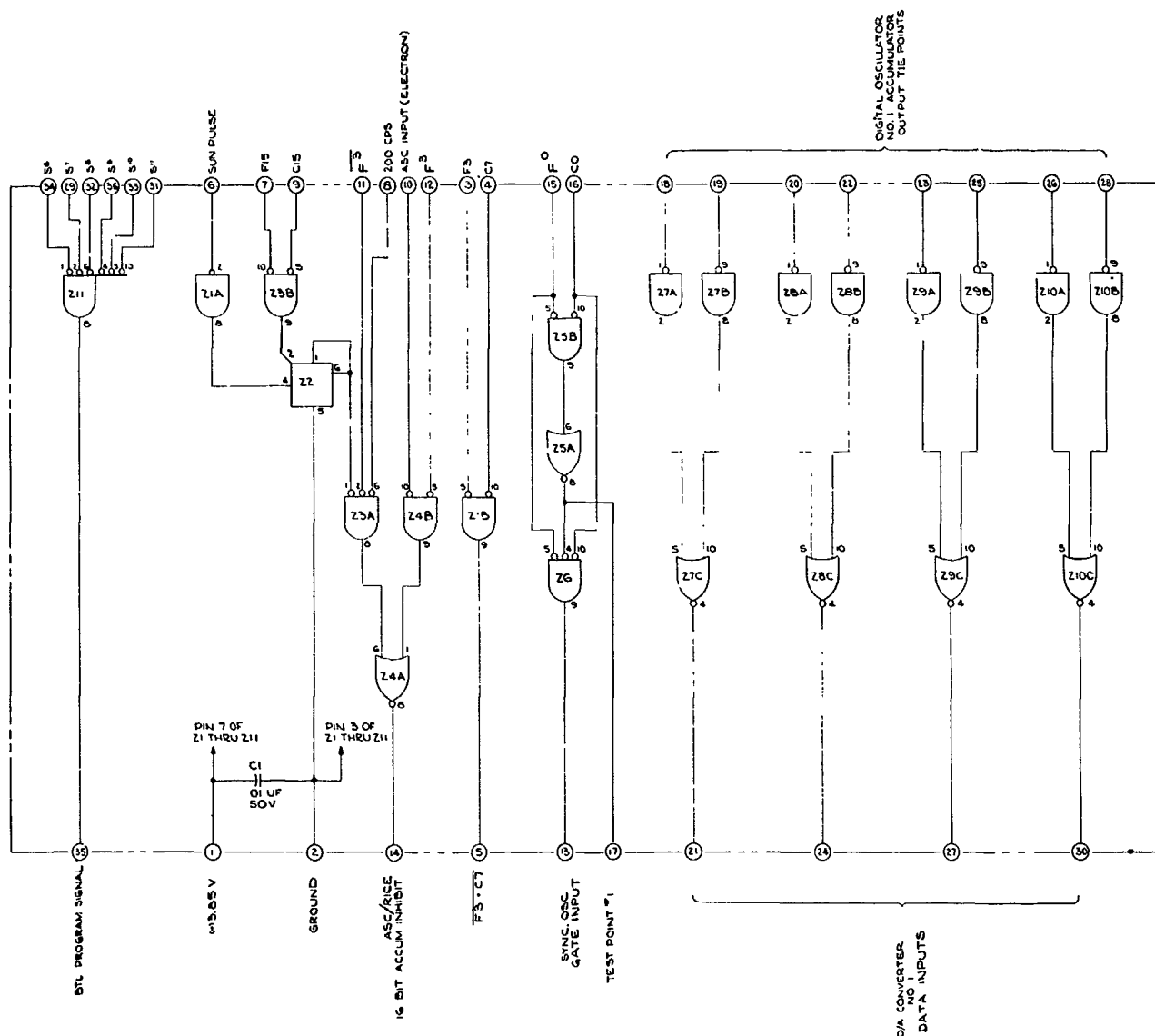


Figure 43-6—Flat-pack submodule logic, circuit diagram.

"cookie sheet" is made in two parts which are brought together in the final assembly operation. The interconnections between halves can be seen in Figure 43-8.

## INTEGRATED CIRCUIT TEST RESULTS

When the integrated circuits were received at Westinghouse, they were given only visual inspection and a leak test. Data are not included here on devices rejected because of incoming visual inspection. However, all other reject data are included in Table 43-1.

It is significant that the highest incident of failures occurs at the first electrical test. This does not imply that the devices were all bad when first turned on. Some devices failed at one of

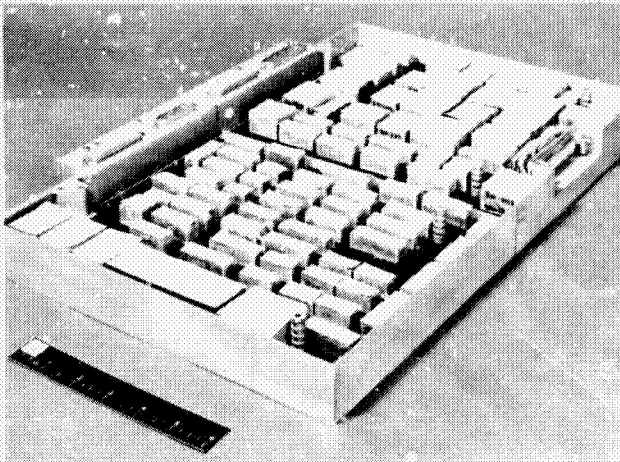


Figure 43-7—Top view of encoder frame.

the three different test temperatures,  $-20^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+80^{\circ}\text{C}$ , imposed during each test phase. Failure analysis on all failed devices to date has diagnosed the causes of failure as follows:

Cracked silicon bar	6
Oxide puncture	5
Mislabeled	5
Defective ball bonds	11
Unknown	6
Total . . . . .	33

Although bad ball-bonds represented the highest single cause of failure in the aluminum-gold devices used in the EME encoder, there was a much more severe problem on another GSFC in-house project at about the same time. This project was plagued with intermittent problems caused by defective ball-bonds in Texas Instruments aluminum-gold series 51 flat-packs manufactured to the NAS-51 specification.

The high ball-bond failure rate occurred in the Optical Aspect Computer for IMP-D (Reference 1), which was used 300 flat-packs per system. In this application one characteristic differed uniquely from the EME encoder: during normal operation there was an interruption of power to the flat-pack logic system at a rate of up to 20 times per minute. This was done to achieve a net power saving, since most of the logic was not in use a good portion of the time. Unfortunately, the

Table 43-1

Series 51 Integrated Circuit Failures as of August 1, 1966

System	Qty.	Leak failures	Submodule Electrical failures		System electrical failures
			Prefoam	Post foam	
Proto. 1	626	7	6	2	1
Flt. 1	626	9	3	1	1
Proto. 2	799	10	5	2	1
		(Gold-Gold Bonding Introduced)			
Flt. 2	799	5	6	1	0
Spares	480	2	3	1	0
Totals	*3330	33	23	7	3

\* 864 manufactured using gold-gold interconnections

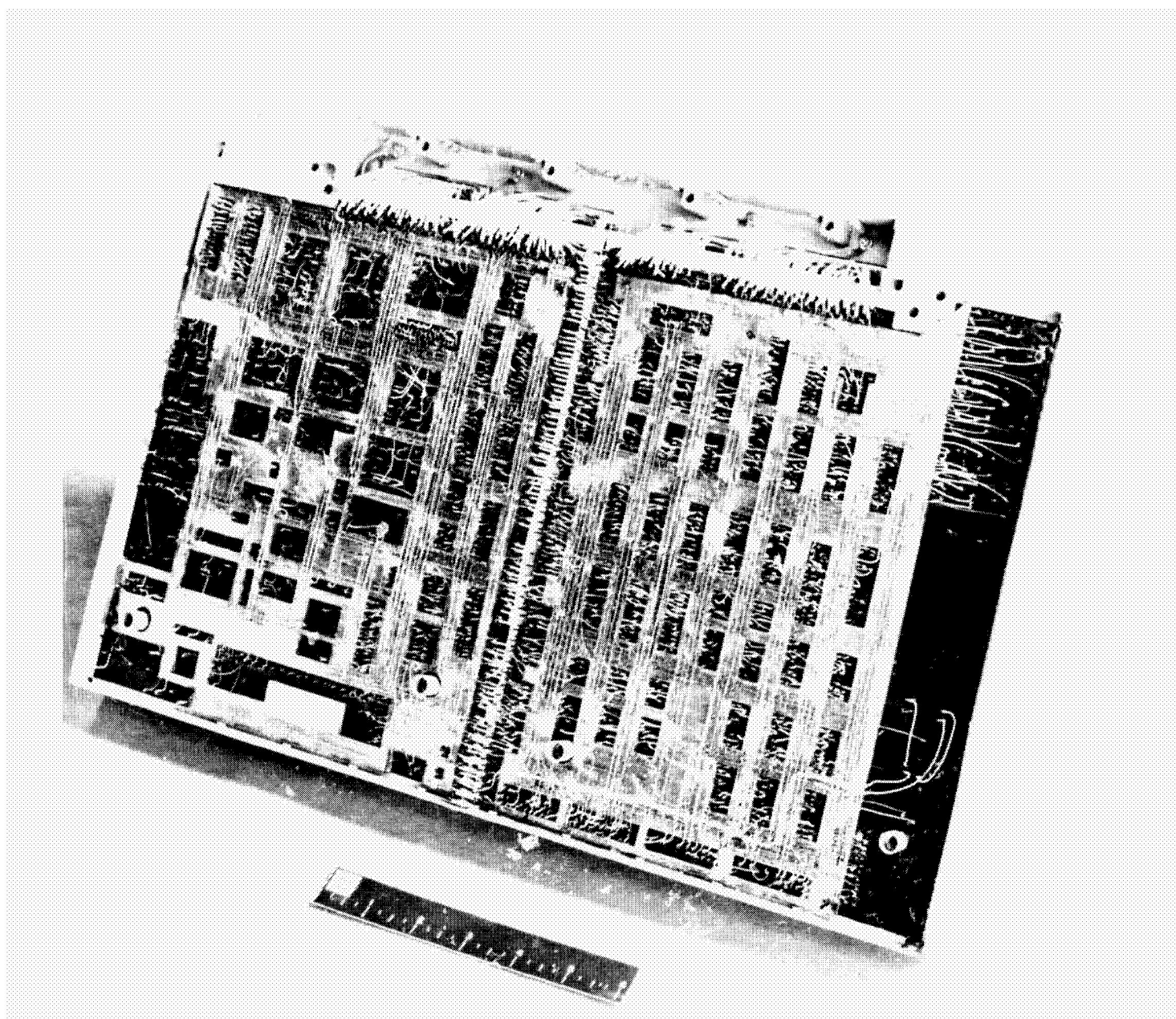


Figure 43-8—Bottom view of encoder frame.

semiconductor power switch was an efficient source of intermittent behavior in flat-pack ball-bonds of the aluminum-gold type. In this one system of 300 flat-packs, more defective ball-bonds were experienced than in the entire EME, which used over twice as many.

Communications were established with Autonetics in Anaheim, California, and with the personnel who were involved in the isolation of a similar problem on the Minuteman II program (Reference 2). Study of the problem and subsequent failure analysis by Texas Instruments, Inc. confirmed that, in at least four cases of intermittents, the trouble was caused by aluminum-gold ball-bonds. The failure analysis cited evidence of the same problem investigated by Autonetics in Reference 2.

It is still not clearly understood just why the power switch produced a higher incidence of intermittent ball-bonds. However, as soon as devices manufactured with the gold-gold interconnections

were introduced, this symptom promptly disappeared. Significantly, the 11 ball-bond failures in EME occurred only when aluminum-gold devices were used.

## SUMMARY

As of this writing, four complete encoders have been fabricated for EME of which three have been given qualification or acceptance tests. The total microelectronic device time totals more than 1,800,000 flat-pack hours.

Three of the systems were fabricated using flat-packs with aluminum-gold interconnections. Most of the fourth system and spares were fabricated with devices having gold-gold bonds. It is interesting to note that, although the process was changed, the failure rate remained essentially the same.

In each encoder there are approximately three flat-packs used for each transistor. However, in the entire EME package (including the power supply and command interface) transistors are used in nearly the same ratio as flat packs. Interestingly, since the outset of this project there has been approximately the same continuing failure rate in transistors and in flat-packs: in each case about 1 percent. Up to the present time there have been no transistor failures in any tests on the complete encoders. However, three flat packs have failed after submodules were assembled into a complete system. These three failures occurred during the encoder preacceptance tests. No failures have occurred during spacecraft qualification or acceptance testing.

## REFERENCES

1. Cliff, R. A., "Power Switching in Digital Systems," NASA TN D-3477, July 1966.
2. Browning, C. V., Colteryahn, L. E., Cummings, D. C., "Failure Mechanisms Associated with Thermocompression Bonds in Integrated Circuits," Physics of Failure in Electronics 4th Annual Symposium, Chicago, Illinois, November 16-18, 1965.

## APPENDIX A

General EME telemetry encoder specifications

	<u>ATS-A</u>	<u>ATS-B</u>
Type	PFM	PFM
No. channels/frame	16	32
No. frames/sequence	16	16
Analog (0-5 volt) data inputs	16	8
Digital data inputs	28	24
Performance parameters:		
analog	9	19
digital	5	7
Sample rate, channels/sec.	50	100
Frame rate, frames/sec.	3.1	3.1
Flat-back power supply	-3.85v±5%	-3.85v±5%
Power consumption	5.0 watts	4.8 watts
Weight	4.9 lbs.	4.0 lbs.
Integrated circuits	799	626
Transistors	279	252
Environmental requirements:		
Temperature	-20°C	+80°C
Maximum vibration 250-400 cps	55g	55g
Vacuum	10 <sup>-5</sup> Torr	10 <sup>-5</sup> Torr